Genesys Logic, Inc.

# GL834

## USB 2.0 SD 3.0/MMC/MS/xD/CF Card Reader Controller

## Datasheet

**Revision 1.01**
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# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | 01/11/2012 | Formal Release |
| 1.01 | 07/06/2012 | 1. Modify Chapter 4 Block Diagram, p.11<br>2. Modify AVDD, DVDD to AVDD33, DVDD33, p8~10<br>3. Modify Chapter 6 Package Dimension, p15 |

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# CHAPTER 1 GENERAL DESCRIPTION

The GL834 is a crystal-less USB 2.0 to Single LUN SD3.0 (UHS-I/SDR-50)/MMC/MS/xD/CF Memory Card Reader controller.

The GL834 is a USB 2.0 Memory Card Reader single chip. It supports USB 2.0 high-speed transmission to CompactFlash™ ,Secure Digital™ (SD), SDHC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro, MMCmobile, Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG™ (MS PRO-HG) and MS PRO Micro and xD-picture card on one chip. It also supports huge density memory cards (up to 2TB), such as SDXC and Memory Stick XC, and high speed memory cards, SD3.0 UHS-I cards. As a single chip solution for USB 2.0 flash card reader, the GL834 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and SD/MMC/MS/xD/CF card interface specification.

The GL834 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and flash card interfaces. Its' pin assignment design fits to card sockets to provide easier PCB layout. Inside the chip, it integrates 5V to 3.3V and 3.3V to 1.8V regulators and power MOSFETs and it enables the function of on-chip clock source (OCCS) which means no external 12MHz XTAL is needed and that effectively reduces the total BOM cost.

 

# CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0
  - Comply with USB Storage Class specification rev. 1.0
  - Support one device address and up to four endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3)
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR)
- Embedded 8051 micro-controller
  - Embedded mask ROM and internal SRAM
- Secure Digital™ (SD)
  - Support SD specification v1.0 / v1.1 / v2.0/ SDHC (Up to 32GB)
  - Support SD specification v3.0 UHS-I: SDR25/SDR50/DDR50
  - Support 1.8V/3.3V switch signal pads
  - Support SDXC (Up to 2TB)
- MultiMediaCard™ (MMC)
  - Support MMC specification v3.x / v4.0 / v4.1 / v4.2.
  - x1 / x4 / x8 bit data bus
- Memory Stick™ / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro /Memory Stick PRO-HG / Memory Stick XC
  - Comply with Memory Stick specification: MS 1.43 / MS PRO 1.05 / MS HG Micro 1.00 / MS PRO-HG Duo 1.03 with 8-bit data bus / MS XC 1.00
  - Support Read/Write quad data access (512Bytex4) for MS PRO-HG to enhance the transmission rate
- Support CompactFlash™ v6.0 with PIO mode 6 / Ultra DMA mode 7 and LBA48 (Capacity up to 144PB)
- Support xD-Picture™ v1.2C Type M/H
- On chip clock source (OCCS) and no need of 12MHz Crystal Clock input.
- On-Chip 5V to 3.3V and 3.3V to 1.8V regulators
- Support 5V to 3.3V Band Gap Regulator for stable voltage supply
- Support 5V power input and 3.3V power input
- Provide Over-Current protection mechanism for safety power supply
- On-Chip power MOSFETs for supplying flash media card power
- Support Power Saving mode/ Selective suspend mode for better power management.
- Support power/memory card access LED
- Package available in 48 pin LQFP (7x7 mm)

 

# CHAPTER 3 PIN ASSIGNMENT

## 3.1 LQFP 48 Pinout

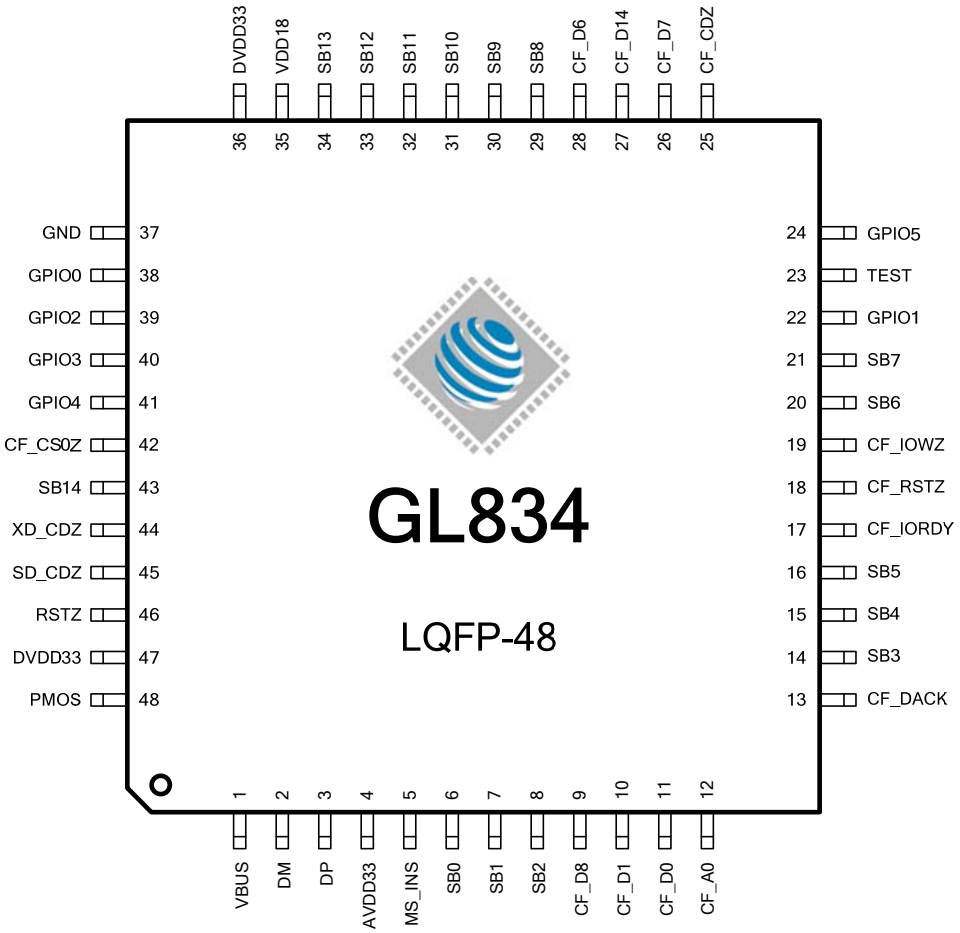


**Figure 3.1 - 48 Pin LQFP Pin out Diagram**

 

## 3.2 Pin List/Descriptions

**Table 3.1 - GL834 Pin List/Descriptions**

| Pin name | LQFP48 | Type | Description |
|---|---|---|---|
| VBUS | 1 | P | VBUS 5V |
| DM | 2 | A | USB D- |
| DP | 3 | A | USB D+ |
| AVDD33 | 4 | P | Analog power 3.3V |
| MS_INS | 5 | I, PU | MS insertion detect<br>0: Card insert<br>1: No card |
| SB0 | 6 | I, PD | CF_D10/xD_D7/SD_D7/MS_CLK |
| SB1 | 7 | I, PD | CF_D9/xD_D6/SD_D6/MS_D3 |
| SB2 | 8 | I, PD | CF_D2/xD_D5 |
| CF_D8 | 9 | I, PD | CF_D8 |
| CF_D1 | 10 | I, PD | CF_D1 |
| CF_D0 | 11 | I, PD | CF_D0 |
| CF_A0 | 12 | I, PD | CF_A0 |
| CF_DACK | 13 | I, PD | CF_DACK |
| SB3 | 14 | I, PD | CF_A1/xD_D4/SD_D5/MS_D2 |
| SB4 | 15 | I, PD | CF_DRQ/xD_D3/SD_D4/MS_D0 |
| SB5 | 16 | I, PD | CF_A2/xD_D2/SD_WP/MS_D1 |
| CF_IORDY | 17 | I, PD | CF_IORDY |
| CF_RSTZ | 18 | I, PD | CF_RSTZ |
| CF_IOWZ | 19 | I, PD | CF_IOWZ |
| SB6 | 20 | I, PD | CF_IORZ/xD_D1/MS_BS |
| SB7 | 21 | I, PD | CF_D15/xD_D0 |
| GPIO1 | 22 | I, PU | Remote Wakeup<br>0:Enable<br>1:Disable(default) |
| TEST | 23 | I, PD | TEST PIN |
| GPIO5 | 24 | I, PU | Power Input Selection<br>0:5V input<br>1:3.3V input(default) |
| CF_CDZ | 25 | I, PU | CF_CDZ |
| CF_D7 | 26 | I, PD | CF_D7 |
| CF_D14 | 27 | I, PD | CF_D14 |
| CF_D6 | 28 | I, PD | CF_D6 |
| SB8 | 29 | I, PD | CF_D13/xD_ALE/SD_D1/MS_D7 |

| | | | |
|---|---|---|---|
| SB9 | 30 | I, PD | CF_D5/xD_CLE/SD_D0/MS_D6 |
| SB10 | 31 | I, PD | CF_D12/xD_WEZ/SD_CLK |
| SB11 | 32 | I, PD | CF_D4/xD_CEZ/SD_CMD |
| SB12 | 33 | I, PD | CF_D11/xD_REZ/SD_D3/MS_D4 |
| SB13 | 34 | I, PD | CF_D3/xD_RBZ/SD_D2/MS_D5 |
| VDD18 | 35 | P | PLL 1.8V Power, the power source of this pin comes from the internal regulator of GL834 and no need of external 1.8V power input |
| DVDD33 | 36 | P | Digital Power 3.3V |
| GND | 37 | P | GND |
| GPIO0 | 38 | I, PD | Power and Access LED |
| GPIO2 | 39 | I, PU | I2C SDA |
| GPIO3 | 40 | I, PU | I2C SCL |
| GPIO4 | 41 | I, PU | Power Saving Mode Selection<br>0:Normal Mode<br>1:Power Saving Mode (default) |
| CF_CS0Z | 42 | I, PD | CF_CS0Z |
| SB14 | 43 | I, PD | CF_CS1Z/xD_WPZ |
| XD_CDZ | 44 | I, PU | xD_CDZ |
| SD_CDZ | 45 | I, PU | SD_CDZ |
| RSTZ | 46 | I, PU | RESET |
| DVDD33 | 47 | P | Digital Power 3.3V |
| PMOS | 48 | P | Card Power 500mA |

**Notation:**

| | | |
|---|---|---|
| **Type** | **O** | Output |
| | **I** | Input |
| | **B** | Bi-directional |
| | **pu** | Internal pull-up when input |
| | **pd** | Internal pull-down when input |
| | **P** | Power / Ground |
| | **A** | Analog |

# CHAPTER 4 BLOCK DIAGRAM

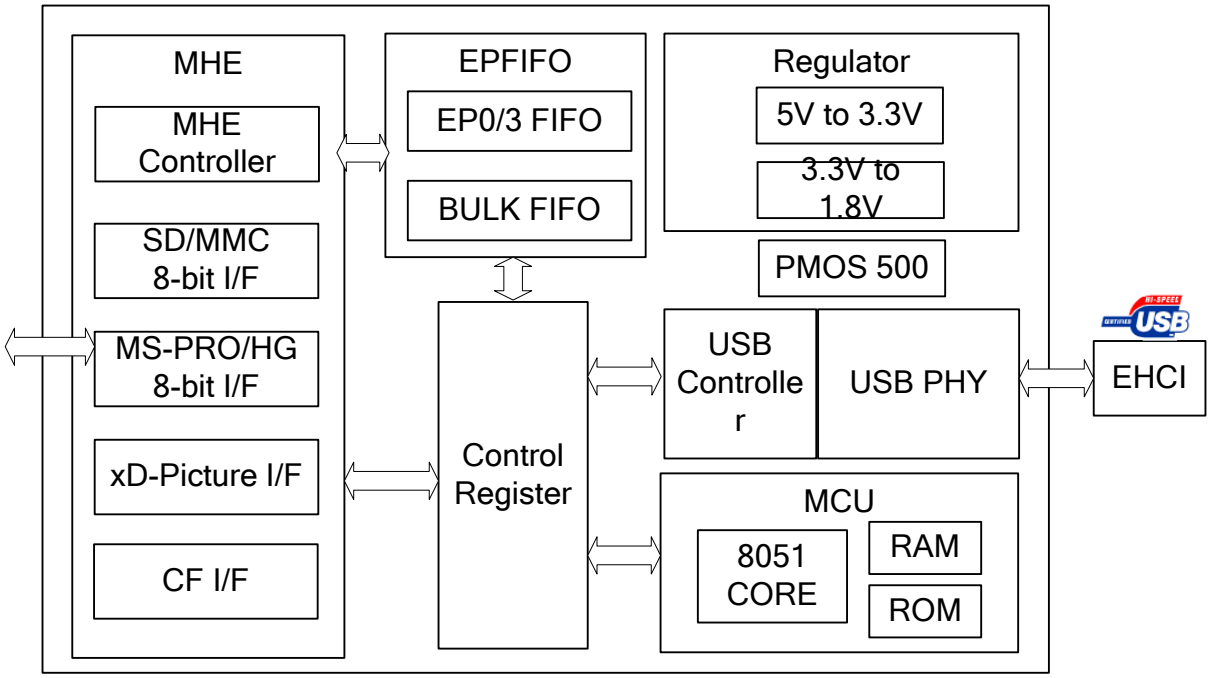


**Figure 4.1 - Functional Block Diagram**

## 4.1 USB PHY

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic. On chip clock source and no need of 12MHz Crystal Clock input.

## 4.2 USB Controller

The USB controller, which contains USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

## 4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), Interrupt FIFO (FIFO3), Bulk In/Out FIFO

- **Control FIFO** FIFO of control endpoint 0. It is 64-byte FIFO and used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by micro-control

## 4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** FW code on ROM
- **RAM** Internal RAM area for MCU access

## 4.5 MHE

- **MIF** Media Interface: CF/xD/SD/MMC/MS/MS PRO/MS PRO-HG
- **MCFIFO** It can access by MCU for memory card short data packet.

## 4.6 Regulator

- **5V to 3.3V** Band Gap Regulator for stable voltage supply for USB PHY, PMOS..
  When Power source is 3.3V, the 5V to 3.3V regulator will be disabled.
- **3.3V to 1.8V** For core logic and internal memory.

## 4.7 PMOS

On-Chip power MOSFETs provide Over-Current protection mechanism

# CHAPTER 5 ELECTRICAL CHARACTERISTICS

## 5.1 Absolute Maximum Ratings

**Table 5.1 - Absolute Maximum Ratings**

| Parameter | Value |
|---|---|
| Storage Temperature | -65°C to +150 °C |
| DC Input Voltage to Any Pin | -0.5V to +5.8V |

## 5.2 Operating Conditions

**Table 5.2 - Operating Conditions**

| Parameter | Value |
|---|---|
| Ta (Ambient Temperature Under Bias) | 0°C to 70°C |
| Supply Voltage (5V Power Source) | 4.75V to 5.25V |
| Supply Voltage (3.3V Power Source) | 3.135V to 3.465V |
| Ground Voltage | 0V |

## 5.3 DC Characteristics

**Table 5.3 - DC Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 5V source | 4.75 | - | 5.25 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | - | | V |
| $V_{IL}$ | Input Low Voltage | | | - | 0.4 | V |
| $I_I$ | Input Leakage current | $0 < V_{IN} < V_{CC}$ | -10 | - | 10 | µA |
| $V_{OH}$ | Output High Voltage | | 2.8 | - | - | V |
| $V_{OL}$ | Output Low Voltage | | - | - | 0.4 | V |
| $I_{OH}$ | Output Current High | | - | 8 | - | mA |
| $I_{OL}$ | Output Current Low | | - | 8 | - | mA |
| $C_{IN}$ | Input Pin Capacitance | | - | 5 | - | pF |
| $I_{SUSP}$ | Suspend current | 1.5K external pull-up included | - | - | 450 | µA |
| $I_{CC}$ | Supply current | Connect to USB with 8051 operating | - | - | 70 | mA |

## 5.4 AC Characteristics of Reset Timing

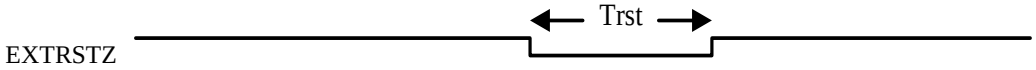


**Figure 5.1 - Timing Diagram of Reset width**

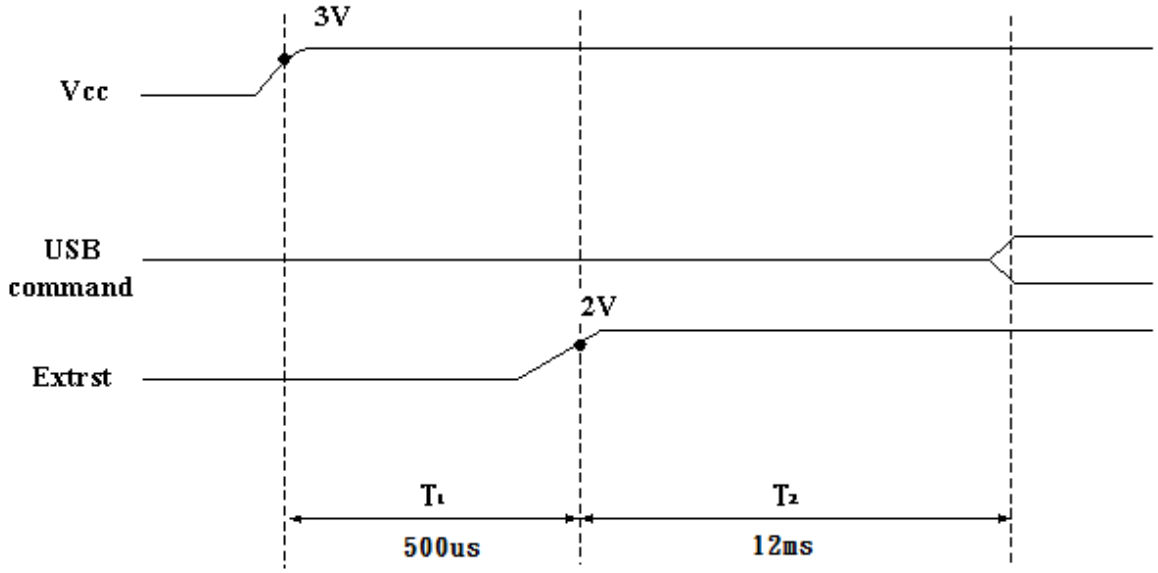


**Figure 5.2 - Timing Diagram of Power Good to USB command receive ready**

**Table 5.4 - Reset Timing**

| Parameter | Description | Min. | Unit |
|---|---|---|---|
| Trst | Chip reset sense timing width | 1 | ms |
| T1 | External reset valid from power up to high | 0.5 | ms |
| T2 | Reset Desertions to respond USB command ready | 12 | ms |

# CHAPTER 6 PACKAGE DIMENSION

| SYMBOL | DIMENSION MM (MIL) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.60 (63.0) |
| A1 | 0.05 (2.0) | --- | 0.15 (5.9) |
| A2 | 1.35 (53.1) | 1.40 (55.1) | 1.45 (57.1) |
| b | 0.17 (6.7) | 0.22 (8.7) | 0.27 (10.6) |
| b1 | 0.17 (6.7) | 0.20 (7.9) | 0.23 (9.1) |
| c | 0.09 (3.5) | --- | 0.20 (7.9) |
| c1 | 0.09 (3.5) | --- | 0.16 (6.3) |
| D | 9.00 (354.3) BSC | | |
| D1 | 7.00 (275.6) BSC | | |
| e | 0.50 (19.7) BSC | | |
| E | 9.00 (354.3) BSC | | |
| E1 | 7.00 (275.6) BSC | | |
| L | 0.45 (17.7) | 0.60 (23.6) | 0.75 (29.5) |
| L1 | 1.00 (39.4) REF | | |
| R1 | 0.08 (3.1) | --- | --- |
| R2 | 0.08 (3.1) | --- | 0.20 (7.9) |
| S | 0.20 (7.9) | --- | --- |
| aaa | 0.20 (7.9) | | |
| bbb | 0.20 (7.9) | | |
| ccc | 0.08 (3.1) | | |
| ddd | 0.08 (3.1) | | |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | --- | --- |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |

NOTE: 1. REFER TO JEDEC MS-026/BBC
2. ALL DIMENSIONS IN MILLIMETERS.

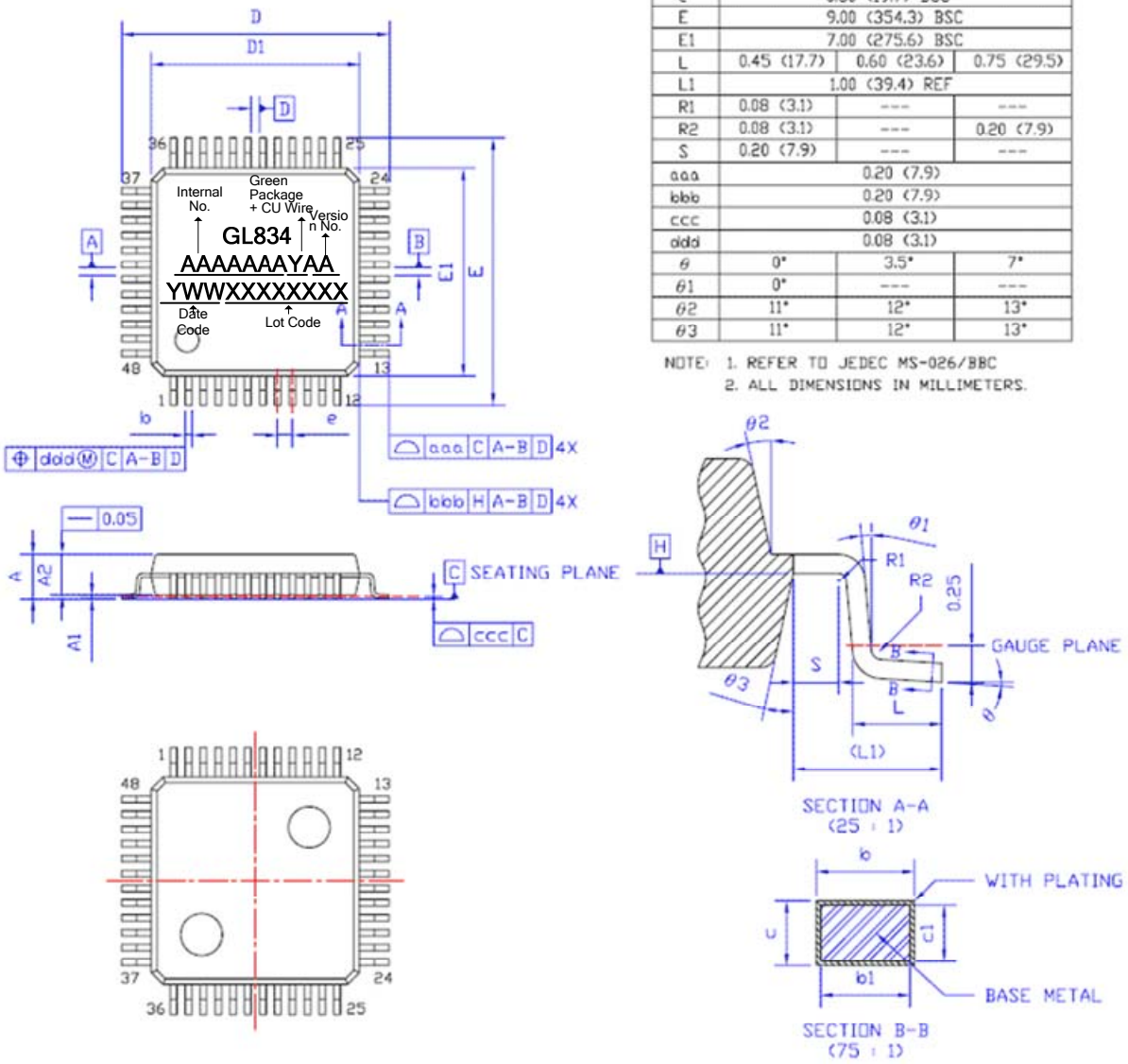


**Figure 6.1 - LQFP 48 Pin Package**

 

# CHAPTER 7 ORDERING INFORMATION

**Table 7.1 - Ordering Information**

| Part Number | Package | Green/Wire Material | Version | Status |
|---|---|---|---|---|
| GL834-MNYXX | LQFP 48 | Green Package + CU Wire | XX | Available |