5-A, WIDE INPUT RANGE, STEP-DOWN SWIFT™ CONVERTER

Check for Samples: TPS5450-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Wide Input Voltage Range: 5.5 V to 36 V**
- **Up to 5-A Continuous (6-A Peak) Output Current**
- **High Efficiency Greater than 90% Enabled by 110-mΩ Integrated MOSFET Switch**
- **Wide Output Voltage Range: Adjustable Down to 1.22 V with 1.5% Initial Accuracy**
- **Internal Compensation Minimizes External Parts Count**
- **Fixed 500-kHz Switching Frequency for Small Filter Size**
- **18-μA Shutdown Supply Current**
- **Improved Line Regulation and Transient Response by Input Voltage Feed Forward**
- **System Protected by Overcurrent Limiting, Overvoltage Protection, and Thermal Shutdown**
- **–40°C to 125°C Operating Junction Temperature Range**
- **Available in Small Thermally Enhanced 8-Pin SOIC PowerPAD™ Package**
- **For SWIFT™ Documentation, Application Reports and Design Software, See the TI Website at www.ti.com/swift**

APPLICATIONS

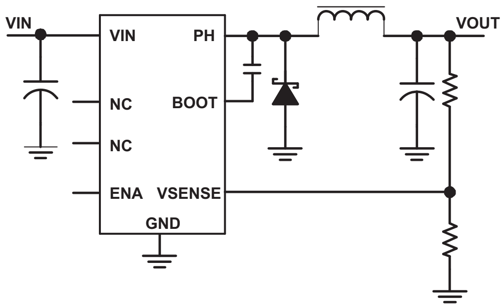
- **High-Density Point-of-Load Regulators**
- **LCD Displays, Plasma Displays**
- **Battery Chargers**
- **12-V/24-V Distributed Power Systems**

DESCRIPTION

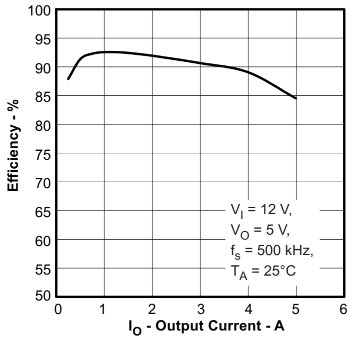
As a member of the SWIFT™ family of DC/DC regulators, the TPS5450 is a high-output-current PWM converter that integrates a low-resistance high-side N-channel MOSFET. Included on the substrate with the listed features are a high-performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions, an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V, an internally set slow-start circuit to limit inrush currents, and a voltage feed-forward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 μA typically. Other features include an active-high enable, overcurrent limiting, overvoltage protection, and thermal shutdown. To reduce design complexity and external component count, the TPS5450 feedback loop is internally compensated.

The TPS5450 device is available in a thermally enhanced, 8-pin SOIC PowerPAD™ package. TI provides evaluation modules and software tools to aid in achieving high-performance power supply designs to meet aggressive equipment development cycles.

Simplified Schematic



Efficiency vs Output Current



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Thermally Enhanced SOIC – DDA	Reel of 2500	TPS5450QDDARQ1	5450Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

V_I	Input voltage range	VIN	–0.3 V to 40 V(3)
		BOOT	–0.3 V to 50 V
		PH (steady-state)	–0.6 V to 40 V(3)
		ENA	–0.3 V to 7 V
		BOOT-PH	10 V
		VSENSE	–0.3 V to 3 V
		PH (transient < 10 ns)	–1.2 V
I_O	Source current	PH	Internally Limited
I_{lkg}	Leakage current	PH	10 μA
T_J	Operating virtual-junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS5450-Q1	UNITS
		DDA	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	48.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	47.1	
θ_{JB}	Junction-to-board thermal resistance(4)	22.5	
ψ_{JT}	Junction-to-top characterization parameter(5)	5.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	22.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

DISSIPATION RATINGS[1] [2]

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT
8-Pin DDA (4-layer board with solder)[3]	30°C/W

(1) Maximum power dissipation may be limited by overcurrent protection.

(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See *Thermal Calculations* in applications section of this data sheet for more information.

(3) Test board conditions:
  (a) 2 in x 1.85 in, 4 layers, 0.062-in (1,57-mm) thickness
  (b) 2-oz copper traces located on the top and bottom of the PCB
  (c) 2-oz copper ground planes on the two internal layers
  (d) Four thermal vias in the PowerPAD area under the device package

RECOMMENDED OPERATING CONDITIONS

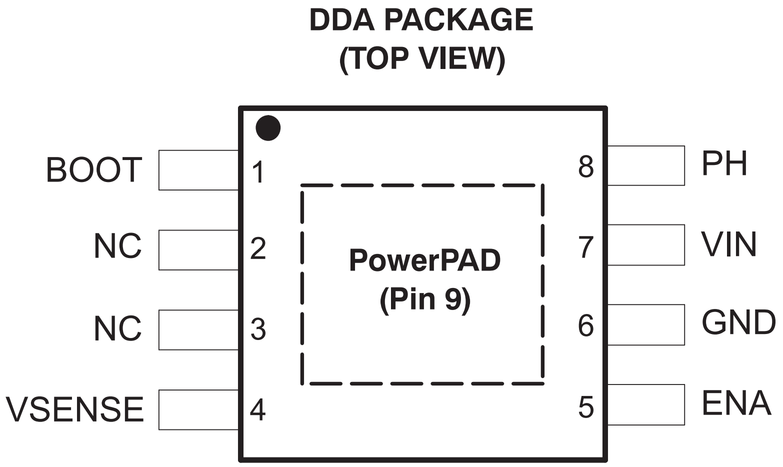
		MIN	MAX	UNIT
V_I	Input voltage range	5.5	36	V
T_J	Operating virtual-junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, VIN = 5.5 V to 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	μA
UNDERVOLTAGE LOCK OUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T_J = 25°C	1.202	1.221	1.239	V
		I_O = 0 A – 5 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87	89		%
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0~100%)		5.4	8	10	ms
CURRENT LIMIT						
	Current limit		5.7	7.5	9.0	A
	Current limit hiccup time		13	16	21	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		°C
OUTPUT MOSFET						
$r_{DS(on)}$	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
				110	230	

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
BOOT	1	Boost capacitor for the high-side FET gate driver. Connect 0.01-μF low-ESR capacitor from BOOT pin to PH pin.
NC	2, 3	No internal connection
VSENSE	4	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	Ground. Connect to thermal pad.
VIN	7	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high-quality low-ESR ceramic capacitor.
PH	8	Source of the high side power MOSFET. Connected to external inductor and diode.
PowerPAD	9	GND pin must be connected to the exposed pad for proper operation.

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

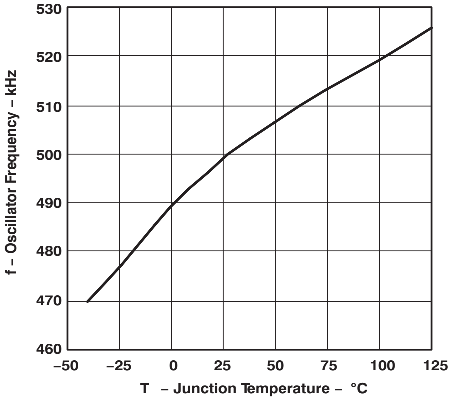


Figure 1.

NON-SWITCHING QUIESCENT CURRENT vs JUNCTION TEMPERATURE

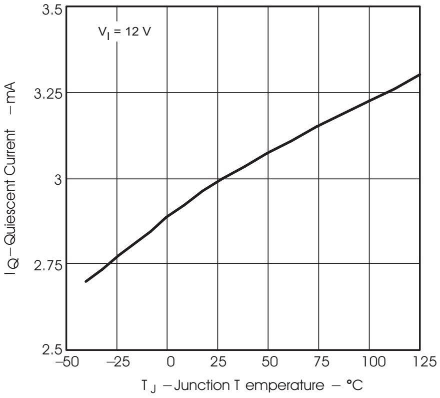


Figure 2.

SHUTDOWN QUIESCENT CURRENT vs INPUT VOLTAGE

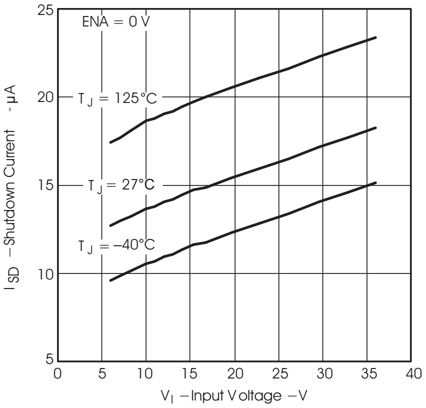


Figure 3.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

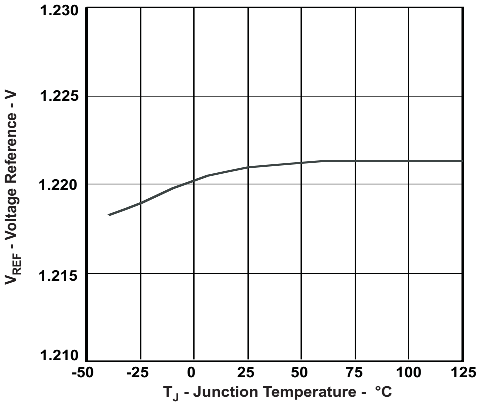


Figure 4.

ON RESISTANCE vs JUNCTION TEMPERATURE

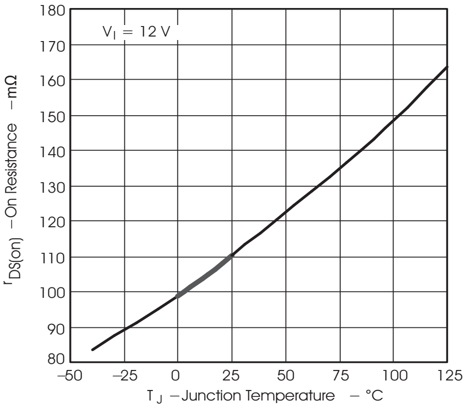


Figure 5.

INTERNAL SLOW START TIME vs JUNCTION TEMPERATURE

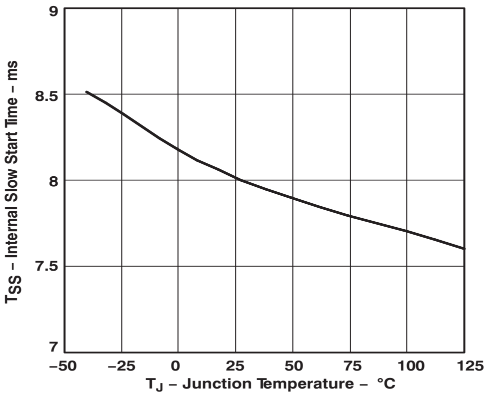


Figure 6.

TYPICAL CHARACTERISTICS (continued)

MINIMUM CONTROLLABLE ON TIME vs JUNCTION TEMPERATURE

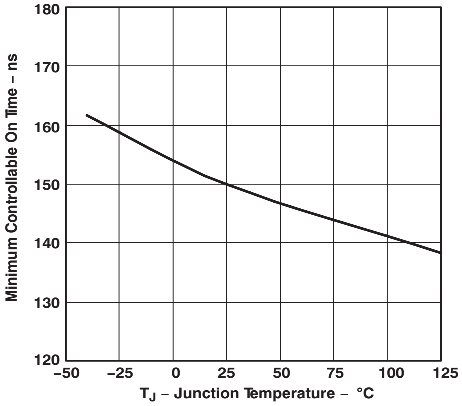


Figure 7.

MINIMUM CONTROLLABLE DUTY RATIO vs JUNCTION TEMPERATURE

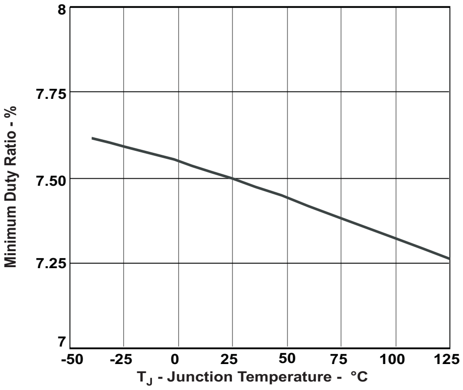
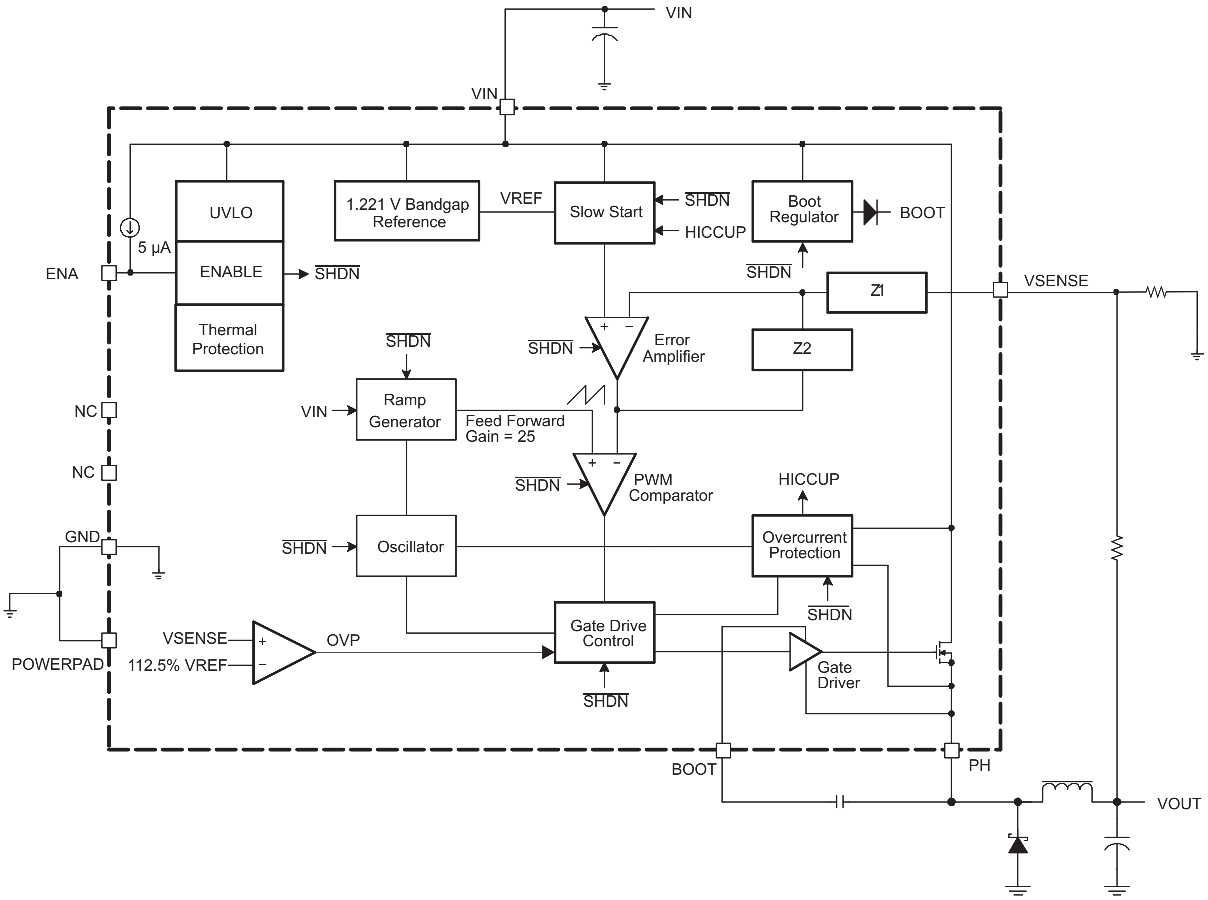


Figure 8.

APPLICATION INFORMATION

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Oscillator Frequency

The internal free-running oscillator sets the PWM switching frequency at 500 kHz. The 500-kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

Enable (ENA) and Internal Slow Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V disables the regulator and activates the shutdown mode. The quiescent current of the TPS5450 in shutdown mode is 18 µA (typical).

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value, linearly. The internal slow start time is 8 ms (typical).

Undervoltage Lockout (UVLO)

The TPS5450 incorporates an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

Boost Capacitor (BOOT)

Connect a 0.01-μF low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

Output Feedback (VSENSE) and Internal Compensation

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

The TPS5450 implements internal compensation to simplify the regulator design. Because the TPS5450 uses voltage-mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* section for more details.

Voltage Feed Forward

The internal voltage feed forward provides a constant dc power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed forward gain:

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk}-\text{pk}}} \tag{1}$$

The typical feed forward gain of TPS5450 is 25.

Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high-gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error-voltage magnitude is converted to a pulse width, which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system ignores the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting mode is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, i.e. hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow start circuit.

Overvoltage Protection

The TPS5450 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% × VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET is forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET is enabled again.

Thermal Shutdown

The TPS5450 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

PCB Layout

Connect a low ESR ceramic bypass capacitor to the VIN pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5450 ground pin. The best way to do this is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7 μF ceramic with a X5R or X7R dielectric.

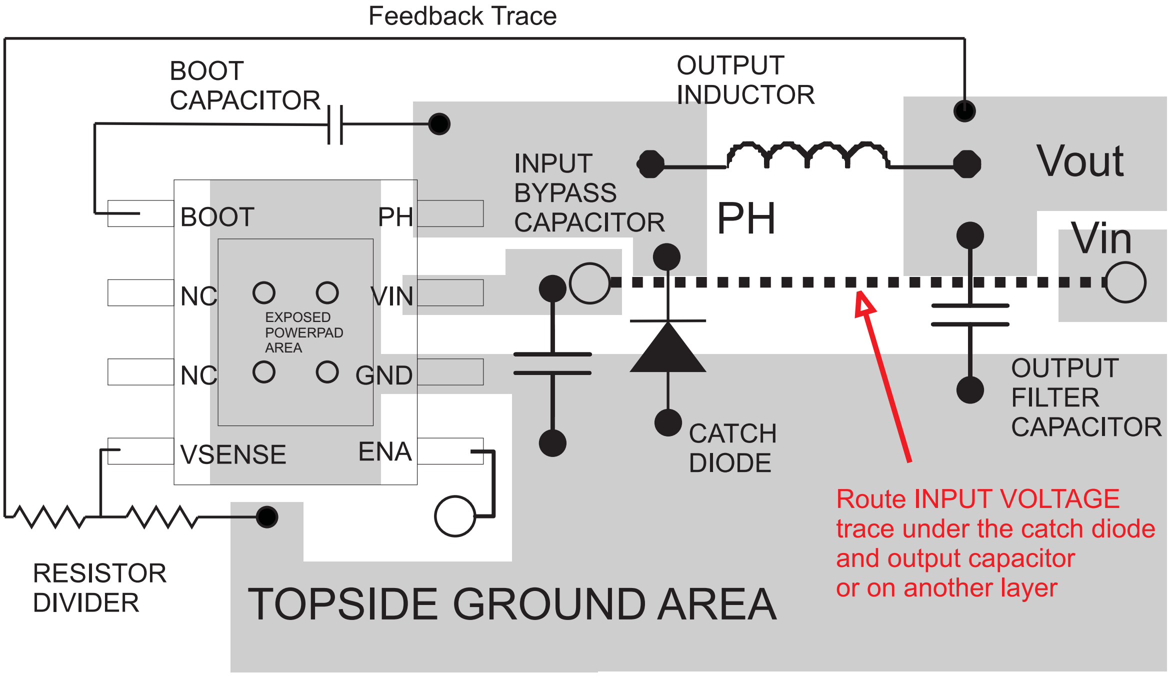
There should be a ground area on the top layer directly underneath the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown below.

The PH pin should be routed to the output inductor, catch diode and boot capacitor. Since the PH connection is the switching node, the inductor should be located very close to the PH pin and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings also may be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

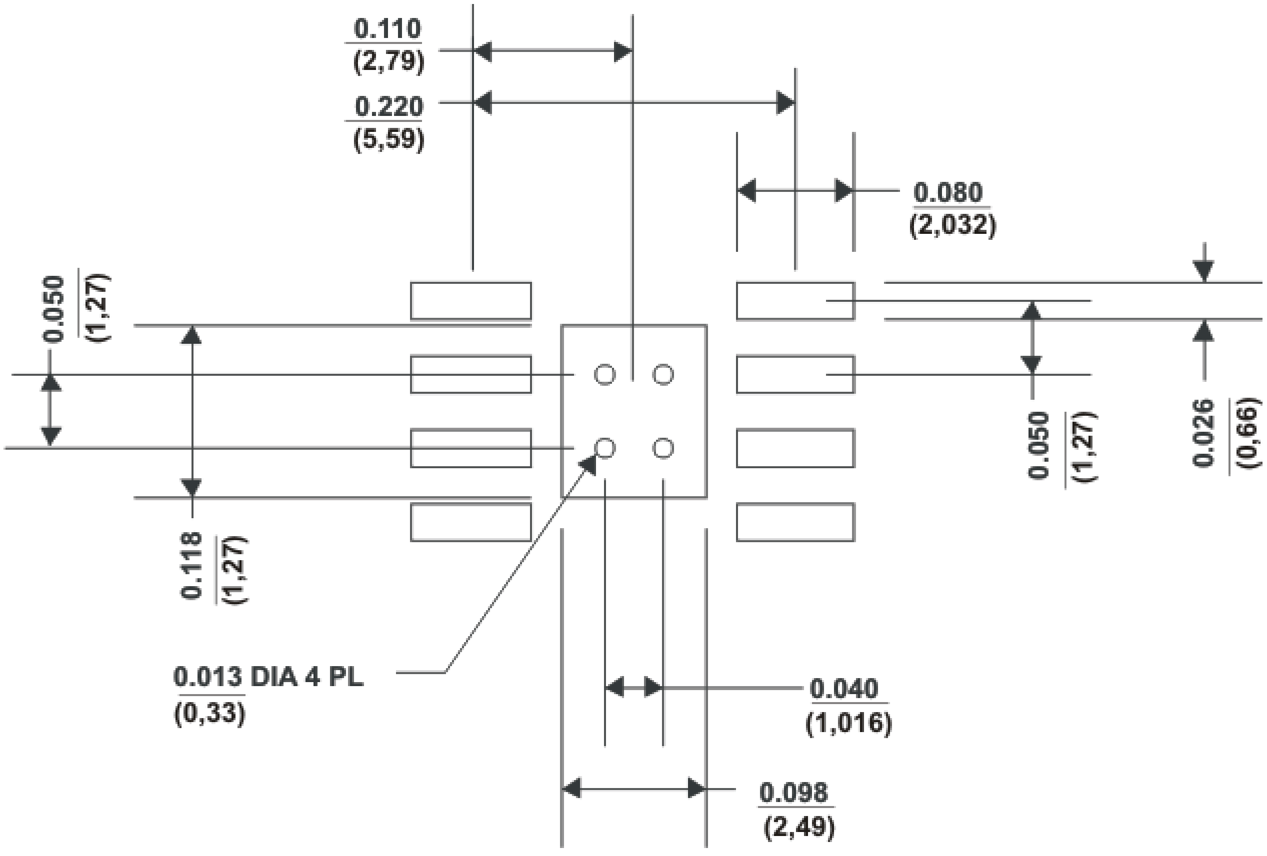
Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pin-out, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If using the grounding scheme shown in Figure 9, use a via connection to a different layer to route to the ENA pin.



○ Signal VIA

Figure 9. Design Layout



All dimensions in inches (millimeters)

Figure 10. TPS5450 Land Pattern

Application Circuits

Figure 11 shows the schematic for a typical TPS5450 application. The TPS5450 can provide up to 5-A output current at a nominal output voltage of 5 V. For proper thermal performance, the exposed PowerPAD™ underneath the device must be soldered down to the printed-circuit board.

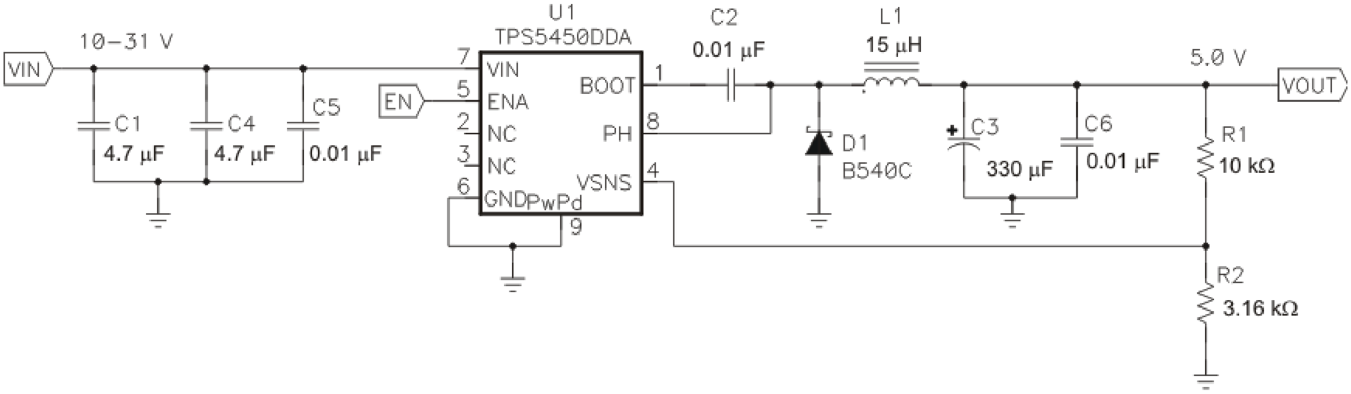


Figure 11. Application Circuit, 12-V to 5.0-V

Design Procedure

The following design procedure can be used to select component values for the TPS5450. Alternately, the SWIFT™ Designer Software may be used to generate a complete design. The SWIFT™ Designer Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

Design Parameters

For this design example, use the following as the input parameters:

DESIGN PARAMETER[1]	EXAMPLE VALUE
Input voltage range	10 V to 31 V
Output voltage	5 V
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

Switching Frequency

The switching frequency for the TPS5450 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

Input Capacitors

The TPS5450 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum recommended decoupling capacitance is 4.7 μF. A high-quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, so long as the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple.

This input ripple voltage can be approximated by Equation 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \tag{2}$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_{IN} is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor. For this design, the input capacitance consists of two 4.7 μF capacitors, C1 and C4, in parallel. An additional high-frequency bypass capacitor, C5 is also used.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 3 :

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \tag{3}$$

In this case the input ripple voltage would be 281 mV and the RMS ripple current would be 2.5 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen input decoupling capacitor is rated for 50 V, and the ripple current capacity is greater than 2.5 A each, providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Additionally some bulk capacitance may be needed, especially if the TPS5450 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Because the TPS5450 is an internally compensated device, a limited range of filter component types and values can be supported.

Inductor Selection

To calculate the minimum value of the output inductor, use Equation 4:

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW(MIN)}} \tag{4}$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak-to-peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current, and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5450, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages can be obtained when paired with the proper output capacitor, the peak switch current will be well below the current limit set point, and relatively low load currents can be sourced before discontinuous operation.

For this design example use K_{IND} = 0.2 and the minimum inductor value is calculated to be 10.4 μH. A higher standard value is 15 μH, which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 5:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^{2} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}} \right)^{2}} \tag{5}$$

and the peak inductor current can be determined with Equation 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}} \tag{6}$$

For this design, the RMS inductor current is 5.004 A, and the peak inductor current is 5.34 A. The chosen inductor is a Sumida CDRH1127/LD-150 15μH. It has a minimum rated current of 5.65 A for both saturation and RMS current. In general, inductor values for use with the TPS5450 are in the range of 10 μH to 100 μH.

Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because, along with the inductor ripple current, it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is desirable to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz, as this frequency range has adequate phase boost to allow for stable operation. For this design example, it is assumed that the intended closed loop crossover frequency is between 2590 Hz and 24 kHz and also below the ESR zero of the output capacitor. Under these conditions the closed loop crossover frequency is related to the LC corner frequency by:

$$f_{CO} = \frac{f_{LC}^{\;2}}{85\ V_{OUT}} \tag{7}$$

And the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \tag{8}$$

For a desired crossover of 12 kHz and a 15-μH inductor, the calculated value for the output capacitor is 330 μF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR should be:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \tag{9}$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}\,(MAX) = \frac{ESR_{MAX}\ x\ V_{OUT}\ x\ \left(V_{IN(MAX)}\ -\ V_{OUT} \right)}{N_{C}\ x\ V_{IN(MAX)}\ x\ L_{OUT}\ x\ F_{SW}} \tag{10}$$

Where:

ΔV_{PP} is the desired peak-to-peak output ripple.

N_C is the number of parallel output capacitors.

F_{SW} is the switching frequency.

For this design example, a single 330-µF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 40 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 10TPB330M, rated at 10 V with a maximum ESR of 35 mΩ and a ripple current rating of 3 A. An additional small 0.1-µF ceramic bypass capacitor, C6 is also used in this design.

The minimum ESR of the output capacitor should also be considered. For good phase margin, the ESR zero when the ESR is at a minimum should not be too far above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C}\right] \tag{11}$$

Where:

N_C is the number of output capacitors in parallel.

F_{SW} is the switching frequency.

Other capacitor types can be used with the TPS5450, depending on the needs of the application.

Output Voltage Setpoint

The output voltage of the TPS5450 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using Equation 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \tag{12}$$

For any TPS5450 design, start with an R1 value of 10 kΩ. For an output voltage closest to but at least 5 V, R2 is 3.16 kΩ.

Boot Capacitor

The boot capacitor should be 0.01 µF.

Catch Diode

The TPS5450 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is VINMAX + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B540A is chosen, with a reverse voltage of 40 V, forward current of 5 A, and a forward voltage drop of 0.5 V.

ADVANCED INFORMATION

Output Voltage Limitations

Due to the internal design of the TPS5450, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230\right) + V_D\right) - \left(I_{OMAX} \times R_L\right) - V_D \tag{13}$$

Where

V_{INMIN} = minimum input voltage
I_{OMAX} = maximum load current
V_D = catch diode forward voltage.
R_L= output inductor series resistance.

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time, which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D \tag{14}$$

Where

V_{INMAX} = maximum input voltage
I_{OMIN} = minimum load current
V_D = catch diode forward voltage.
R_L= output inductor series resistance.

This equation assumes nominal on resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to ensure proper functionality.

Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5450. These designs are based on certain assumptions and will tend to always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS5450. Equation 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)} \tag{15}$$

Where

Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz
Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz
Fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed forward gain and output filter characteristics, the closed loop transfer function can be derived.

Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: Pcon = $I_{OUT}{}^{2}$ x $R_{DS(on)}$ x V_{OUT}/V_{IN}
Switching Loss: Psw = V_{IN} x I_{OUT} x 0.01
Quiescent Current Loss: Pq = V_{IN} x 0.01
Total Loss: Ptot = Pcon + Psw + Pq
Given T_A => Estimated Junction Temperature: $T_J = T_A$ + Rth x Ptot
Given T_{JMAX} = 125°C => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX}$ – Rth x Ptot

PERFORMANCE GRAPHS

The performance graphs (Figure 12 through Figure 18) are applicable to the circuit in Figure 11. Ta = 25 °C. unless otherwise specified.

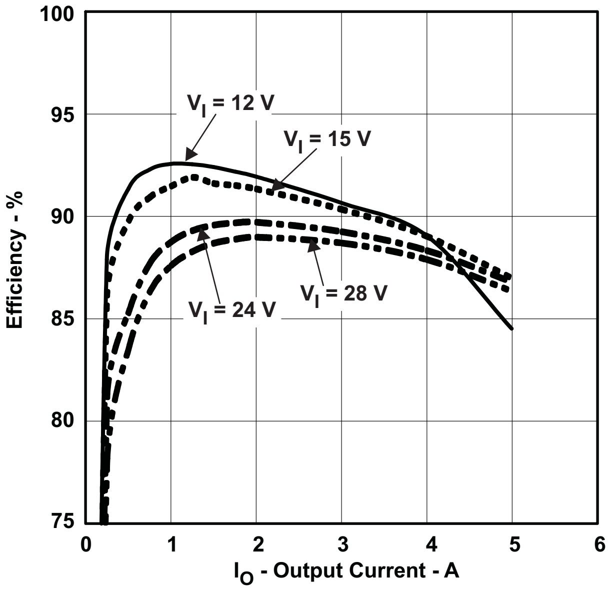


Figure 12. Efficiency vs. Output Current

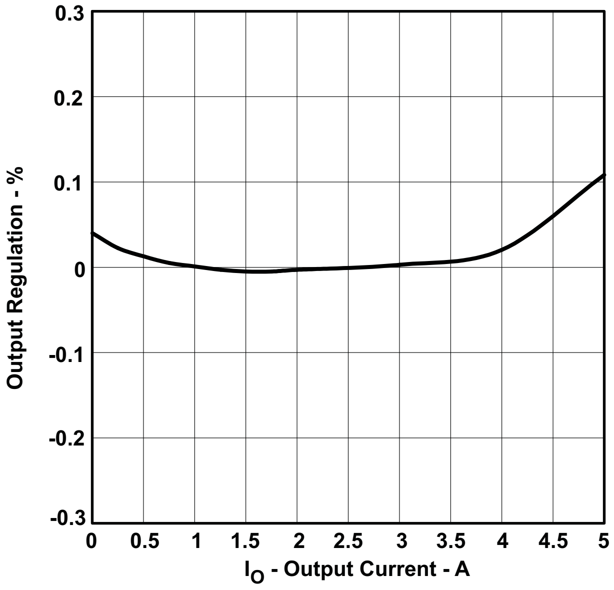


Figure 13. Output Regulation % vs. Output Current

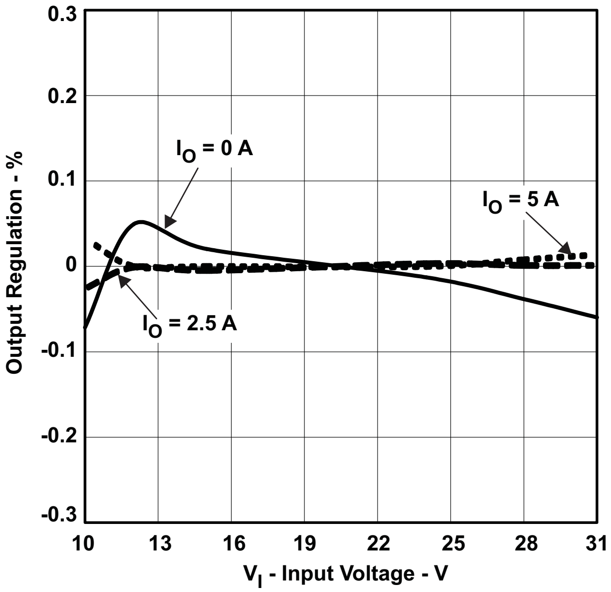


Figure 14. Output Regulation % vs. Input Voltage

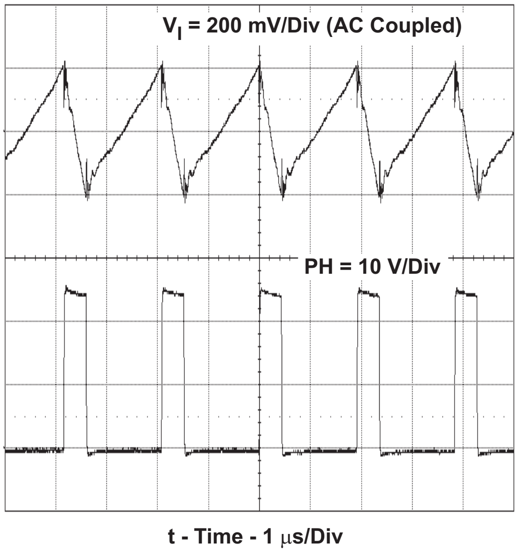


Figure 15. Input Voltage Ripple and PH Node, Io = 5 A.

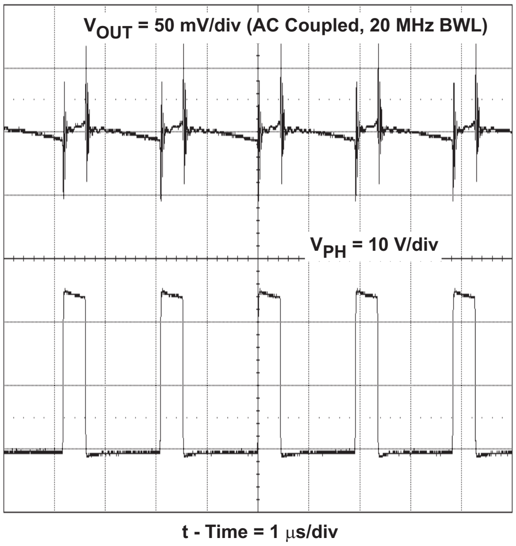


Figure 16. Output Voltage Ripple and PH Node, Io = 5 A

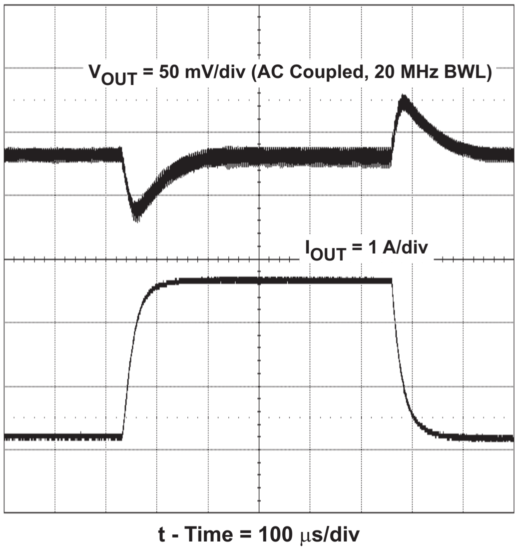


Figure 17. Transient Response, Io Step 1.25 to 3.75 A.

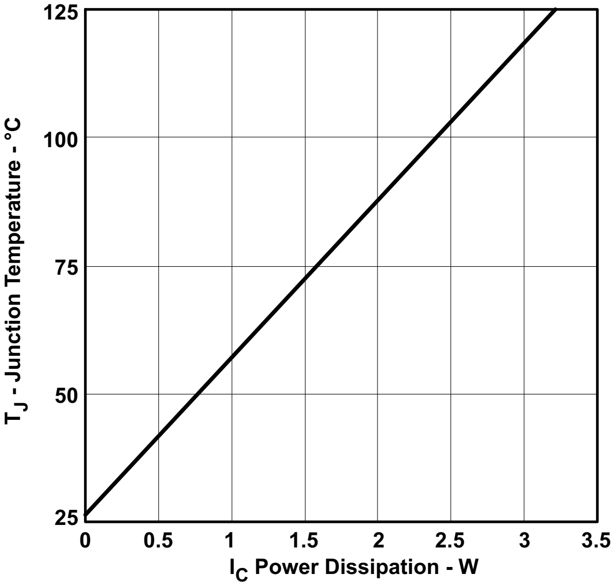


Figure 18. TPS5450 Power Dissipation vs Junction Temperature.

REVISION HISTORY

Changes from Original (July 2008) to Revision A	**Page**
• Added *Thermal Table*	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5450QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5450Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS5450-Q1 :

- Catalog: TPS5450

- Enhanced Product: TPS5450-EP

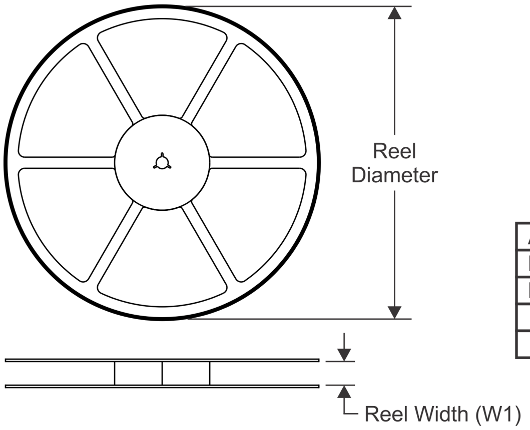
NOTE: Qualified Version Definitions:

  - Catalog - TI's standard catalog product

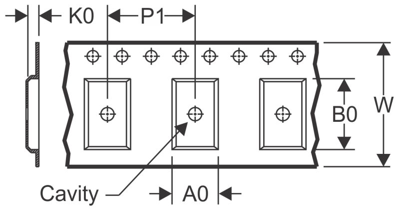
  - Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

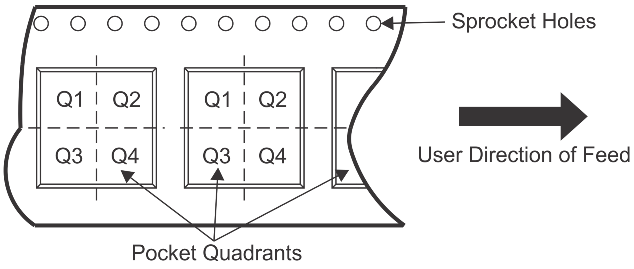


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

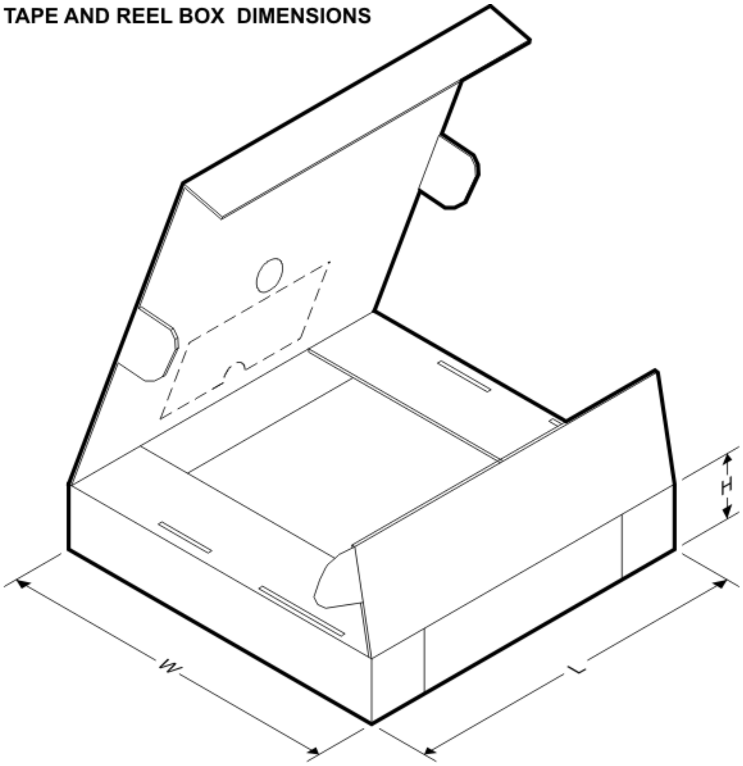
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5450QDDARQ1	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

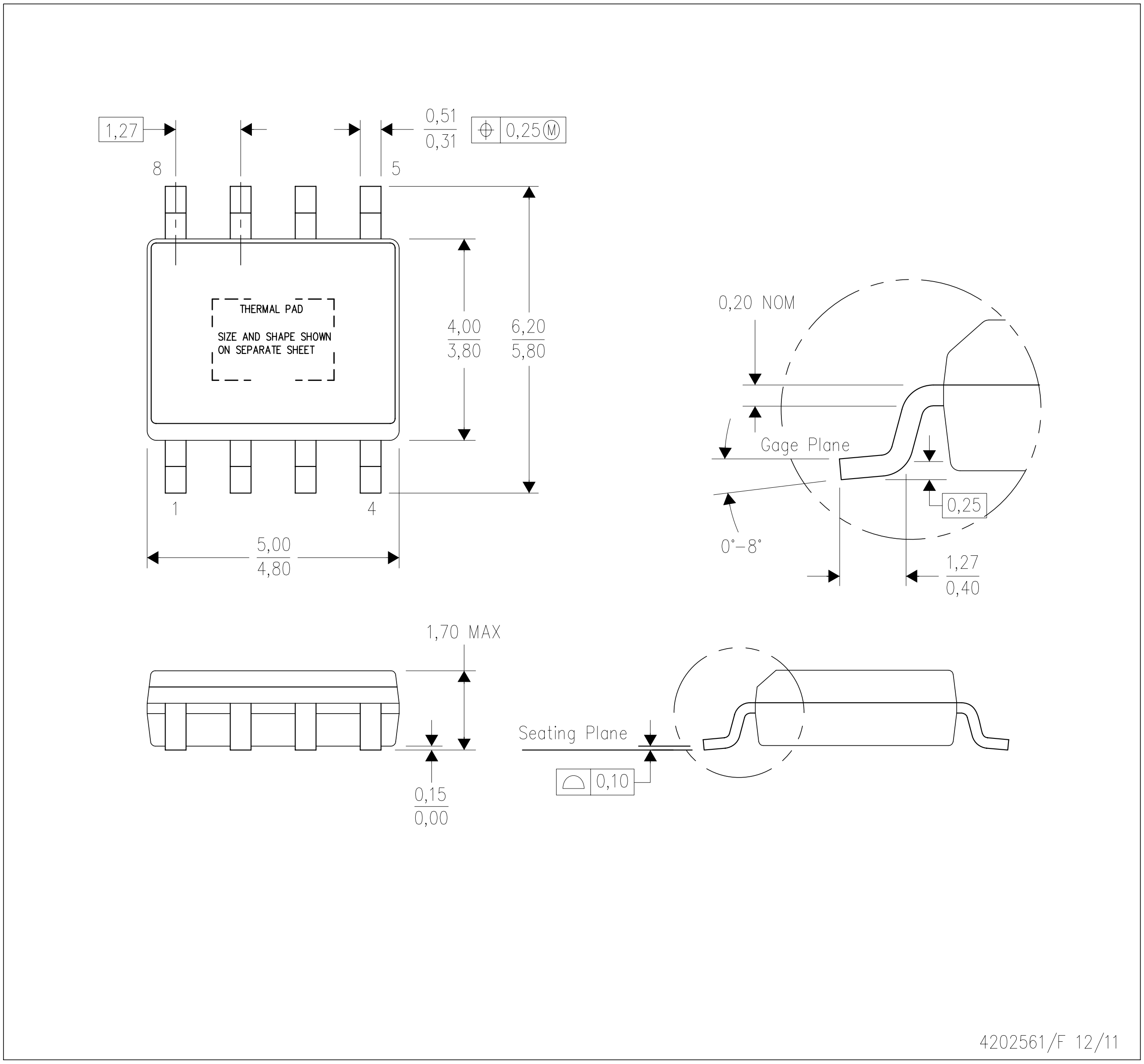
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5450QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

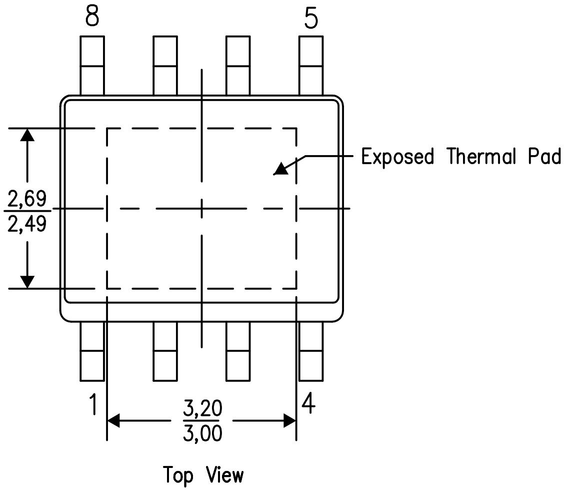
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–7/L 05/12

NOTE: A. All linear dimensions are in millimeters

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