LMV751 Low Noise, Low Vos, Single Op Amp

Check for Samples: LMV751

FEATURES

- **Low Noise 6.5nV/√Hz**
- **Low V_{OS} (0.05mV typ.)**
- **Wideband 4.5MHz GBP typ.**
- **Low Supply Current 500uA typ.**
- **Low Supply Voltage 2.7V to 5.0V**
- **Ground-Referenced Inputs**
- **Unity Gain Stable**
- **Small Package**

APPLICATIONS

- **Cellular Phones**
- **Portable Equipment**
- **Radio Systems**

DESCRIPTION

The LMV751 is a high performance CMOS operational amplifier intended for applications requiring low noise and low input offset voltage. It offers modest bandwidth of 4.5MHz for very low supply current and is unity gain stable.

The output stage is able to drive high capacitance, up to 1000pF and source or sink 8mA output current.

It is supplied in the space saving SOT-23-5 Tiny package.

The LMV751 is designed to meet the demands of small size, low power, and high performance required by cellular phones and similar battery operated portable electronics.

Connection Diagram

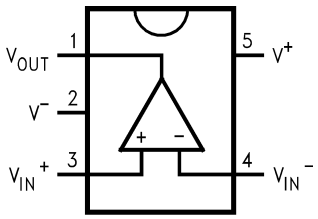


Figure 1. SOT-23-5 Top View

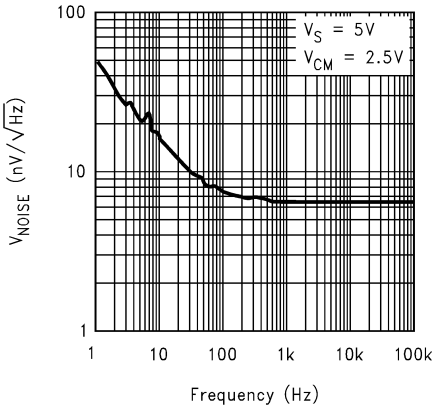


Figure 2. Voltage Noise

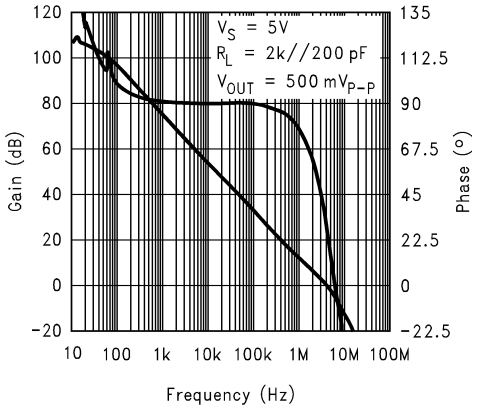


Figure 3. Gain/Phase

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999–2013, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Differential Input Voltage	±Supply Voltage
Supply Voltage (V^+ - V^-)	5.5V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature (T_J) (4)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 1000pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions

Supply Voltage	2.7V to 5.0V
Temperature Range	$-40°C \le T_J \le 85°C$
Thermal Resistance (θ_{JA}) (1)	
DBV-5 Package, SOT-23-5	274°C/W

(1) All numbers are typical, and apply to packages soldered directly onto PC board in still air.

2.7V Electrical Characteristics

$V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.35V$, $T_A = 25°C$ unless otherwise stated. **Boldface limits** apply over the Temperature Range.

Symbol	Parameter	Condition	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		0.05	1.0 **1.5**	mV max
V_{CM}	Input common-Mode Voltage Range	For CMRR ≥ 50dB		0	V min
			1.4	1.3	V max
CMRR	Common Mode Rejection Ratio	$0V < V_{CM} < 1.3V$	100	85 **70**	dB min
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7V$ to 5.0V	107	85 **70**	dB min
I_S	Supply Current		0.5	0.8 **0.85**	mA max
I_{IN}	Input Current		1.5	100	pA max
I_{OS}	Input Offset Current		0.2		pA
A_{VOL}	Voltage Gain	R_L = 10k Connect to $V^+/2$ V_O = 0.2V to 2.2V	120	110 **95**	dB min
		R_L = 2k Connect to $V^+/2$ V_O = 0.2V to 2.2V	120	100 **85**	

(1) Typical values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis

Copyright © 1999–2013, Texas Instruments Incorporated

2.7V Electrical Characteristics (continued)

V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, T_A = 25°C unless otherwise stated. **Boldface limits** apply over the Temperature Range.

Symbol	Parameter	Condition	Typ (1)	Limit (2)	Units
V_O	Positive Voltage Swing	R_L = 10k Connect to $V^+/2$	2.62	2.54 **2.52**	V min
		R_L = 2k Connect to $V^+/2$	2.62	2.54 **2.52**	
V_O	Negative Voltage Swing	R_L = 10k Connect to $V^+/2$	78	140 **160**	mV max
		R_L = 2k Connect to $V^+/2$	78	160 **180**	
I_O	Output Current	Sourcing, V_O = 0V V_{IN} (diff) = ±0.5V	12	6.0 **1.5**	mA min
		Sinking, V_O = 2.7V V_{IN} (diff) = ±0.5V	11	6.0 **1.5**	
e_n (10Hz)	Input Referred Voltage Noise		15.5		nV/√Hz
e_n (1kHz)	Input Referred Voltage Noise		7		nV/√Hz
e_n (30kHz)	Input Referred Voltage Noise		7	10	nV/√Hz max
I_N(1kHz)	Input Referred Current Noise		0.01		pA/√Hz
GBW	Gain-Bandwidth Product		4.5	2	MHZ min
SR	Slew Rate		2		V/µs

5.0V Electrical Characteristics

V^+ = 5.0V, V^- = 0V, V_{CM} = 2.5V, T_A = 25°C unless otherwise stated.**Boldface limits** apply over the Temperature Range.

Symbol	Parameter		Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		0.05	1.0 **1.5**	mV max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 3.6V	103	85 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		0	V min
			3.7	3.6	V max
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5.0V	107	85 **70**	dB min
I_S	Supply Current		0.6	0.9 **0.95**	mA max
I_{IN}	Input Current		1.5	100	pA max
I_{OS}	Input offset Current		0.2		pA
A_{VOL}	Voltage Gain	R_L = 10k Connect to $V^+/2$ V_O = 0.2V to 4.5V	120	110 **95**	db min
		R_L = 2k Connect to $V^+/2$ V_O = 0.2V to 4.5V	120	100 **85**	
V_O	Positive Voltage Swing	R_L = 10k Connect to $V^+/2$	4.89	4.82 **4.80**	V min
		R_L = 2k Connect to $V^+/2$	4.89	4.82 **4.80**	
V_O	Negative Voltage Swing	R_L = 10k Connect to $V^+/2$	86	160 **180**	mV max
		R_L = 2k Connect to $V^+/2$	86	180 **200**	

(1) Typical values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis

Copyright © 1999–2013, Texas Instruments Incorporated

5.0V Electrical Characteristics (continued)

V^+ = 5.0V, V^- = 0V, V_{CM} = 2.5V, T_A = 25°C unless otherwise stated. **Boldface limits** apply over the Temperature Range.

Symbol	Parameter		Typ (1)	Limit (2)	Units
I_O	Output Current	Sourcing, V_O = 0V V_{IN} (diff) = ±0.5V	15	8.0 **2.5**	mA min
		Sinking, V_O = 5V V_{IN} (diff) = ±0.5V	20	8.0 **2.5**	
e_n (10Hz)	Input Referred Voltage Noise		15		nV/ $\sqrt{Hz}$
e_n (1kHz)	Input Referred Voltage Noise		6.5		nV/ $\sqrt{Hz}$
e_n (30kHz)	Input Referred Voltage Noise		6.5	10	nV/ $\sqrt{Hz}$ max
I_N (1kHz)	Input Referred Current Noise		0.01		pA/$\sqrt{Hz}$
GBW	Gain-Bandwidth Product		5	2	MHz min
SR	Slew Rate		2.3		V/µs

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Performance Characteristics

Supply Current vs. Voltage

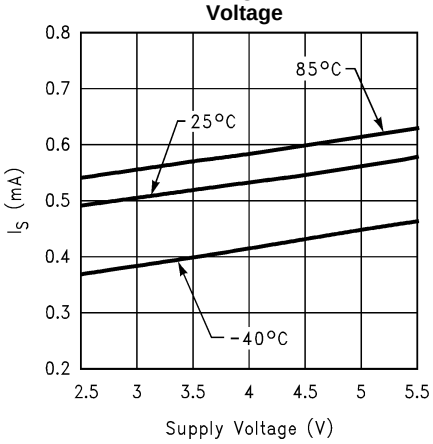


Figure 4.

V_{OS} vs. V_{CM}, V^+ = 2.7V

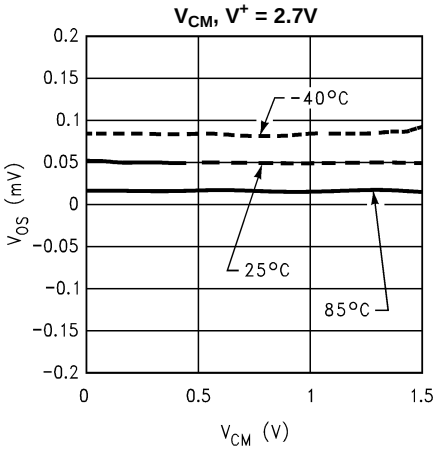


Figure 5.

V_{OS} vs. V_{CM}, V^+ = 5.0V

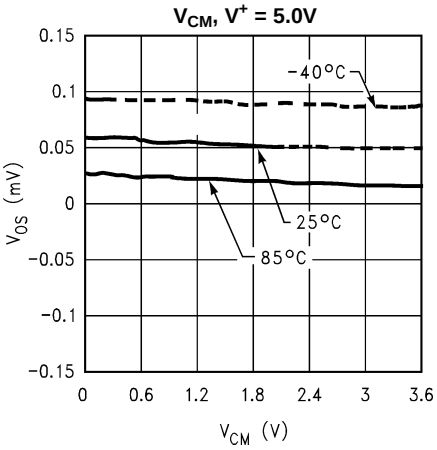


Figure 6.

Source Current vs. Out, V^+ = 2.7V

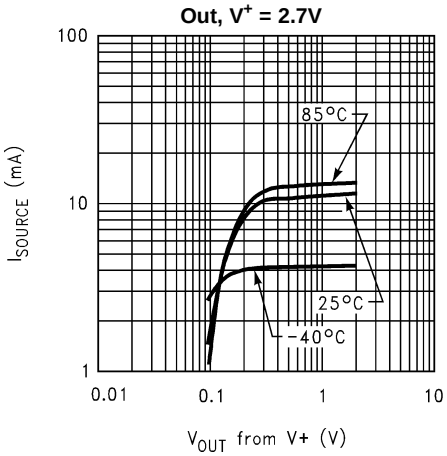


Figure 7.

Source Current vs. V_{OUT}, V^+ = 5.0V

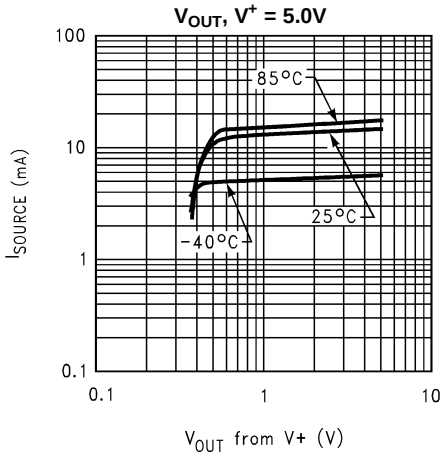


Figure 8.

Gain/Phase

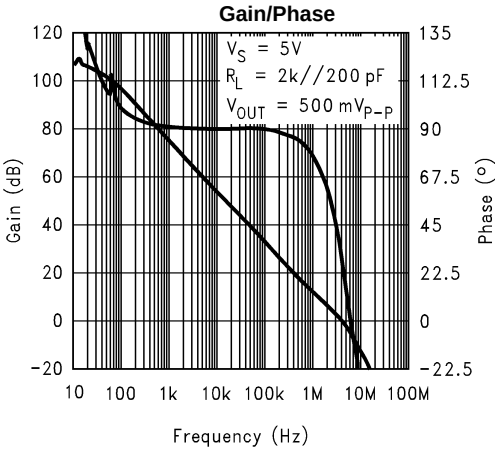


Figure 9.

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Sinking Current vs. V_{OUT}, V^+ = 2.7V

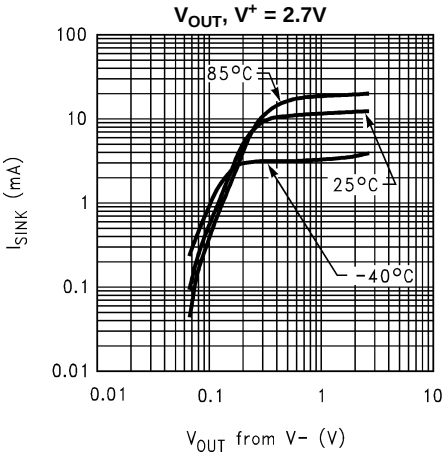


Figure 10.

Sinking Current vs. V_{OUT}, V^+ = 5.0V

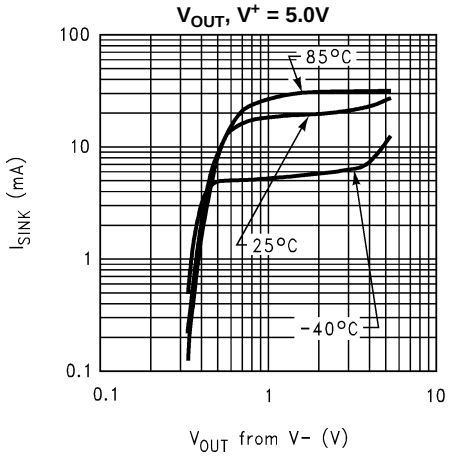


Figure 11.

V_{OS} vs. V^+

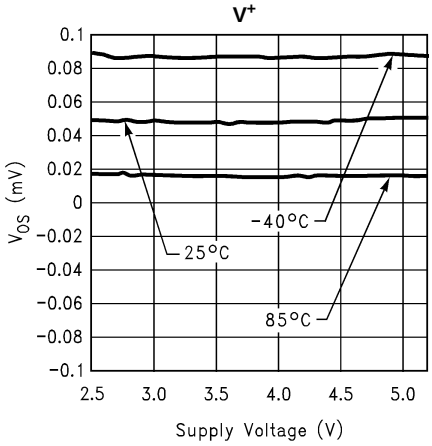


Figure 12.

V_{IN} vs. V_{OUT}, V^+ = 2.7V, R_L = 2k

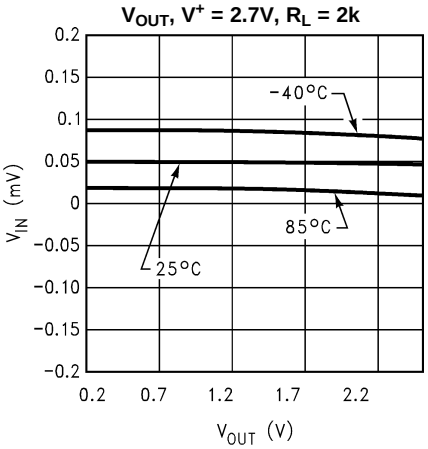


Figure 13.

V_{IN} vs. V_{OUT}, V^+ = 5.0V, R_L = 2k

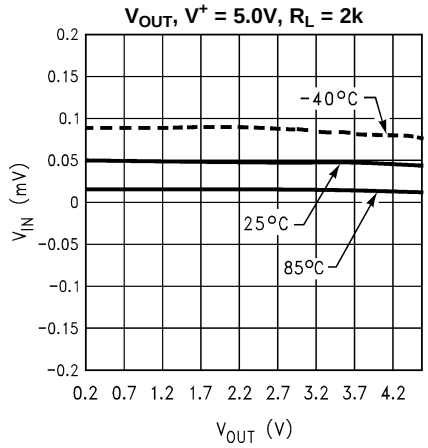


Figure 14.

Input Bias vs. V_{CM}, T_A = 25°C

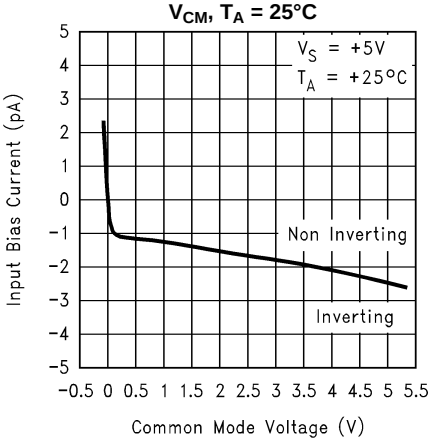


Figure 15.

Copyright © 1999–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Input Bias vs. V_{CM}, T_A = 85°C

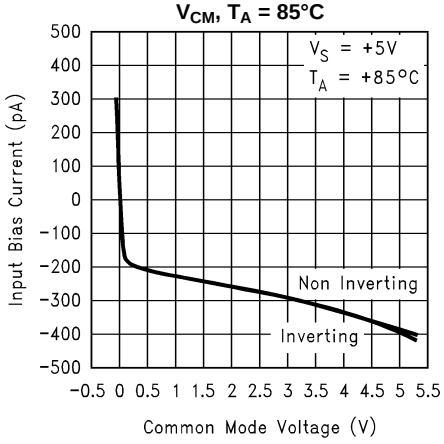


Figure 16.

PSRR +

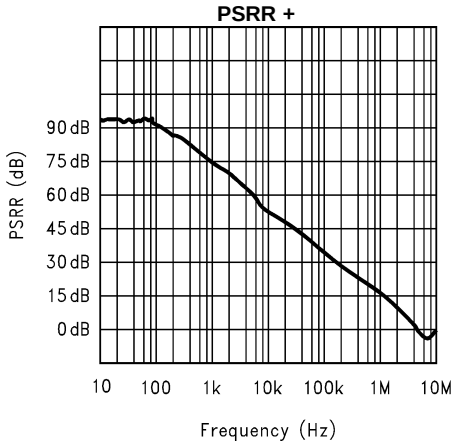


Figure 17.

PSRR −

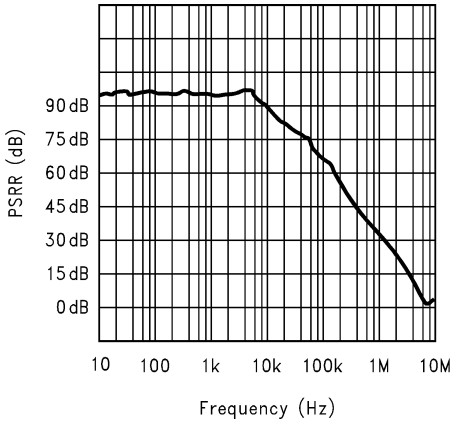


Figure 18.

Voltage Noise

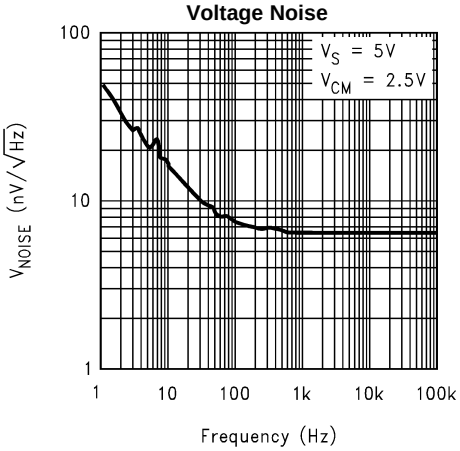


Figure 19.

CMRR

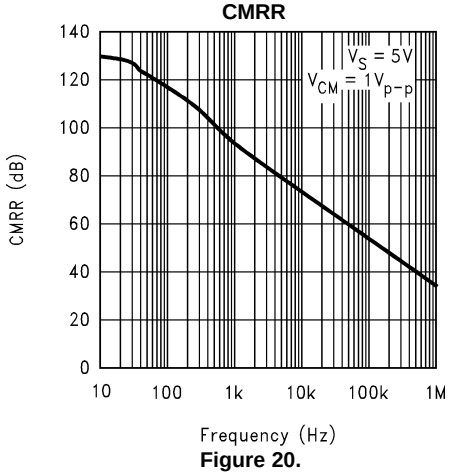


Figure 20.

APPLICATION HINTS

Noise

There are many sources of noise in a system: thermal noise, shot noise, 1/f, popcorn noise, resistor noise, just to name a few. In addition to starting with a low noise op amp, such as the LMV751, careful attention to detail will result in the lowest overall noise for the system.

To invert or not invert?

Both inverting and non-inverting amplifiers employ feedback to stabilize the closed loop gain of the block being designed. The loop gain (in decibels) equals the algebraic difference between the open loop and closed loop gains. Feedback improves the Total Harmonic Distortion (THD) and the output impedance. The various noise sources, when input referred, are amplified, not by the closed loop gain, but by the noise gain. For a non-inverting amplifier, the noise gain is equal to the closed loop gain, but for an inverting amplifier, the noise gain is equal to the closed loop gain plus one. For large gains, e.g., 100, the difference is negligible, but for small gains, such as one, the noise gain for the inverting amplifier would be two. This implies that non-inverting blocks are preferred at low gains.

Source impedance

Because noise sources are uncorrelated, the system noise is calculated by taking the RMS sum of the various noise sources, that is, the square root of the sum of the squares. At very low source impedances, the voltage noise will dominate; at very high source impedances, the input noise current times the equivalent external resistance will dominate. For a detailed example calculation, refer to Note 1.

Bias current compensation resistor

In CMOS input op amps, the input bias currents are very low, so there is no need to use R_{COMP} (see Figure 21 and Figure 22) for bias current compensation that would normally be used with early generation bipolar op amps. In fact, inclusion of the resistor would act as another thermal noise source in the system, increasing the overall noise.

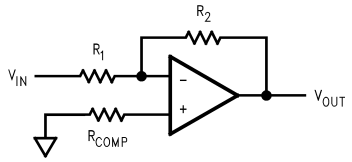


Figure 21. Bias Current Compensation Resistor

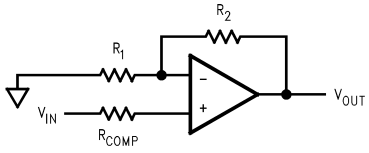


Figure 22. Bias Current Compensation Resistor

Resistor types

Thermal noise is generated by any passive resistive element. This noise is "white"; meaning it has a constant spectral density. Thermal noise can be represented by a mean-square voltage generator e_R^2 in series with a noiseless resistor, where e_R^2 is given by: Where:

$e_R^2 = 4K\ TRB\ (volts)^2$

where

- T = temperature in °K
- R = resistor value in ohms
- B = noise bandwidth in Hz
- K = Boltzmann's constant (1.38 x 10-23 W-sec/°K) (1)

Copyright © 1999–2013, Texas Instruments Incorporated

Actual resistor noise measurements may have more noise than the calculated value. This additional noise component is known as excess noise. Excess noise has a 1/f spectral response, and is proportional to the voltage drop across the resistor. It is convenient to define a noise index when referring to excess noise in resistors. The noise index is the RMS value in uV of noise in the resistor per volt of DC drop across the resistor in a decade of frequency. Noise index expressed in dB is:

$NI = 20 \log ((E_{EX}/V_{DC}) \times 10^6)$ db

where

- E_{EX} = resistor excess noise in uV per frequency decade
- V_{DC} = DC voltage drop across the resistor (2)

Excess noise in carbon composition resistors corresponds to a large noise index of +10 dB to -20 dB. Carbon film resistors have a noise index of -10 dB to -25 dB. Metal film and wire wound resistors show the least amount of excess noise, with a noise index figure of -15 dB to -40 dB.

Other noise sources:

As the op amp and resistor noise sources are decreased, other noise contributors will now be noticeable. Small air currents across thermocouples will result in low frequency variations. Any two dissimilar metals, such as the lead on the IC and the solder and copper foil of the pc board, will form a thermocouple. The source itself may also generate noise. An example would be a resistive bridge. All resistive sources generate thermal noise based on the same equation listed above under "resistor types". (2)

Putting it all together

To a first approximation, the total input referred noise of an op amp is:

$E_t^2 = e_n^2 + e_{req}^2 + (i_n * Req)^2$

where

- Req is the equivalent source resistance at the inputs (3)

At low impedances, voltage noise dominates. At high impedances, current noise dominates. With a typical noise current on most CMOS input op amps of 0.01 pA/$\sqrt{Hz}$, the current noise contribution will be smaller than the voltage noise for Req less than one megohm.

Other Considerations

Comparator operation

Occasionally operational amplifiers are used as comparators. This is not optimum for the LMV751 for several reasons. First, the LMV751 is compensated for unity gain stability, so the speed will be less than could be obtained on the same process with a circuit specifically designed for comparator operation. Second, op amp output stages are designed to be linear, and will not necessarily meet the logic levels required under all conditions. Lastly, the LMV751 has the newer PNP-NPN common emitter output stage, characteristic of many rail-to-rail output op amps. This means that when used in open loop applications, such as comparators, with very light loads, the output PNP will saturate, with the output current being diverted into the previous stage. As a result, the supply current will increase to the 20-30 mA. range. When used as a comparator, a resistive load between 2kΩ and 10kΩ should be used with a small amount of hysteresis to alleviate this problem. When used as an op amp, the closed loop gain will drive the inverting input to within a few millivolts of the non-inverting input. This will automatically reduce the output drive as the output settles to the correct value; thus it is only when used as a comparator that the current will increase to the tens of milliampere range.

Rail-to-Rail

Because of the output stage discussed above, the LMV751 will swing “rail-to-rail” on the output. This normally means within a few hundred millivolts of each rail with a reasonable load. Referring to the Electrical Characteristics table for 2.7V to 5.0V, it can be seen that this is true for resistive loads of 2kΩ and 10kΩ. The input stage consists of cascoded P-channel MOSFETS, so the input common mode range includes ground, but typically requires 1.2V to 1.3V headroom from the positive rail. This is better than the industry standard LM324 and LM358 that have PNP input stages, and the LMV751 has the advantage of much lower input bias currents.

Copyright © 1999–2013, Texas Instruments Incorporated

Loading

The LMV751 is a low noise, high speed op amp with excellent phase margin and stability. Capacitive loads up to 1000 pF can be handled, but larger capacitive loads should be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

General Circuits

With the low noise and low input bias current, the LMV751 would be useful in active filters, integrators, current to voltage converters, low frequency sine wave generators, and instrumentation amplifiers. (3)

NOTE

1. Sherwin, Jim “Noise Specs Confusing?” AN-104 (SNVA515), Texas Instruments.
2. Christensen, John, “Noise-figure curve ease the selection of low-noise op amps”, EDN, pp 81-84, Aug. 4, 1994.
3. “Op Amp Circuit Collection”, AN-31 (SNLA140), Texas Instruments.

Copyright © 1999–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

Copyright © 1999–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV751M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A32A	
LMV751M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A32A	Samples
LMV751M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A32A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

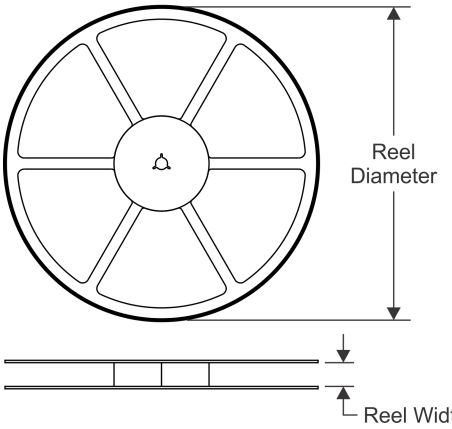
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

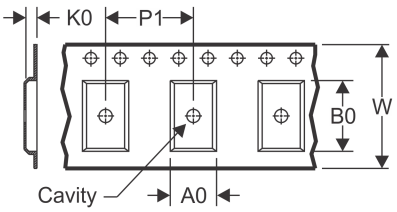
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

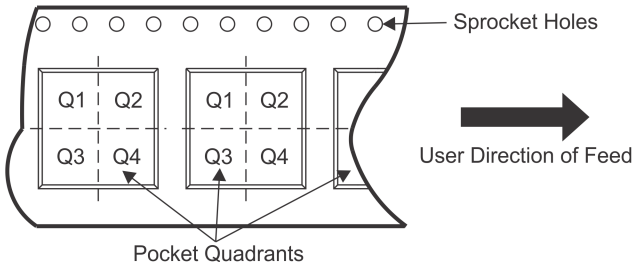


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

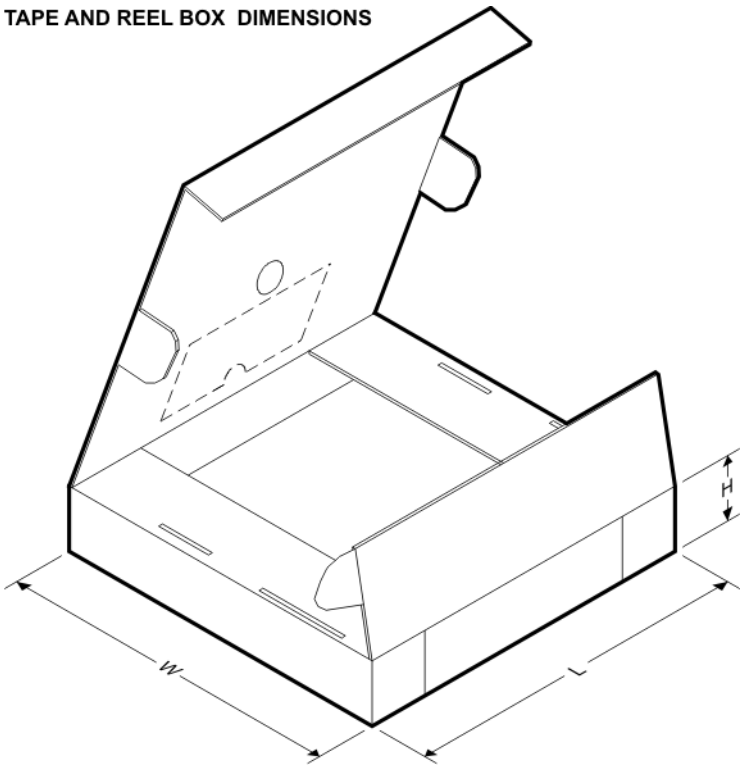
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV751M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV751M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV751M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

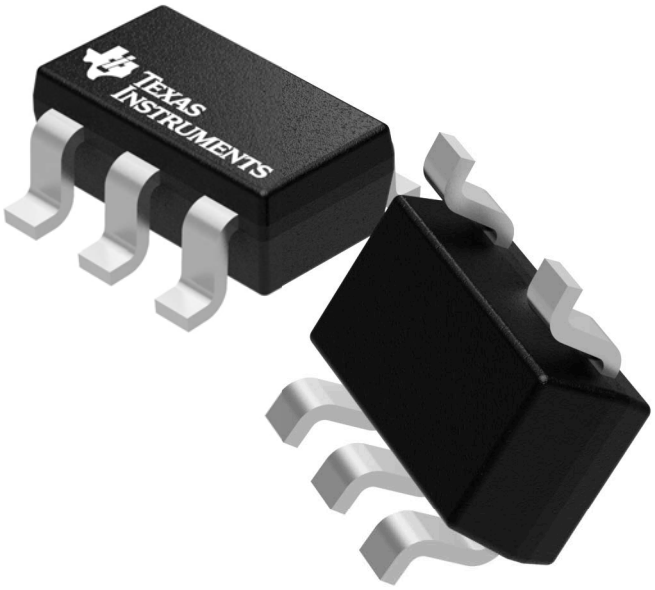


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV751M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV751M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV751M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated