LPV811/LPV812 Precision 425 nA Nanopower Operational Amplifiers

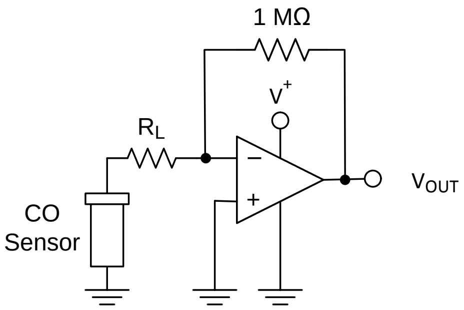
1 Features

- Nanopower Supply Current: 425 nA/channel
- Offset Voltage: 300 µV (max)
- TcVos: 1 µV/°C
- Gain-Bandwidth: 8 kHz
- Unity-Gain Stable
- Low Input Bias Current : 100 fA
- Wide Supply Range: 1.6 V to 5.5 V
- Rail-to-Rail Output
- No Output Reversals
- EMI Protection
- Temperature Range: –40°C to 125°C
- Industry Standard Packages:
  - Single in 5-pin SOT-23
  - Dual in 8-pin VSSOP

2 Applications

- CO and O_2 Gas Detectors (TIDA-0756)
- PIR Motion Detectors
- Current Sensing
- Thermostats
- IoT Remote Sensors
- Active RFID Readers and Tags
- Portable Medical Equipment

Figure 1. Nanopower CO Sensor



3 Description

The LPV811 (single) and LPV812 (dual) are a ultra-low-power precision operational amplifier family for “Always ON” sensing applications in battery powered wireless and low power wired equipment. With 8 kHz of bandwidth from 425 nA of quiescent current and a trimmed offset voltage to under 300µV, the LPV81x amplifiers provide the required precision while minimizing power consumption in equipment such as gas detectors and portable electronic devices where operational battery-life is critical.

In addition to being ultra-low-power, the LPV81x amplifiers have CMOS input stages with fempto-amp bias currents for impedance source applications. The LPV81x amplifiers also feature a negative-rail sensing input stage and a rail-to-rail output stage that swings within millivolts of the rails, maintaining the widest dynamic range possible. EMI protection is designed into the LPV81x in order to reduce system sensitivity to unwanted RF signals from mobile phones, WiFi, radio transmitters, and tag readers.

Device Information(1)

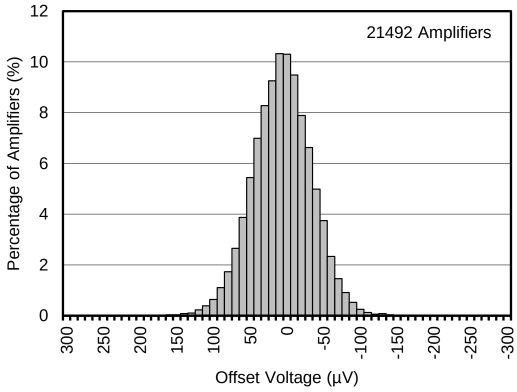
PART NUMBER	PACKAGE	BODY SIZE
LPV811	SOT-23 (5)	2.90 mm x 1.60 mm
LPV812	VSSOP (8)	3.00 mm × 3.00 mm

LPV8xx Family of Nanopower Amplifiers

PART NUMBER	CHANNELS	SUPPLY CURRENT (Typ/Ch)	OFFSET VOLTAGE (Max)
LPV801	1	500 nA	3.5 mV
LPV802	2	320 nA	3.5 mV
LPV811	1	450 nA	370 µV
LPV812	2	425 nA	300 µV

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Figure 2. LPV812 Offset Voltage Distribution



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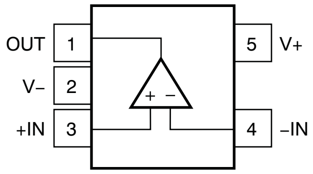
4 Revision History

Changes from Revision A (October 2016) to Revision B	Page
• Added family upsell table to front page	1
• Changed Front page O2 Sens circuit to Vos Disty Graph	1
• Deleted larger family upsell table	2
• Deleted LPV811 preview "preliminary spec" table note.	5
• Added separate LPV811 CMRR Specification.	5
• Added offset distribution graphs	6

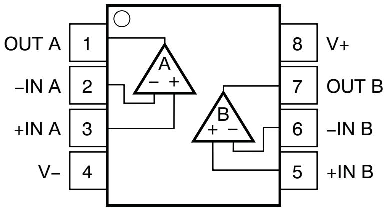
Changes from Original (August 2016) to Revision A	Page
• Changed Product Preview to Production Data.	1

5 Pin Configuration and Functions

LPV811 5-Pin SOT-23
DBV Package
Top View



LPV812 8-Pin VSSOP
DGK Package
Top View



Pin Functions: LPV811 DBV

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Output
-IN	4	I	Inverting Input
+IN	3	I	Non-Inverting Input
V-	2	P	Negative (lowest) power supply
V+	5	P	Positive (highest) power supply

Pin Functions: LPV812 DGK

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_s = (V+) - (V-)			–0.3	6	V
Input pins	Voltage (2) (3)	Common mode	(V-) - 0.3	(V+) + 0.3	V
		Differential	(V-) - 0.3	(V+) + 0.3	V
Input pins	Current		-10	10	mA
Output short current (4)			Continuous	Continuous	
Storage temperature, T_{stg}			–65	150	°C
Junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not to exceed -0.3V or +6.0V on ANY pin, referred to V-
(3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(4) Short-circuit to Vs/2, one amplifier per package. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage (V+ – V–)	1.6	5.5	V
Specified temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LPV811 DBV (SOT-23) 5 PINS	LPV812 DGK (VSSOP) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	177.4	177.6	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	133.9	68.8	
θ_{JB}	Junction-to-board thermal resistance	36.3	98.2	
ψ_{JT}	Junction-to-top characterization parameter	23.6	12.3	
ψ_{JB}	Junction-to-board characterization parameter	35.7	96.7	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

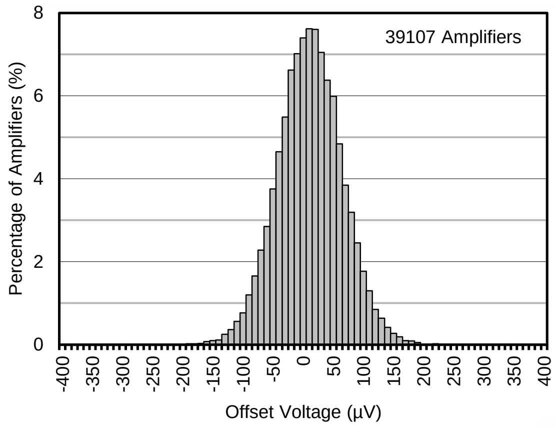
6.5 Electrical Characteristics

T_A = 25°C, V_S = 1.8 V to 5 V, V_{CM} = V_{OUT} = V_S/2, and R_L≥ 10 MΩ to V_S / 2, unless otherwise noted .

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage, LPV811	V_S = 1.8V and 3.3V, V_{CM} = V-			±60	±370	µV
	Input offset voltage, LPV812	V_S = 1.8V and 3.3V, V_{CM} = V-			±55	±300	µV
$\Delta V_{OS}/\Delta T$	Input offset drift	V_{CM} = V-	T_A = –40°C to 125°C		±1		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8V to 3.3V, V_{CM} = V-			±1.6	±60	µV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	V_S = 3.3V		0		2.4	V
CMRR	Common-mode rejection ratio, LPV811	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S = 3.3V		77	95		dB
	Common-mode rejection ratio, LPV812	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S = 3.3V		80	98		dB
INPUT BIAS CURRENT							
I_B	Input bias current	V_S = 1.8V			±100		fA
I_{OS}	Input offset current	V_S = 1.8V			±100		fA
INPUT IMPEDANCE							
	Differential				7		pF
	Common mode				3		pF
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			6.5		µVp-p
e_n	Input voltage noise density	f = 100 Hz			340		nV/√Hz
		f = 1 kHz			420		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V ≤ V_O ≤ (V+) – 0.3 V, R_L = 100 kΩ			120		dB
OUTPUT							
V_{OH}	Voltage output swing from positive rail	V_S = 1.8V, R_L = 100 kΩ to $V^+/2$		10	3.5		mV
V_{OL}	Voltage output swing from negative rail	V_S = 1.8V, R_L = 100 kΩ to $V^+/2$			2.5	10	
I_{SC}	Short-circuit current	V_S = 3.3V, Short to V_S/2			4.7		mA
Z_O	Open loop output impedance	f = 1 KHz, I_O = 0 A			90		kΩ
FREQUENCY RESPONSE							
GBP	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ, V_S = 5V			8		kHz
SR	Slew rate (10% to 90%)	G = 1, Rising Edge, C_L = 20 pF, V_S = 5V			2		V/ms
		G = 1, Falling Edge, C_L = 20 pF, V_S = 5V			2.1		
POWER SUPPLY							
I_Q	Quiescent Current, LPV811	V_{CM} = V-, I_O = 0, V_S = 3.3V			450	540	nA
	Quiescent Current, Per Channel, LPV812	V_{CM} = V-, I_O = 0, V_S = 3.3V			425	495	

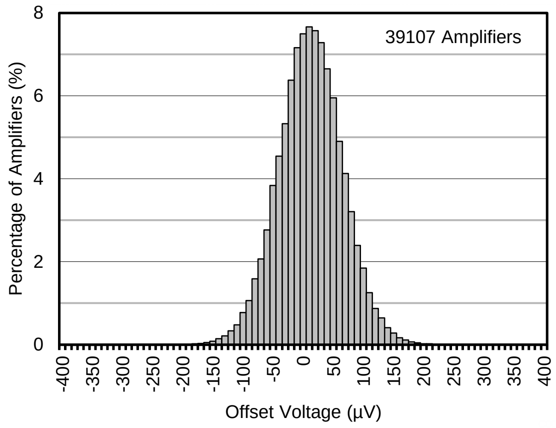
6.6 Typical Characteristics

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



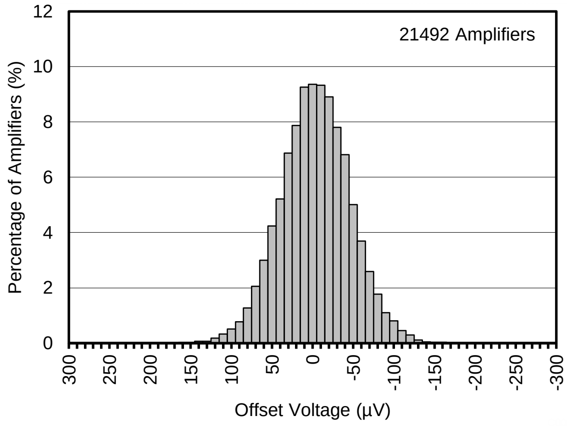
V_S = 1.8V LPV811
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 3. Offset Distribution of LPV811



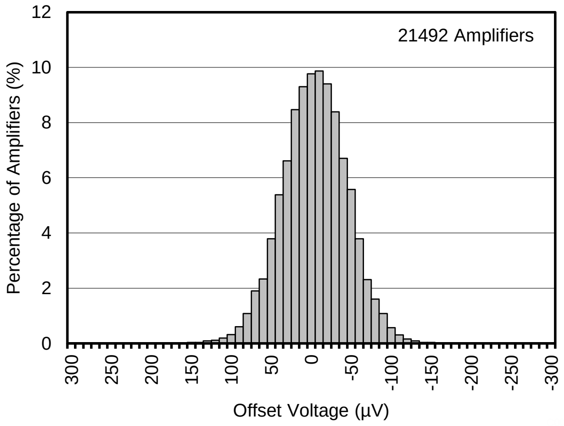
V_S = 3.3V LPV811
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 4. Offset Distribution of LPV811



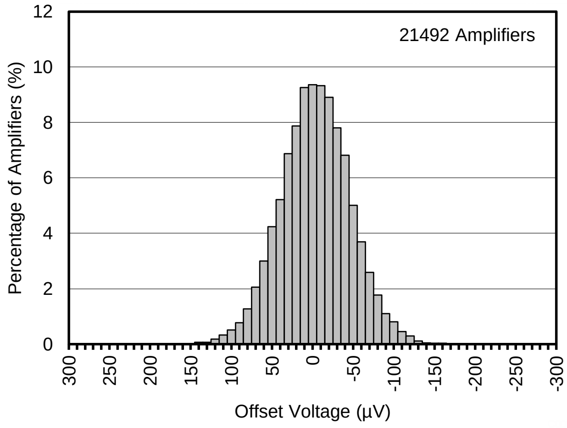
V_S = 1.8V LPV812, Channel A
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 5. Offset Distribution of LPV812, CH A



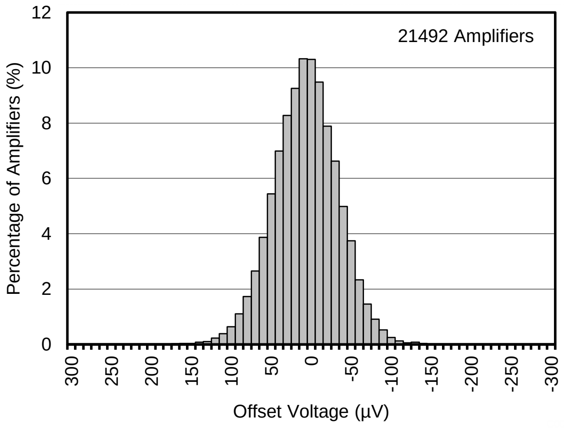
V_S = 3.3V LPV812, Channel A
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 6. Offset Distribution of LPV812, CH A



V_S =1.8V LPV812, Channel B
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 7. Offset Distribution of LPV812, CH B

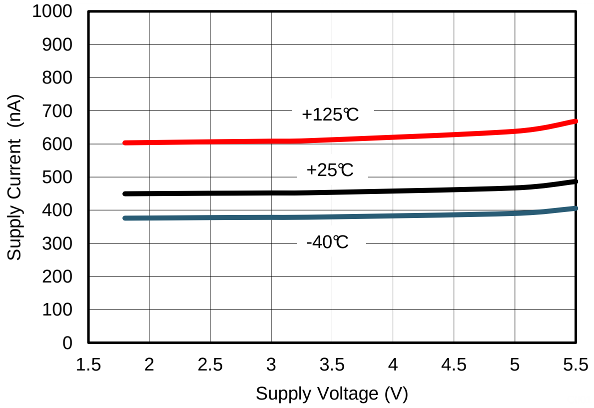


V_S = 3.3V LPV812, Channel B
T_A = 25°C V_{CM} = V- R_L=No Load

Figure 8. Offset Distribution of LPV812, CH B

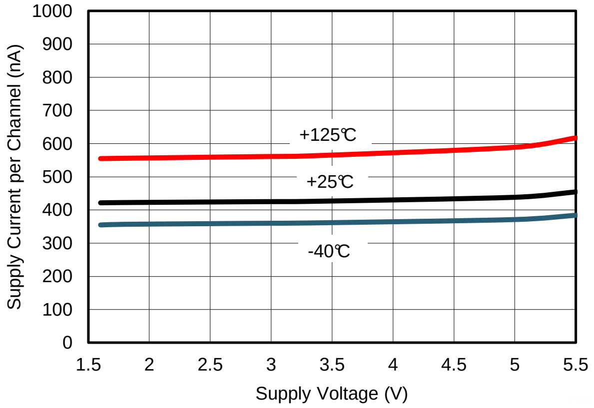
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



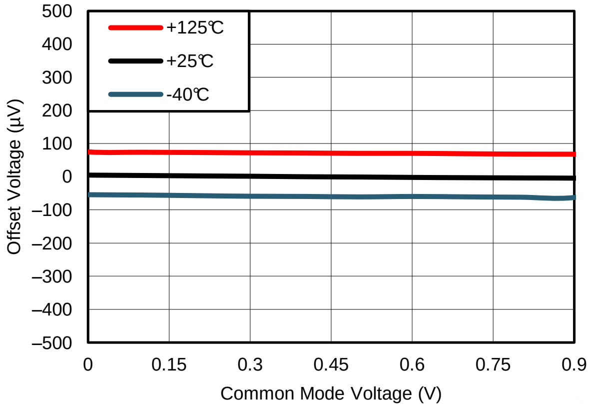
V_{CM} = V- LPV811 R_L=No Load

Figure 9. Supply Current vs. Supply Voltage, LPV811



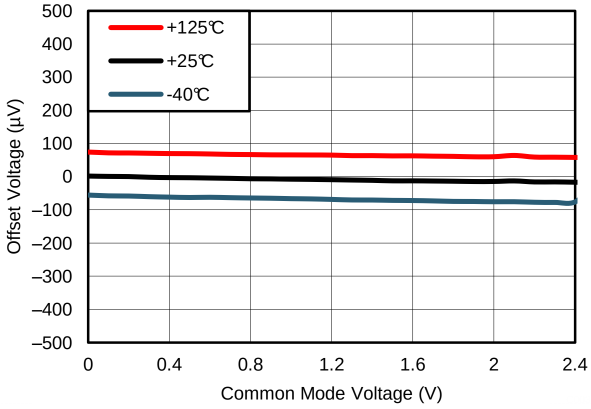
V_{CM} = V- LPV812 R_L=No Load

Figure 10. Supply Current vs. Supply Voltage, LPV812



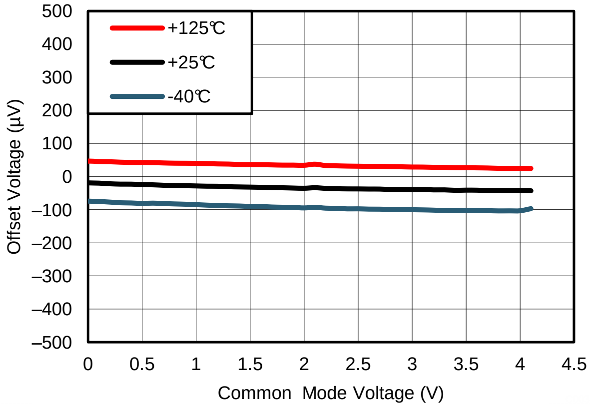
V_S= 1.8V R_L= 10MΩ

Figure 11. Typical Offset Voltage vs. Common Mode Voltage



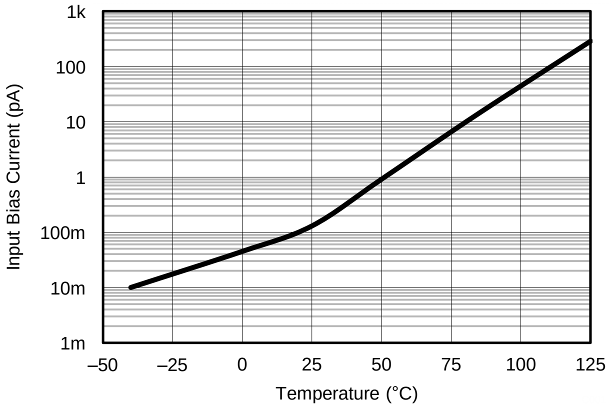
V_S= 3.3V R_L= 10MΩ

Figure 12. Typical Offset Voltage vs. Common Mode Voltage



V_S= 5V R_L= 10MΩ

Figure 13. Typical Offset Voltage vs. Common Mode Voltage



V_S= 5V T_A = -40 to 125 V_{CM} = Vs/2

Figure 14. Input Bias Current vs. Temperature

Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.

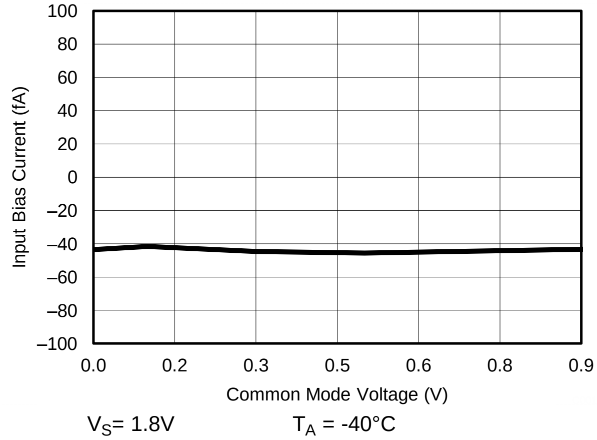


Figure 15. Input Bias Current vs. Common Mode Voltage

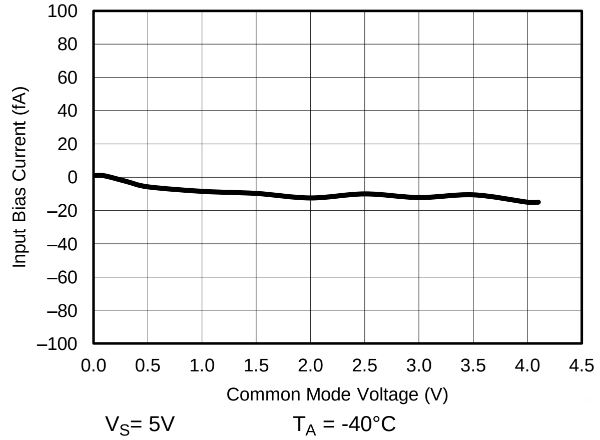


Figure 16. Input Bias Current vs. Common Mode Voltage

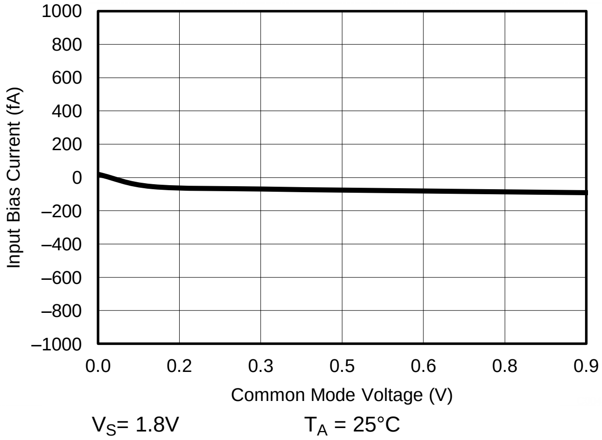


Figure 17. Input Bias Current vs. Common Mode Voltage

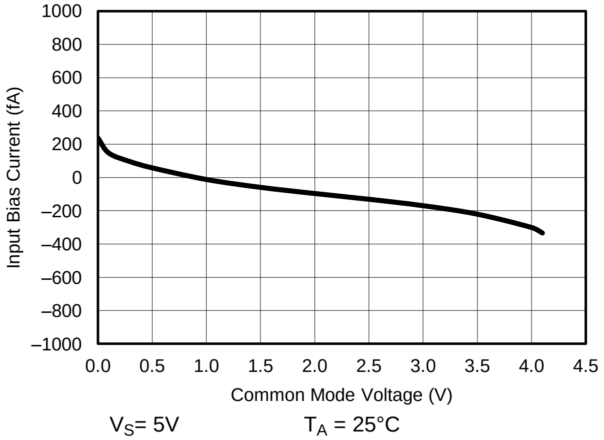


Figure 18. Input Bias Current vs. Common Mode Voltage

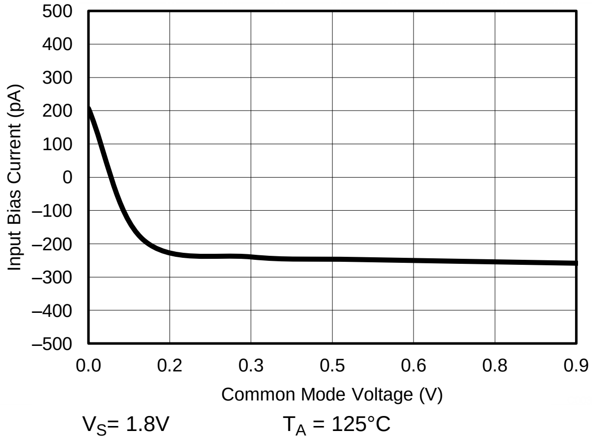


Figure 19. Input Bias Current vs. Common Mode Voltage

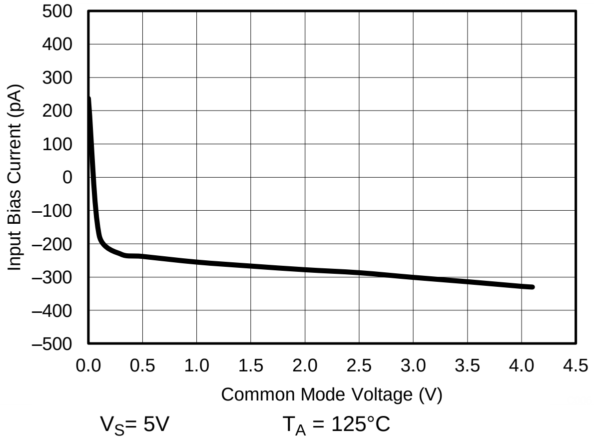
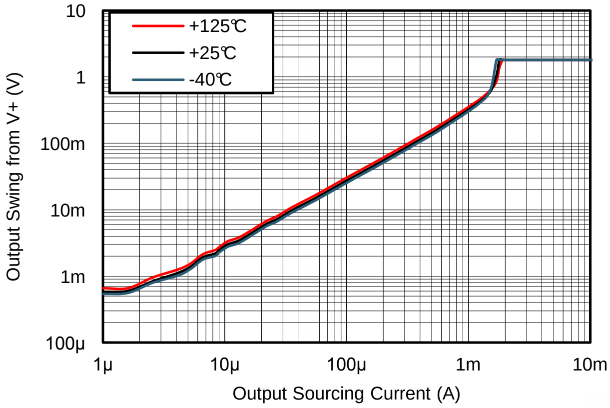


Figure 20. Input Bias Current vs. Common Mode Voltage

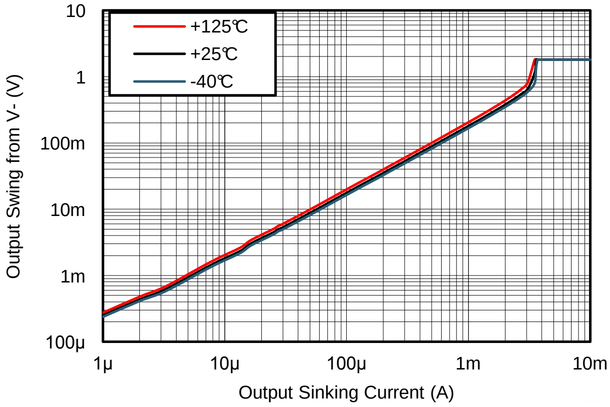
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



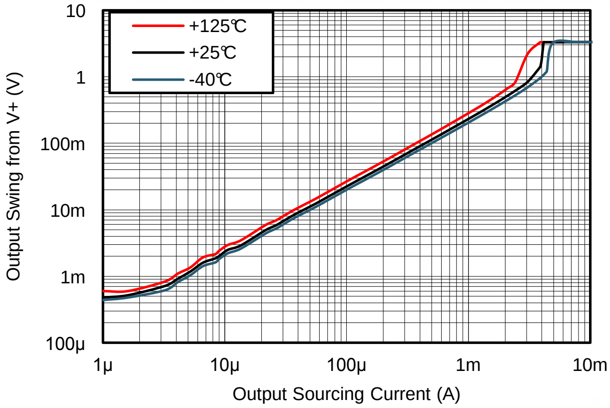
V_S= 1.8V R_L= No Load

Figure 21. Output Swing vs. Sourcing Current, 1.8V



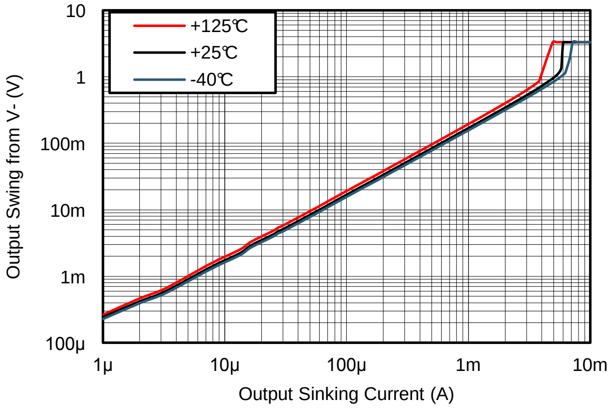
V_S= 1.8V R_L= No Load

Figure 22. Output Swing vs. Sinking Current, 1.8V



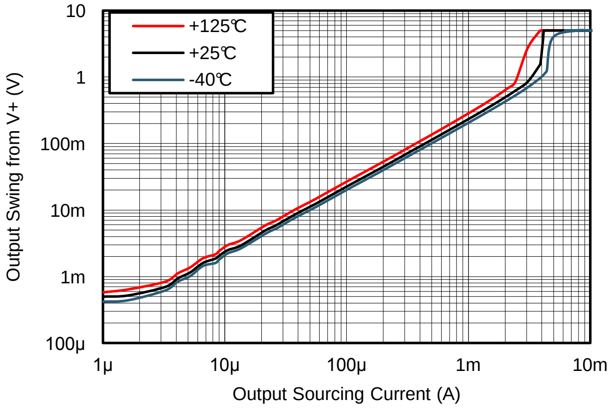
V_S= 3.3V R_L= No Load

Figure 23. Output Swing vs. Sourcing Current, 3.3V



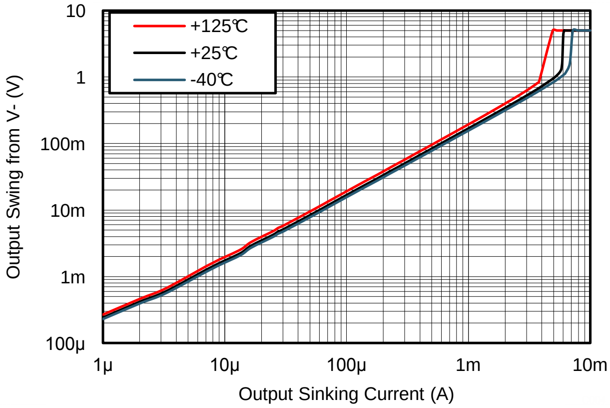
V_S= 3.3V R_L= No Load

Figure 24. Output Swing vs. Sinking Current, 3.3V



V_S= 5V R_L= No Load

Figure 25. Output Swing vs. Sourcing Current, 5V

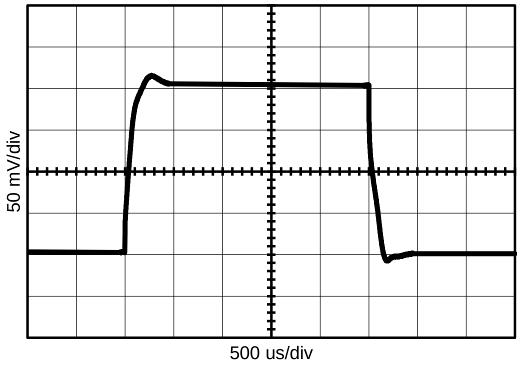


V_S= 5V R_L= No Load

Figure 26. Output Swing vs. Sinking Current, 5V

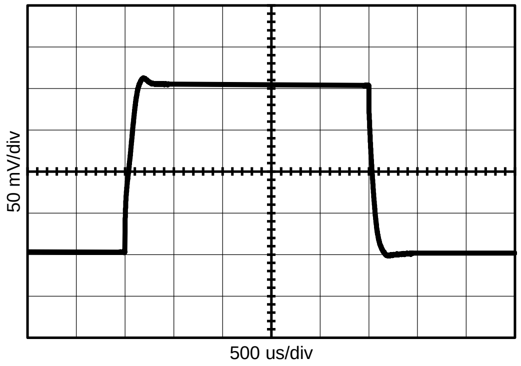
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



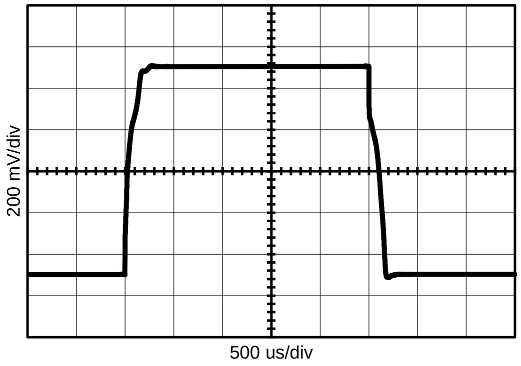
T_A = 25 R_L= 10MΩ Vout = 200mVpp
V_S= ±0.9V C_L= 20pF A_V = +1

Figure 27. Small Signal Pulse Response, 1.8V



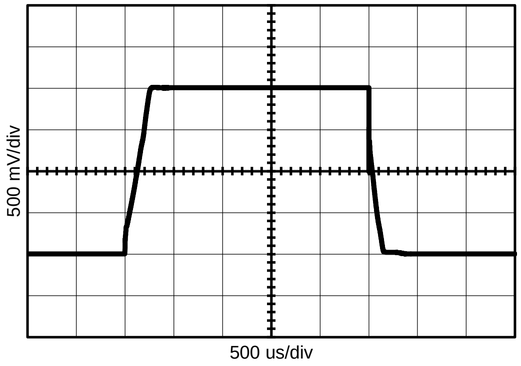
T_A = 25 R_L= 10MΩ Vout = 200mVpp
V_S= ±2.5V C_L= 20pF A_V = +1

Figure 28. Small Signal Pulse Response, 5V



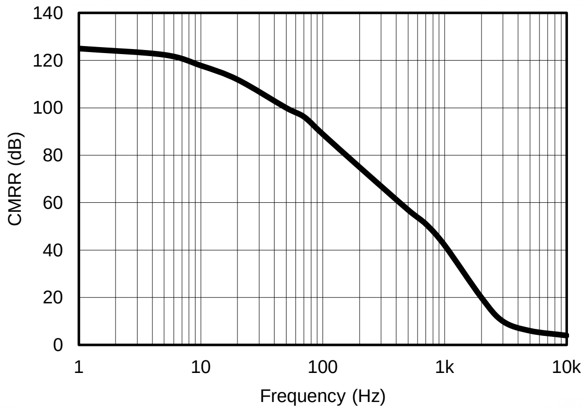
T_A = 25 R_L= 10MΩ Vout = 1Vpp
V_S= ±0.9V C_L= 20pF A_V = +1

Figure 29. Large Signal Pulse Response, 1.8V



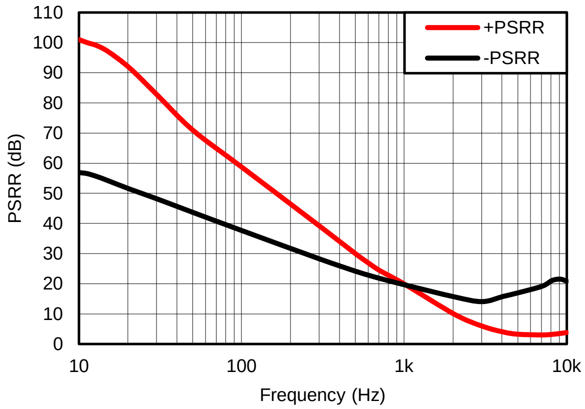
T_A = 25 R_L= 10MΩ Vout = 2Vpp
V_S= ±2.5V C_L= 20pF A_V = +1

Figure 30. Large Signal Pulse Response, 5V



T_A = 25 R_L= 10MΩ ΔV_{CM} = 0.5Vpp
V_S= 5V C_L= 20p
V_{CM} = Vs/2 A_V = +1

Figure 31. CMRR vs Frequency

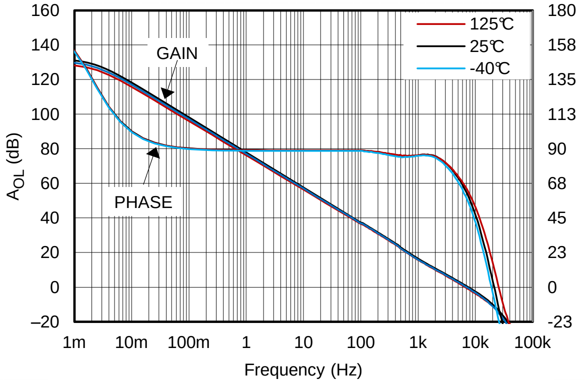


T_A = 25 R_L= 10MΩ ΔV_S = 0.5Vpp
V_S= 3.3V C_L= 20p
V_{CM} = Vs/2 A_V = +1

Figure 32. ±PSRR vs Frequency

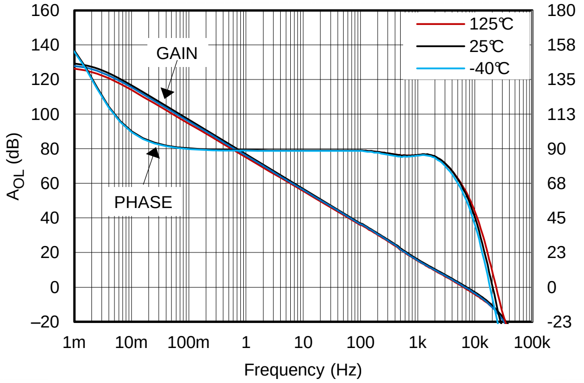
Typical Characteristics (continued)

at T_A = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



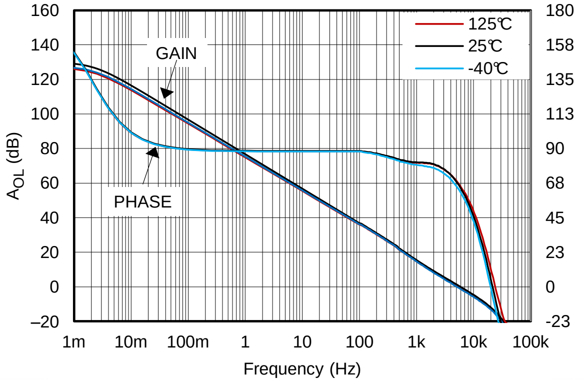
T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV$_{PP}$
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 33. Open Loop Gain and Phase, 5V, 10 MΩ Load



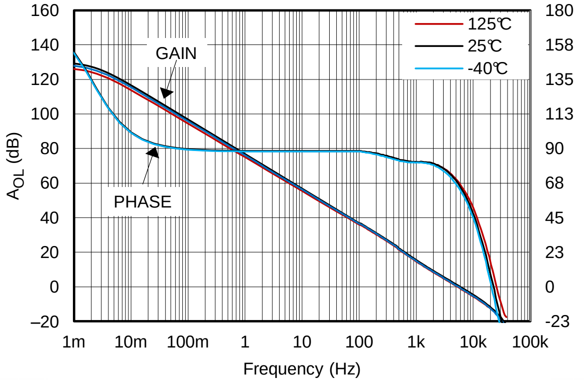
T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV$_{PP}$
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 34. Open Loop Gain and Phase, 3.3V, 10 MΩ Load



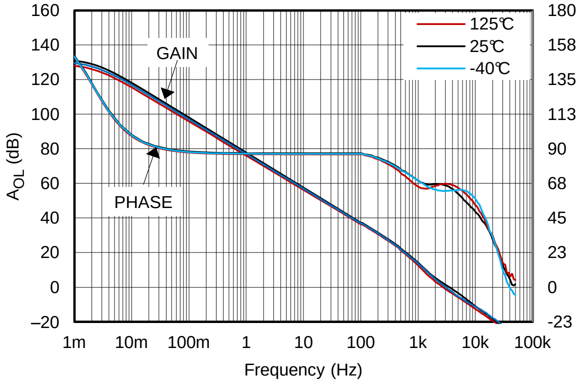
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV$_{PP}$
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 35. Open Loop Gain and Phase, 5V, 1 MΩ Load



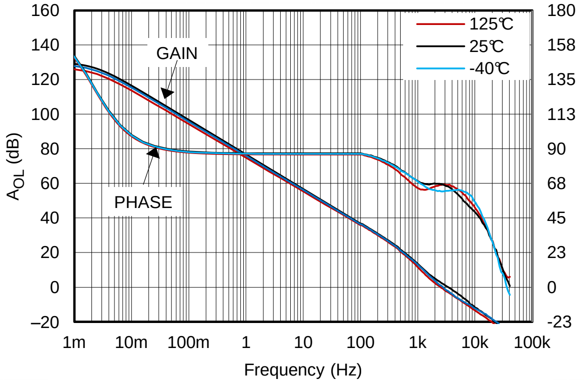
T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV$_{PP}$
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 36. Open Loop Gain and Phase, 3.3V, 1 MΩ Load



T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV$_{PP}$
V_S= 5V C_L= 20pF V_{CM} = Vs/2

Figure 37. Open Loop Gain and Phase, 5V, 100kΩ Load

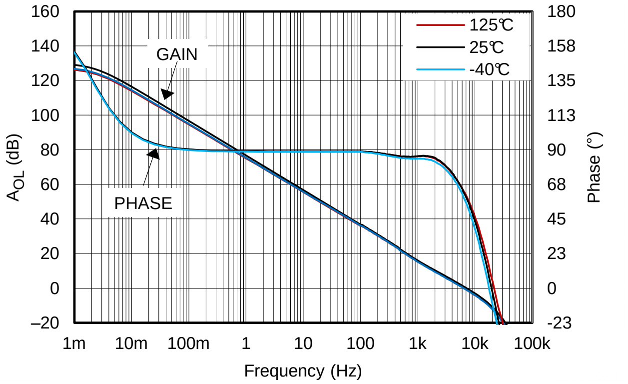


T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV$_{PP}$
V_S= 3.3V C_L= 20pF V_{CM} = Vs/2

Figure 38. Open Loop Gain and Phase, 3.3V, 100kΩ Load

Typical Characteristics (continued)

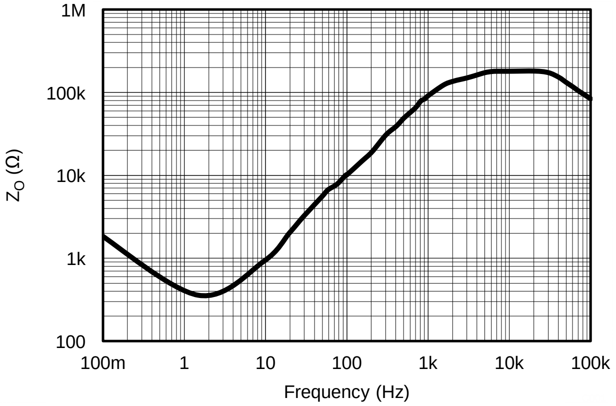
at T_A = 25°C, R_L = 10MΩ to $V_S/2$,C_L = 20pF, V_{CM} = V_S / 2V unless otherwise specified.



T_A = -40, 25, 125°C R_L= 10MΩ V_{OUT} = 200mV_{PP}

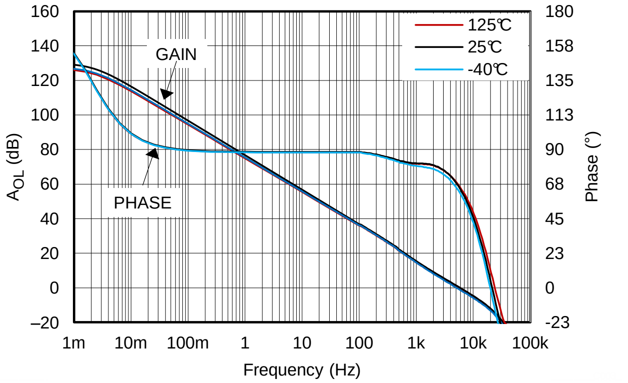
V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 39. Open Loop Gain and Phase, 1.8V, 10 MΩ Load



T_A = 25°C V_S= 5 V R_L= 10MΩ

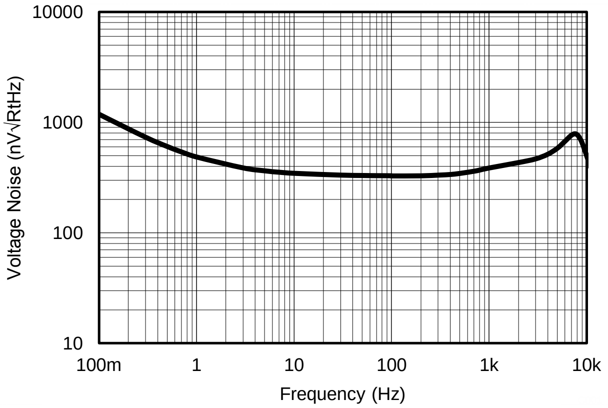
Figure 40. Open Loop Output Impedance



T_A = -40, 25, 125°C R_L= 1MΩ V_{OUT} = 200mV_{PP}

V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

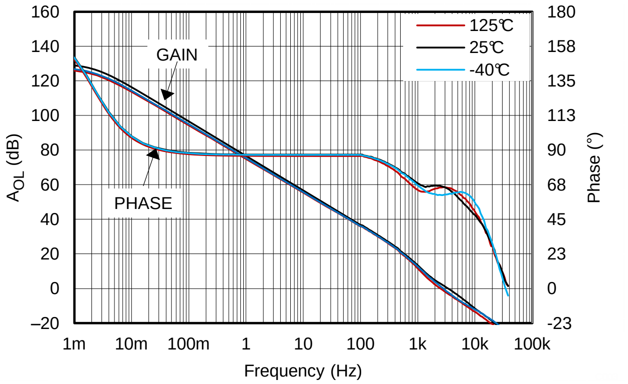
Figure 41. Open Loop Gain and Phase, 1.8V, 1 MΩ Load



T_A = 25 R_L= 1MΩ V_{CM} = Vs/2

V_S= 5V C_L= 20pF A_V = +1

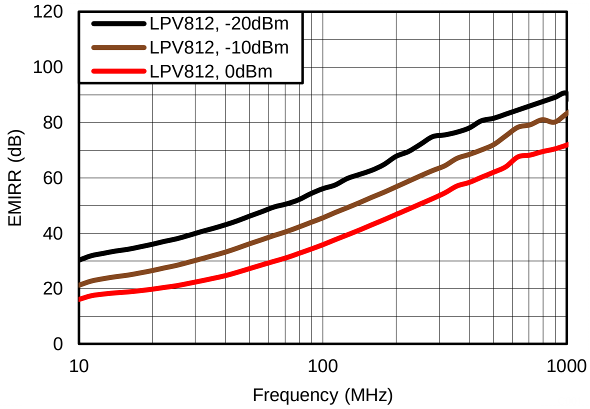
Figure 42. Input Voltage Noise vs Frequency



T_A = -40, 25, 125°C R_L= 100kΩ V_{OUT} = 200mV_{PP}

V_S= 1.8V C_L= 20pF V_{CM} = Vs/2

Figure 43. Open Loop Gain and Phase, 1.8V, 100kΩ Load



T_A = 25 R_L= 1MΩ V_{CM} = Vs/2

V_S= 3.3V C_L= 20pF A_V = +1

Figure 44. EMIRR Performance

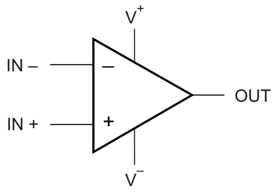
7 Detailed Description

7.1 Overview

The LPV811 (single) and LPV812 (dual) series of nanoPower CMOS operational amplifiers are designed for long-life battery-powered and energy harvested applications. They operate on a single supply with operation as low as 1.6V. The Input Offset is trimmed to less than 300uV and the output is rail-to-rail and swings to within 3.5mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply making it ideal for single-supply applications. EMI protection has been employed internally to reduce the effects of EMI.

Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

7.2 Functional Block Diagram



7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 120 dB (1,000,000x, or 1,000,000 Volts per microvolt). (1)

7.4 Device Functional Modes

7.4.1 Negative-Rail Sensing Input

The input common-mode voltage range of the LPV81x extends from (V-) to (V+) – 0.9 V. In this range, low offset can be expected with a minimum of 77dB CMRR. The LPV81x is protected from output "inversions" or "reversals".

7.4.2 Rail to Rail Output Stage

The LPV81x output voltage swings 3.5 mV from rails at 1.8 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV81x Maximum Output Voltage Swing graph defines the maximum swing possible under a particular output load.

7.4.3 Design Optimization for Nanopower Operation

When designing for ultra-low power, choose system feedback components carefully. To minimize quiescent current consumption, select large-value feedback resistors. Any large resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electrolytics may have large static leakage currents in the nanoamps.

Device Functional Modes (continued)

7.4.4 Driving Capacitive Load

The LPV81x is internally compensated for stable unity gain operation, with a 8 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (>50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 45. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive. The recommended value for R_{ISO} is 30-50kΩ.

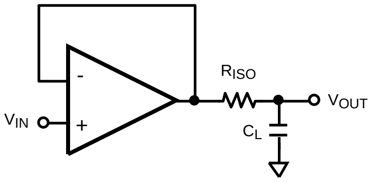


Figure 45. Resistive Isolation Of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV81x is a ultra-low power operational amplifier that provides 8 kHz bandwidth with only 425nA typical quiescent current, trimmed input offset voltage and precision drift specifications. These rail-to-rail output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the negative supply rail and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

8.2 Typical Application: Three Terminal CO Gas Sensor Amplifier

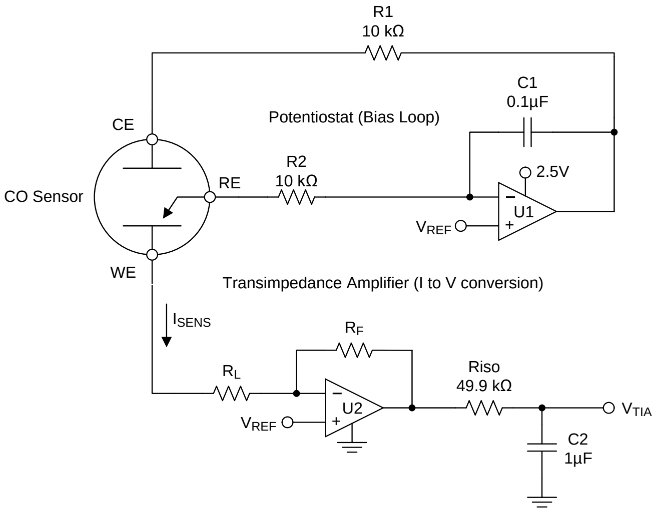


Figure 46. Three Terminal Gas Sensor Amplifier Schematic

8.2.1 Design Requirements

Figure 46 shows a simple micropower potentiostat circuit for use with three terminal unbiased CO sensors, though it is applicable to many other type of three terminal gas sensors or electrochemical cells.

The basic sensor has three electrodes; The Sense or Working Electrode ("WE"), Counter Electrode ("CE") and Reference Electrode ("RE"). A current flows between the CE and WE proportional to the detected concentration.

The RE monitors the potential of the internal reference point. For an unbiased sensor, the WE and RE electrodes must be maintained at the same potential by adjusting the bias on CE. Through the Potentiostat circuit formed by U1, the servo feedback action will maintain the RE pin at a potential set by V_{REF}.

R1 is to maintain stability due to the large capacitance of the sensor. C1 and R2 form the Potentiostat integrator and set the feedback time constant.

U2 forms a transimpedance amplifier ("TIA") to convert the resulting sensor current into a proportional voltage. The transimpedance gain, and resulting sensitivity, is set by R_F according to Equation 2.

$$V_{TIA} = (-I * R_F) + V_{REF} \tag{2}$$

R_L is a load resistor of which the value is normally specified by the sensor manufacturer (typically 10 ohms). The potential at WE is set by the applied $V_{REF.}$ Riso provides capacitive isolation and, combined with C2, form the output filter and ADC reservoir capacitor to drive the ADC.

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.2 Detailed Design Procedure

For this example, we will be using a CO sensor with a sensitivity of 69nA/ppm. The supply voltage and maximum ADC input voltage is 2.5V, and the maximum concentration is 300ppm.

First the V_{REF} voltage must be determined. This voltage is a compromise between maximum headroom and resolution, as well as allowance for "footroom" for the minimum swing on the CE terminal, since the CE terminal generally goes negative in relation to the RE potential as the concentration (sensor current) increases. Bench measurements found the difference between CE and RE to be 180mV at 300ppm for this particular sensor.

To allow for negative CE swing "footroom" and voltage drop across the 10k resistor, 300mV was chosen for V_{REF}.

Therefore +300mV will be used as the minimum V_{ZERO} to add some headroom.

$V_{ZERO} = V_{REF} = +300mV$

where

- V_{ZERO} is the zero concentration voltage
- V_{REF} is the reference voltage (300mV) (3)

Next we calculate the maximum sensor current at highest expected concentration:

$I_{SENSMAX} = I_{PERPPM} * ppmMAX = 69nA * 300ppm = 20.7uA$

where

- $I_{SENSMAX}$ is the maximum expected sensor current
- I_{PERPPM} is the manufacturer specified sensor current in Amps per ppm
- ppmMAX is the maximum required ppm reading (4)

Now find the available output swing range above the reference voltage available for the measurement:

$V_{SWING} = V_{OUTMAX} – V_{ZERO} = 2.5V – 0.3V = 2.2V$

where

- V_{SWING} is the expected change in output voltage
- V_{OUTMAX} is the maximum amplifier output swing (usually near V+) (5)

Now we calculate the transimpedance resistor $®_F$) value using the maximum swing and the maximum sensor current:

$R_F = V_{SWING} / I_{SENSMAX} = 2.2V / 20.7µA = 106.28\ kΩ$ (we will use 110 kΩ for a common value) (6)

Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.3 Application Curve

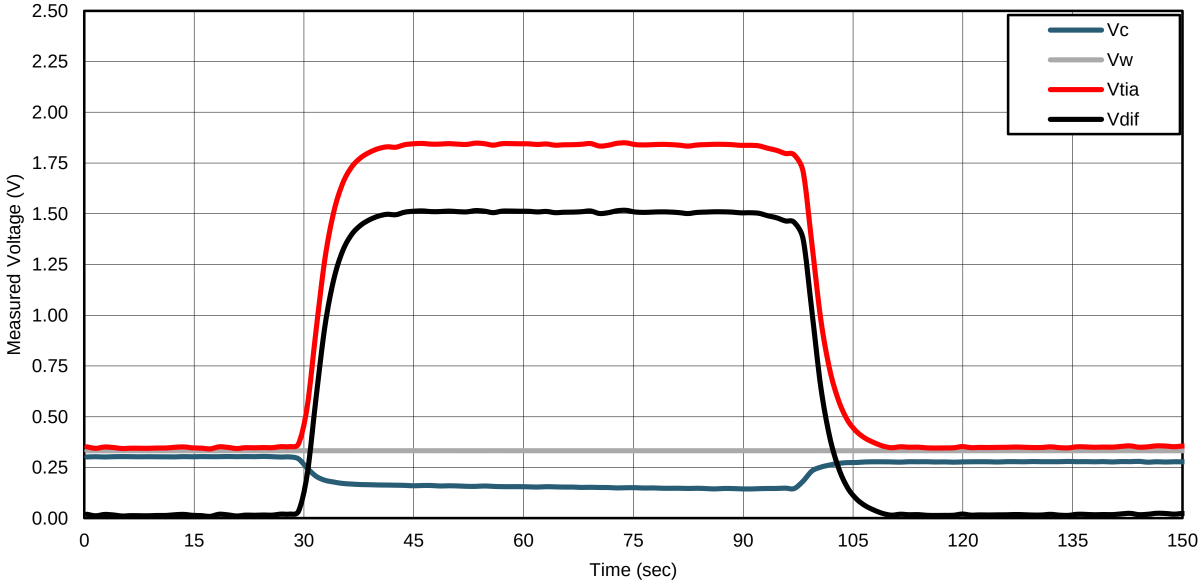


Figure 47. Monitored Voltages when exposed to 200ppm CO

Figure 47 shows the resulting circuit voltages when the sensor was exposed to 200ppm step of carbon monoxide gas. V_C is the monitored CE pin voltage and clearly shows the expected CE voltage dropping below the WE voltage, V_W, as the concentration increases.

V_{TIA} is the output of the transimpedance amplifier U2. V_{DIFF} is the calculated difference between V_{REF} and V_{TIA}, which will be used for the ppm calculation.

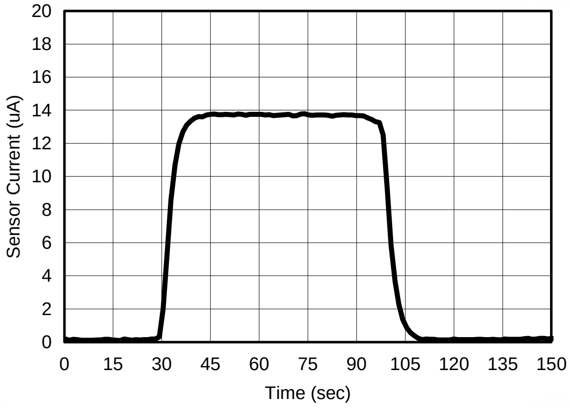


Figure 48. Calculated Sensor Current

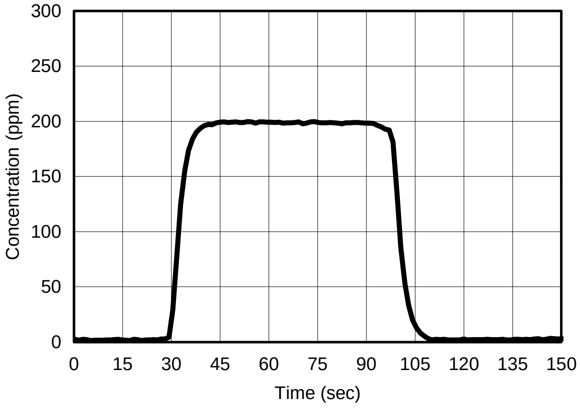


Figure 49. Calculated ppm

Figure 48 shows the calculated sensor current using the formula in Equation 7 :

$$I_{SENSOR} = V_{DIFF} / R_F = 1.52V / 110\ k\Omega = 13.8uA \quad (7)$$

Equation 8 shows the resulting conversion of the sensor current into ppm.

$$ppm = I_{SENSOR} / I_{PERPPM} = 13.8\mu A / 69nA = 200 \quad (8)$$

Total supply current for the amplifier section is less than 700 nA, minus sensor current. Note that the sensor current is sourced from the amplifier output, which in turn comes from the amplifier supply voltage. Therefore, any continuous sensor current must also be included in supply current budget calculations.

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1mA or less (1KΩ per volt).

9 Power Supply Recommendations

The LPV81x is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize strays.

10.2 Layout Example

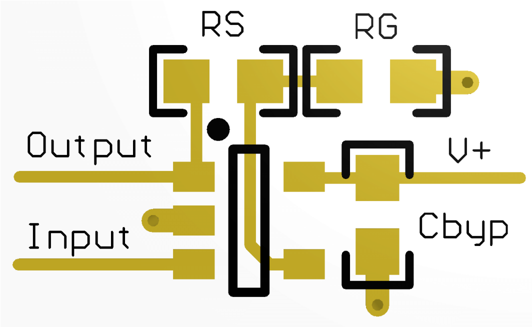


Figure 50. SOT-23 Layout Example (Top View)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

TINA-TI SPICE-Based Analog Simulation Program

DIP Adapter Evaluation Module

TI Universal Operational Amplifier Evaluation Module

TI FilterPro Filter Design Software

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *AN-1798 Designing with Electro-Chemical Sensors*
- *AN-1803 Design Considerations for a Transimpedance Amplifier*
- *AN-1852 Designing With pH Electrodes*
- *Compensate Transimpedance Amplifiers Intuitively*
- *Transimpedance Considerations for High-Speed Operational Amplifiers*
- *Noise Analysis of FET Transimpedance Amplifiers*
- *Circuit Board Layout Techniques*
- *Handbook of Operational Amplifier Applications*

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LPV811	Click here	Click here	Click here	Click here	Click here
LPV812	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.

11.6 Trademarks (continued)

All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV811DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	15TM	Samples
LPV811DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	15TM	Samples
LPV812DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV 812	Samples
LPV812DGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	LPV 812	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

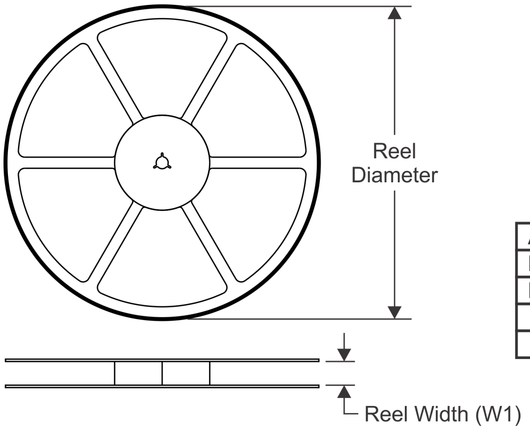
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

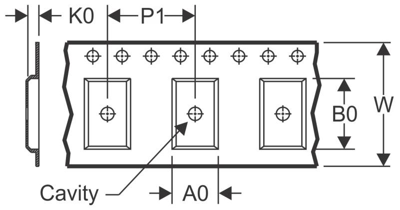
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

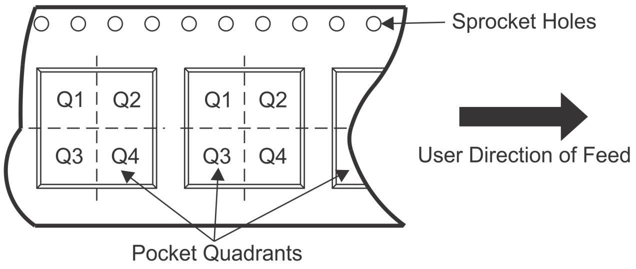


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

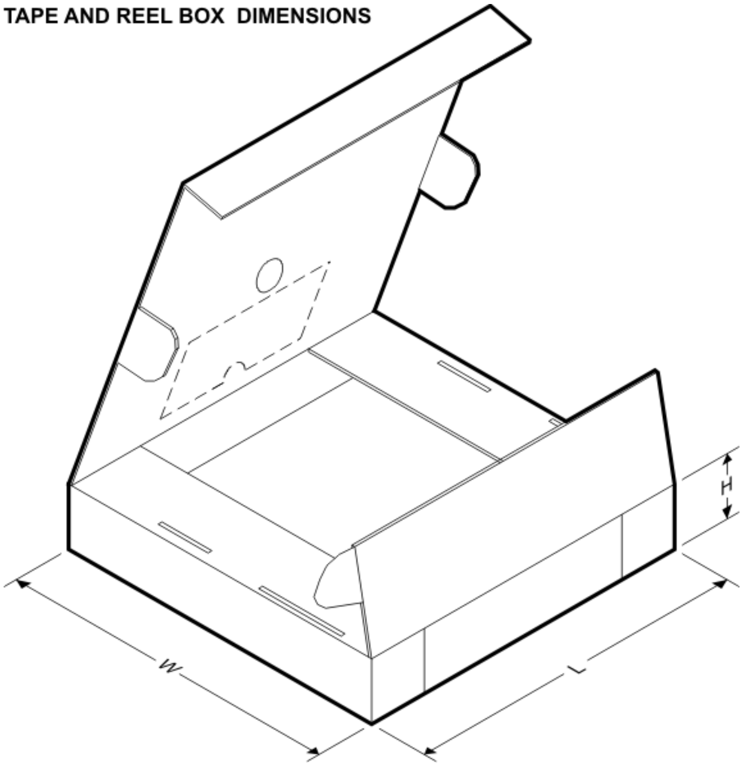
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV811DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV811DBVT	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV812DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV812DGKT	VSSOP	DGK	8	250	178.0	13.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



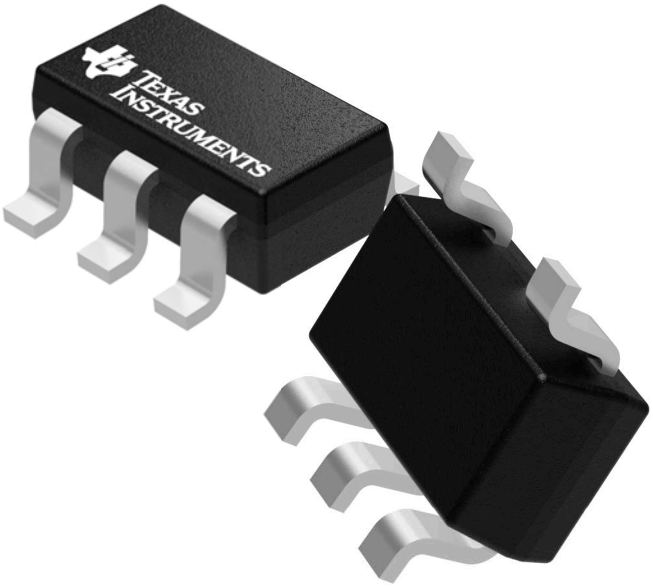
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV811DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LPV811DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
LPV812DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LPV812DGKT	VSSOP	DGK	8	250	202.0	201.0	28.0

DBV 5

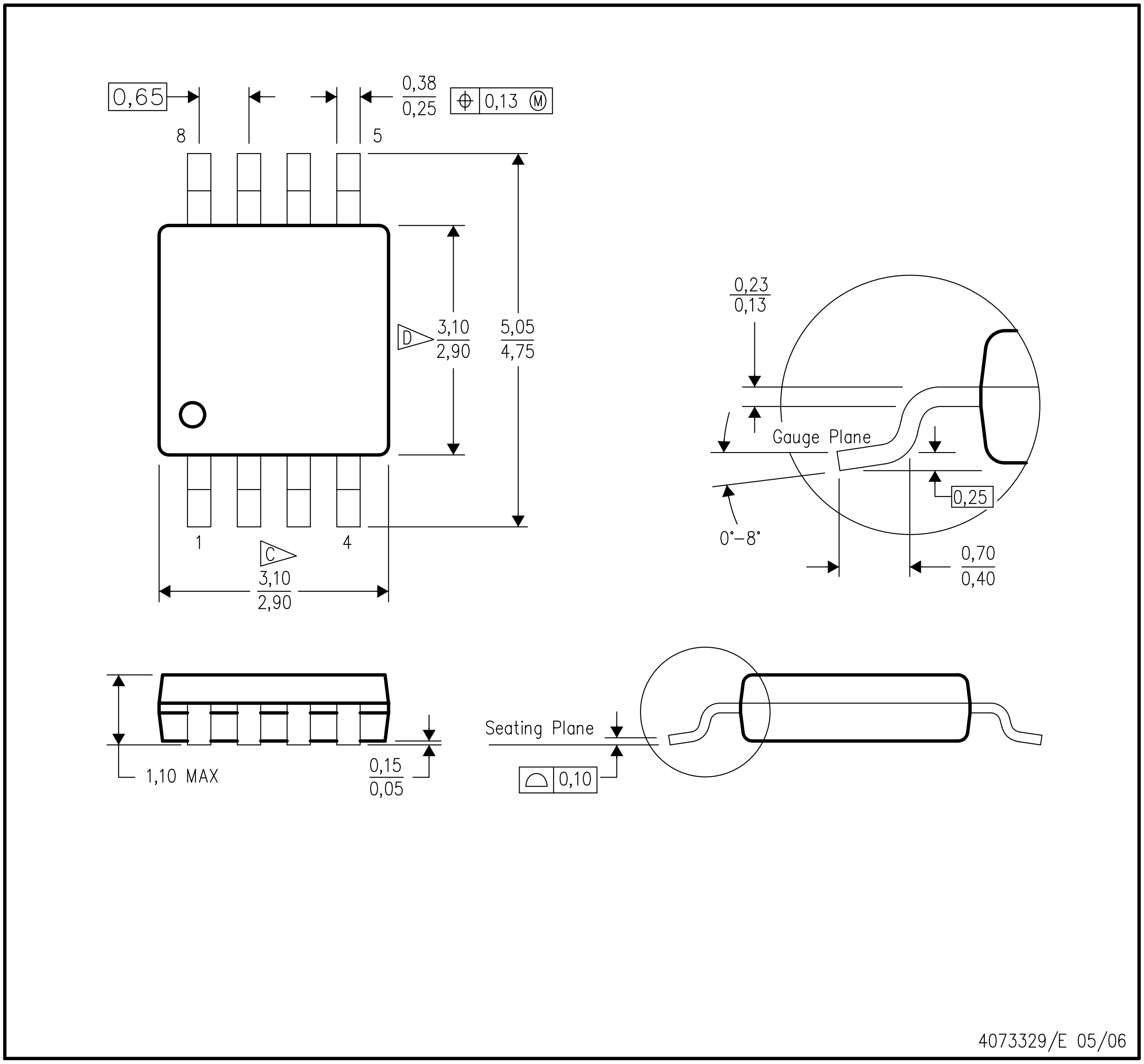
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



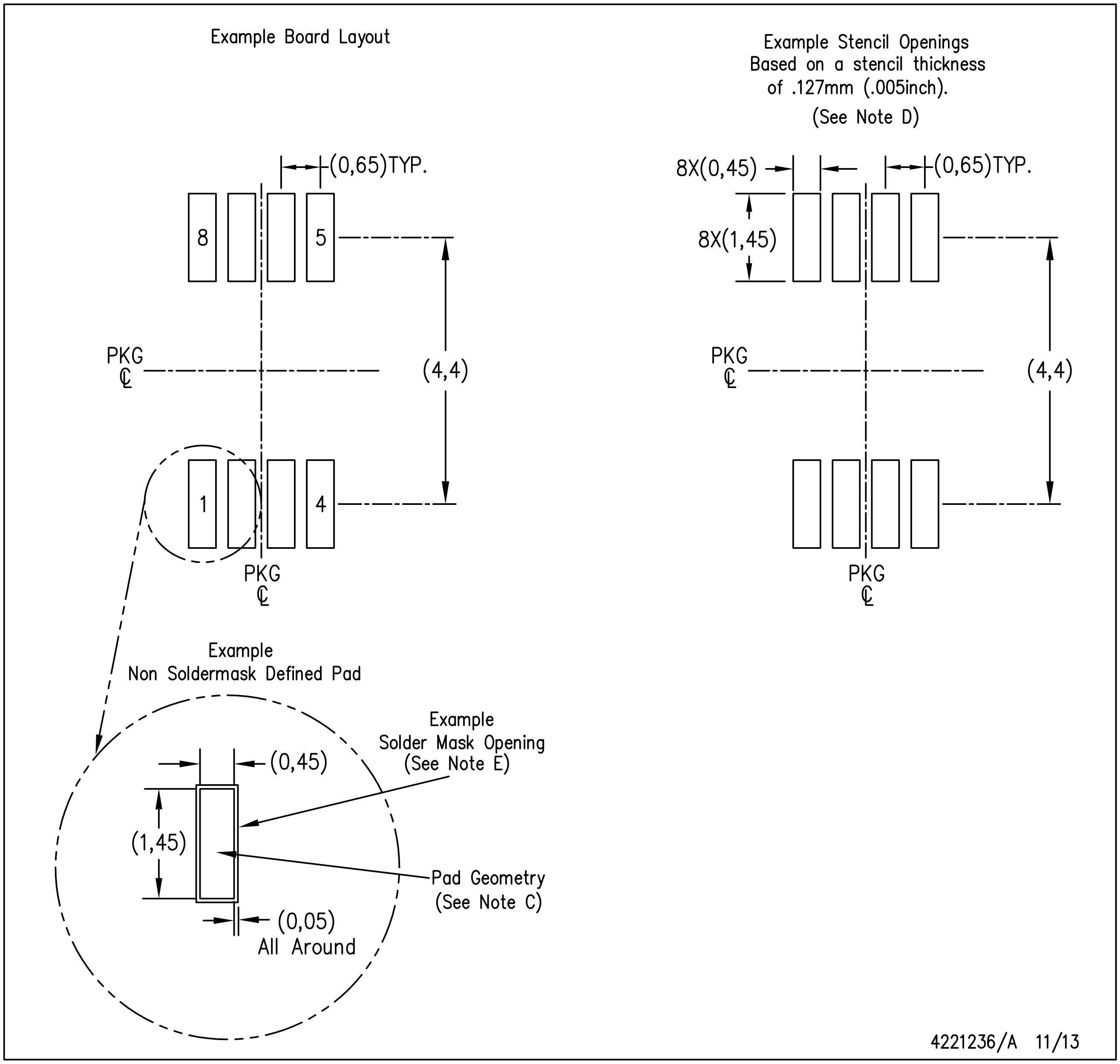
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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