DS3487 Quad TRI-STATE Line Driver

Check for Samples: DS3487

FEATURES

- **Four Independent Drivers**
- **TRI-STATE Outputs**
- **Fast Propagation Times (typ 10 ns)**
- **TTL Compatible**
- **5V Supply**
- **Output Rise and Fall Times Less than 15 ns**
- **Pin Compatible with DS8924 and MC3487**

DESCRIPTION

The DS3487 quad RS-422 driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs.

Block and Connection Diagrams

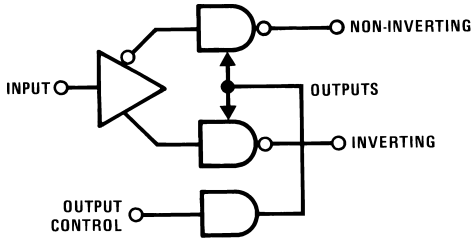


Figure 1. Block Diagram

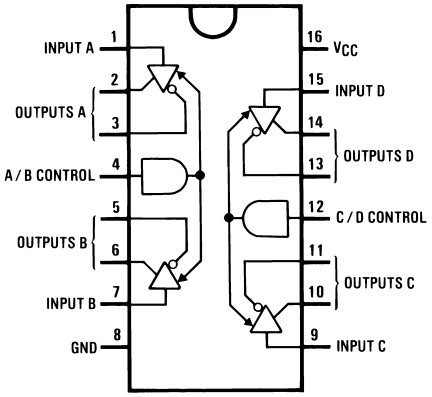


Figure 2. PDIP Package- Top View
See Package Number D0016A or NFG0016E

Truth Table(1)

Input	Control	Non-Inverting	Inverting
	Input	Output	Output
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation (3) at 25°C	
PDIP Package	1476 mW
SOIC Package	1051 mW
Lead Temperature	
(Soldering, 4 seconds)	260°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Derate PDIP molded package 11.9 mW/°C above 25°C. Derate SOIC package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3487	0	+70	°C

Electrical Characteristics(1)(2)(3)(4)

Parameter		Test Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	µA
I_{IH}	Input High Current	V_{IH} = 2.7V				50	µA
		V_{IH} = 5.5V				100	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)	V_O = 0.5V				−100	µA
		V_O = 5.5V				100	µA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0V	V_O = 6V			100	µA
			V_O = −0.25V			−100	µA
$\lvert V_{OS} - \overline{V}_{OS} \rvert$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\lvert V_T \rvert - \lvert \overline{V}_T \rvert$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current	Active			50	80	mA
		TRI-STATE			35	60	mA

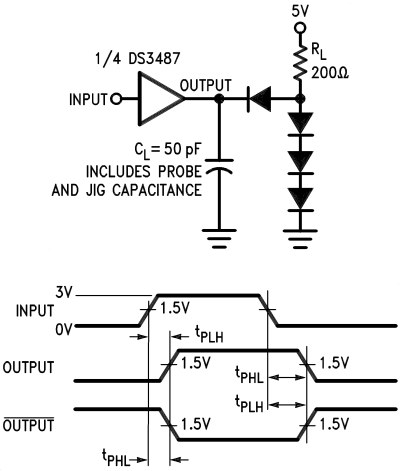
(1) Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) All currents into device pins are positive, all currents out of device pins as negative. All voltages are referenced to ground unless otherwise specified.
(3) Only one output at a time should be shorted.
(4) Symbols and definitions correspond to EIA RS-422, where applicable.

Switching Characteristics

V_{CC} = 5V, T_A = 25°C

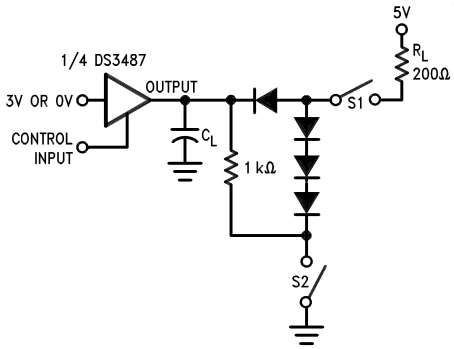
Parameter		Test Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		15	25	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		15	25	ns

AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS

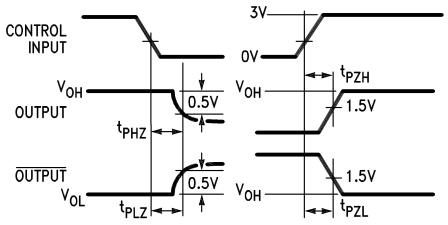


Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

Figure 3. Propagation Delays

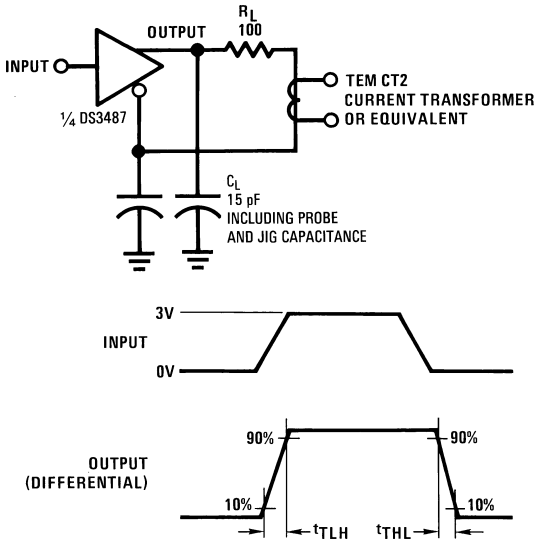


S1 and S2 closed except as noted.
C_L includes probe and jig capacitance.



Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.
S1 = open for t_{PZH}
S2 = open for t_{PZL}

Figure 4. TRI-STATE Enable and Disable Delays



Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

Figure 5. Differential Rise and Fall Times

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS3487MX/NOPB	LIFEBUY	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS3487M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

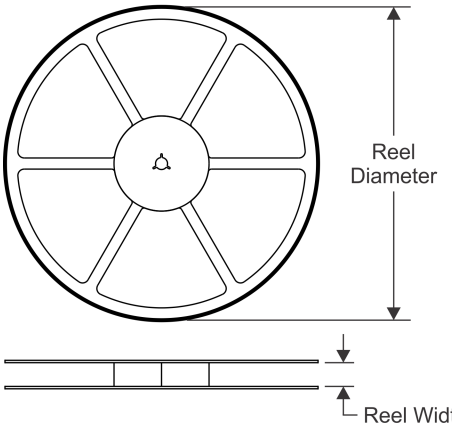
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

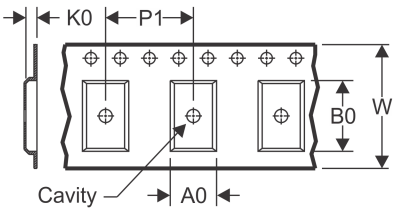
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

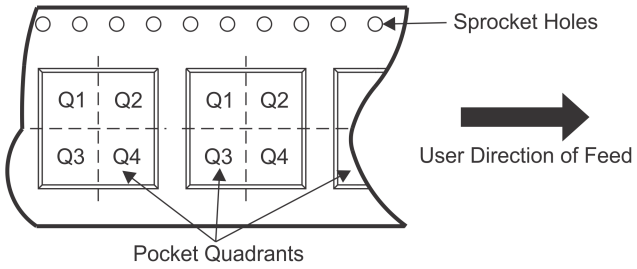


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

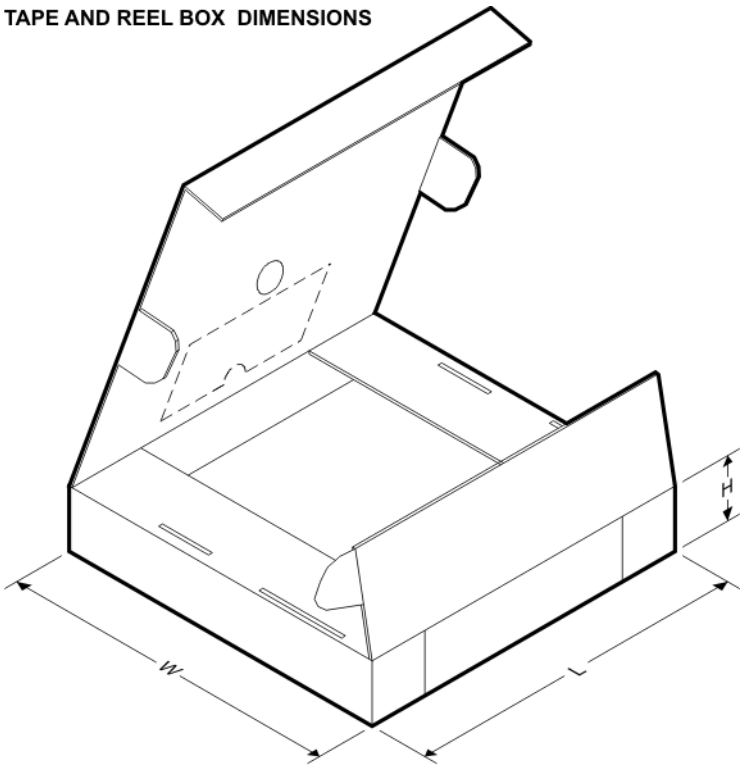
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3487MX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

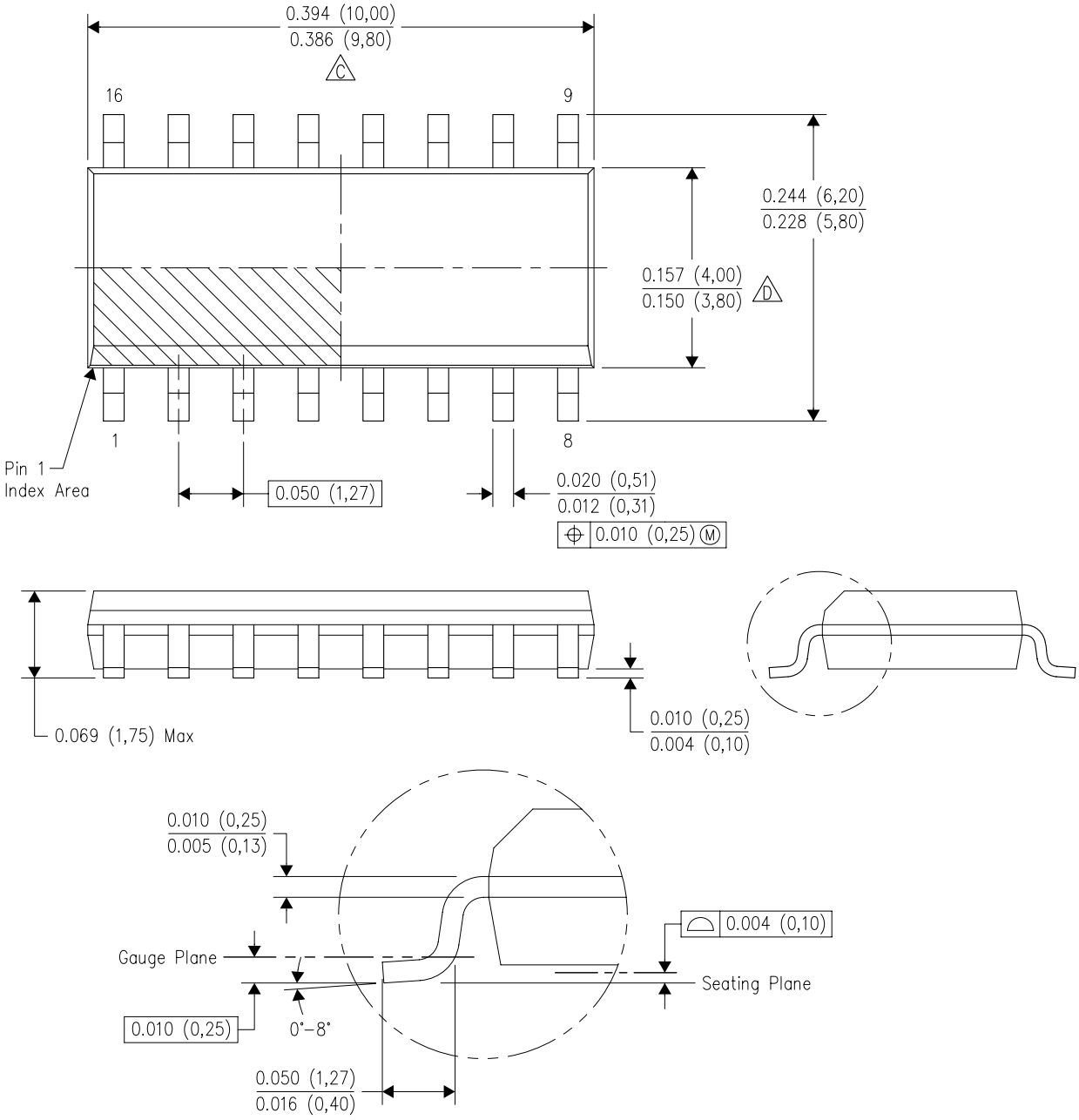
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3487MX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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