CS0809V
Low Capacitance TVS Protection

Features

- Transient protection for high-speed data lines
  - IEC 61000-4-2 (ESD) ±15kV (Air)
    ±8kV (Contact)
  - IEC 61000-4-4 (EFT) 40A (5/50 ns)
  - Cable Discharge Event (CDE)
- Package optimized for high-speed lines
- Small package (2.9mm × 2.8mm × 1.4mm)
- Protects four data lines
- Low capacitance: 3.5pF Typical @ 0V
- Low leakage current: 0.1μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge

General Description

CS0809V is a low-capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 3.5pF only, CS0809V is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A, 5/50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

CS0809V uses small SOT23-6L package. Each CS0809V device can protect four high-speed data lines. The combined features of low capacitance, small size and high ESD robustness make CS0809V ideal for high-speed data ports and high-frequency lines (e.g., USB2.0) applications. The low clamping voltage of the CS0809V guarantees a minimum stress on the protected IC.

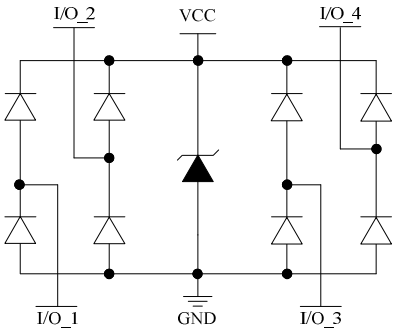
Applications

- USB2.0 Power and Data Line Protection
- Digital Visual Interfaces (DVI)
- 10/100/1000M Ethernet Interfaces
- Desktops, Servers and Notebooks
- SIM Ports
- Monitors and Flat Panel Displays
- Video Graphics Cards

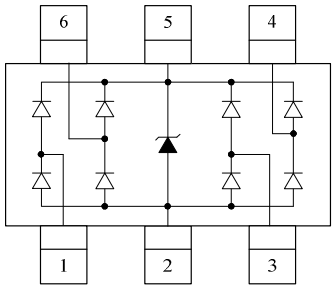
Mechanical Characteristics

- SOT23-6L package
- MSL-3 level
- Flammability Rating: UL 94V-0
- Marking: Part number, Date
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



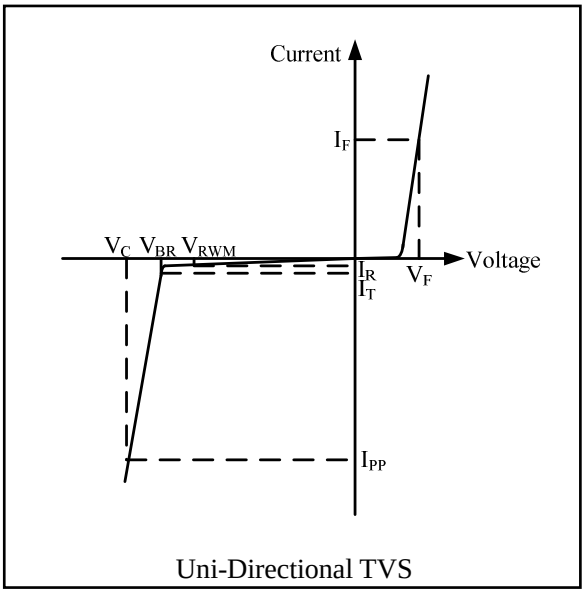
SOT23-6L
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (8/20μs)	17	A
P_{PK}	Peak Pulse Power (8/20μs)	350	Watts
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±30 ±30	kV
T_{OPT}	Operating Temperature	-55/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T = 25° C)

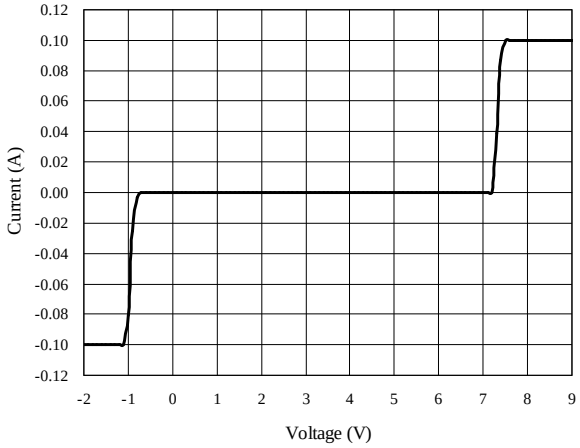
Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F



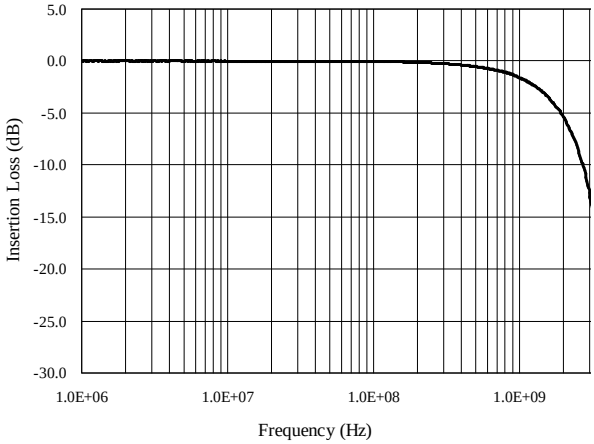
Uni-Directional TVS

Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	V_{RWM} = 5V, T = 25° C Between I/O and GND		0.1	1.0	μA
V_{BR}	I_T = 1mA Between I/O and GND	6.0	7.0	9.0	V
V_F	I_F = 15mA			1.2	V
V_C	I_{PP} = 1A, t_p = 8/20μs Between I/O and GND			12	V
V_C	I_{PP} = 5A, t_p = 8/20μs Between I/O and GND			17	V
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and GND		3.5	5.0	pF
C_{ESD}	V_R = 0V, f = 1MHz Between I/O and I/O		1.5	2.5	pF

Voltage Sweeping of I/O to GND

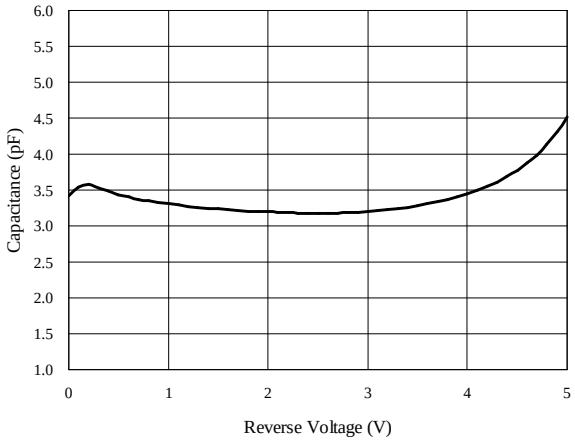


Insertion Loss S21 of I/O to GND

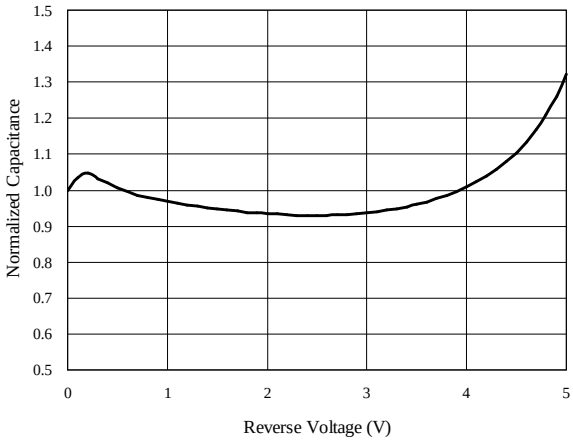


Capacitance *vs.* Voltage of I/O to GND (f = 1MHz)

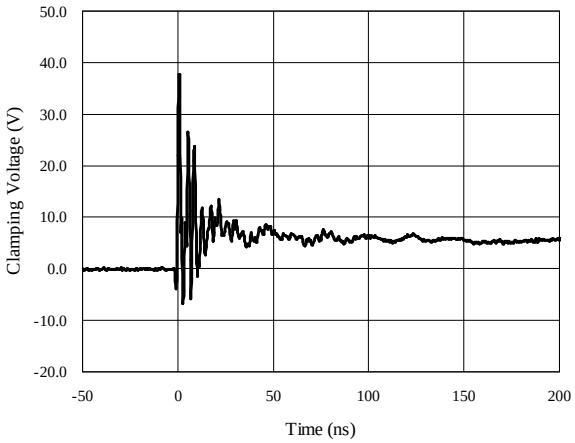
Capacitance *vs.* Reverse Voltage



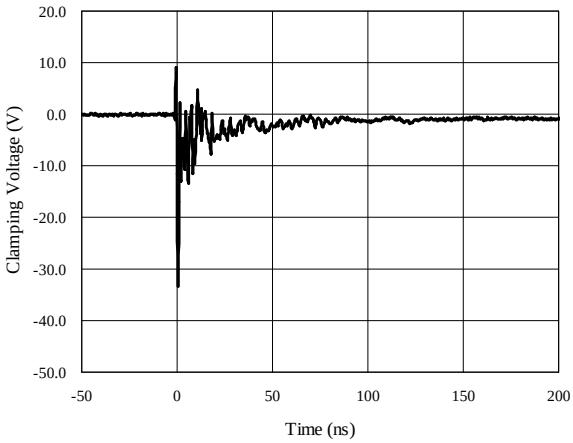
Normalized Capacitance *vs.* Reverse Voltage



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

CS0809V is capable to provide ESD protection for four data lines simultaneously. The pin connection is shown in Figure 1.

Four parallel data lines, from inner IC to I/O port connector, could connect to CS0809V four I/O pins directly. Pin 2 of CS0809V is the negative reference pin, which should connect to the GND of PCB; while Pin 5 of CS0809V is the positive reference pin, which should connect to the power supply of PCB. The connection wires should be as short as possible in order to minimize the parasitic inductance.

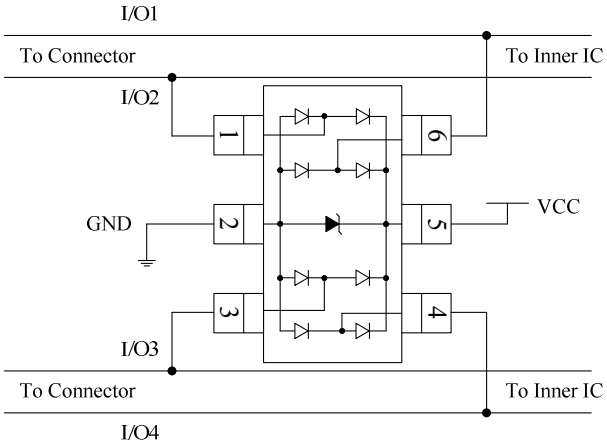


Figure 1 CS0809V pin connection in PCB

Clamping Voltage Optimization

CS0809V could use its power clamping circuit to limit the TVS clamping voltage (V_C) to a suitable value during positive and negative mode ESD stress. Taking positive mode as example shown in Figure 2, if there is no power clamping circuit in CS0809V, the I_{ESD1} will be the ESD shunting current from I/O to VCC via D1 and L_p. The clamping voltage V_C at I/O port will be:

$$V_C = V_{F,D1} + L_p \frac{dI_{ESD1}}{dt} + V_{CC} \qquad (1)$$

where $V_{F,D1}$ is the forward turn-on voltage of the steering diode D1, L_p is the parasitic inductance in the ESD current shunting path.

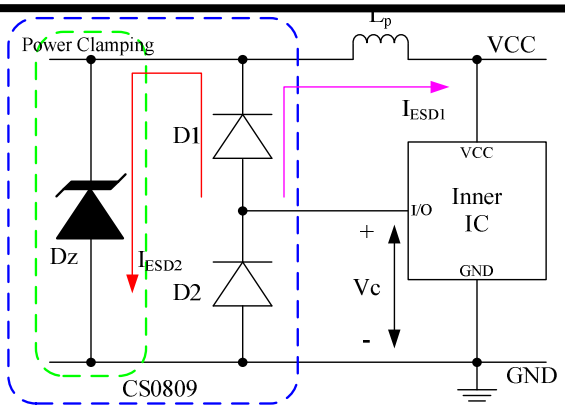


Figure 2 Positive ESD Clamping Voltage Optimization

As we all know, the ESD pulse could discharge huge current in a very short time, from 0.2ns to 10 ns. Thus, the V_C will exceed the inner circuit capability. However, if with the power clamping circuit in CS0809V, the ESD shunting current will be I_{ESD2}, which leading to the clamping voltage V_C as:

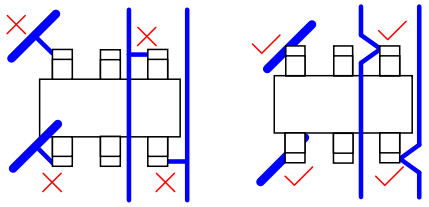
$$V_C = V_{F,D1} + V_{BR,Dz} + V_{CC} \qquad (2)$$

where $V_{BR,Dz}$ is the reverse breakdown voltage of diode D_Z, which is much smaller than the induced clamping voltage by parasitic inductance L_p in (1)

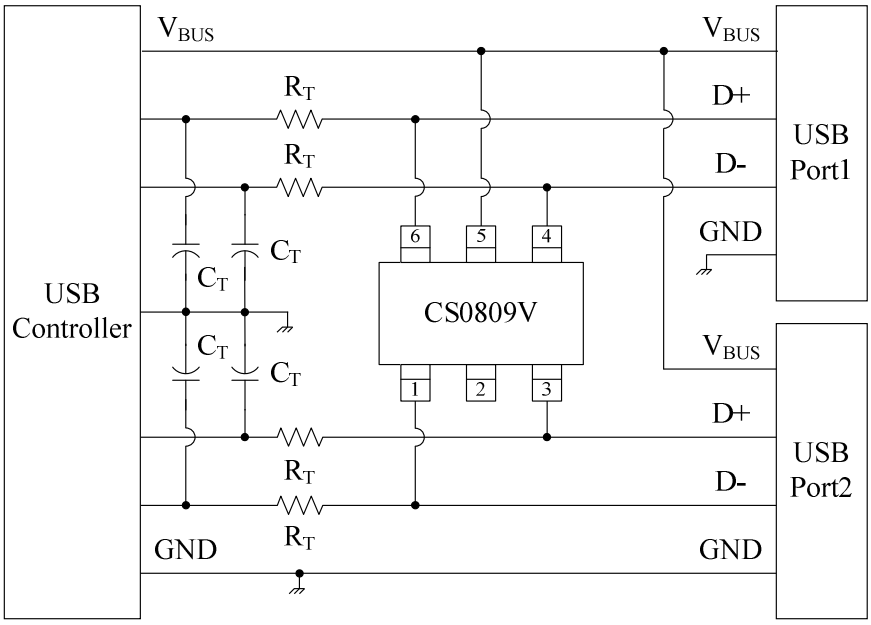
PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

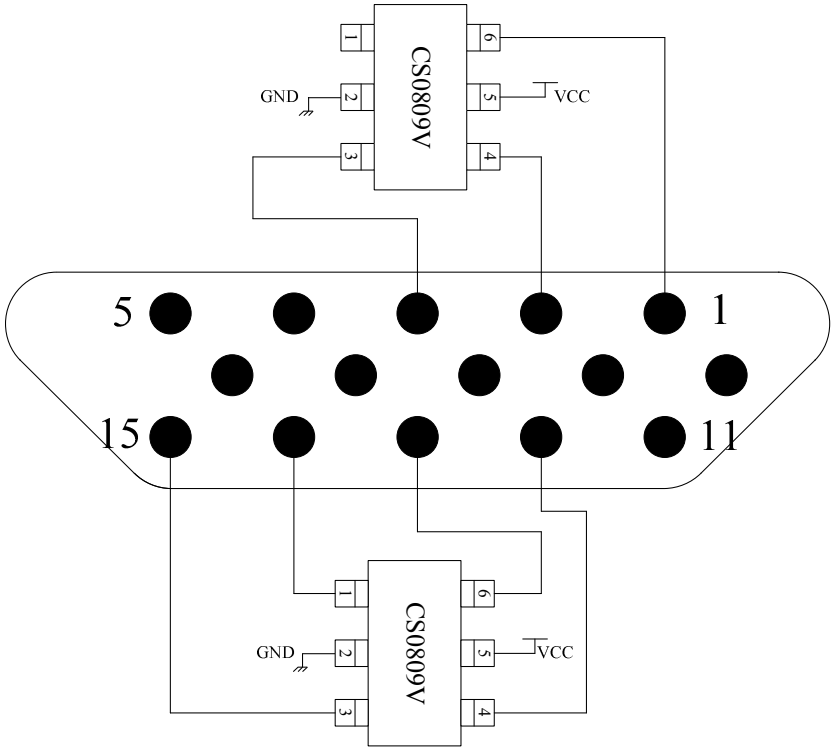
- CS0809V GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting CS0809V VCC & GND pins to the PCB VCC & GND should be wide.
- Place CS0809V as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.



Application Information (*continued*)

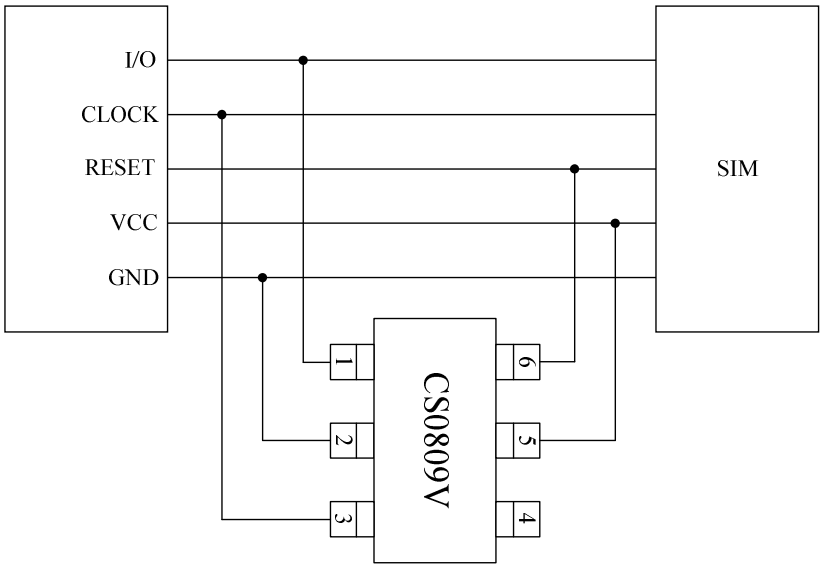


Layout Top View for Dual USB Ports with CS0809V

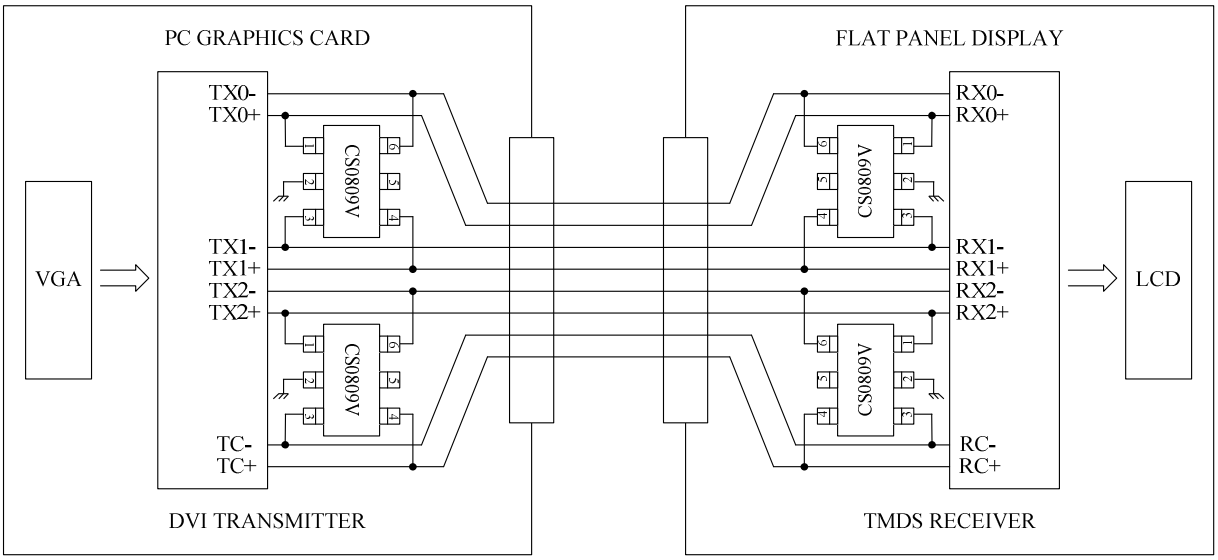


Layout Top View for Video (VGA) Interface with CS0809V

Application Information (*continued*)

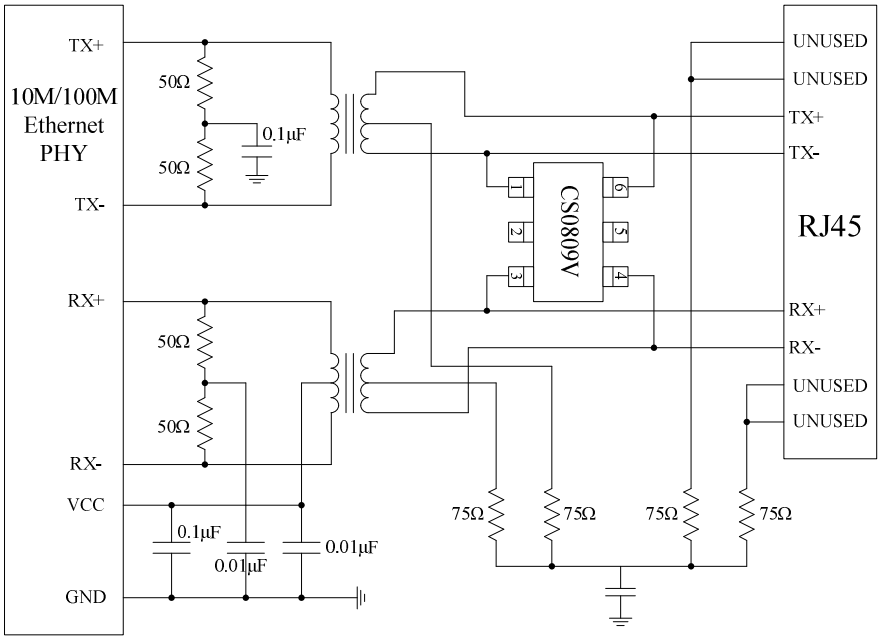


Layout Top View for SIM Port with CS0809V

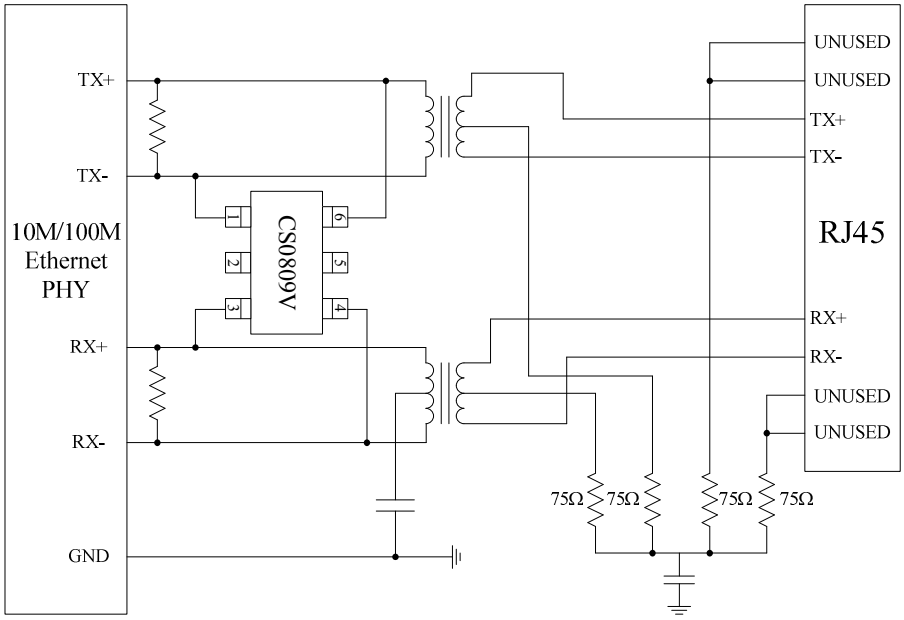


Layout Top View for Digital Visual Interface (DVI) with CS0809V

Application Information (*continued*)



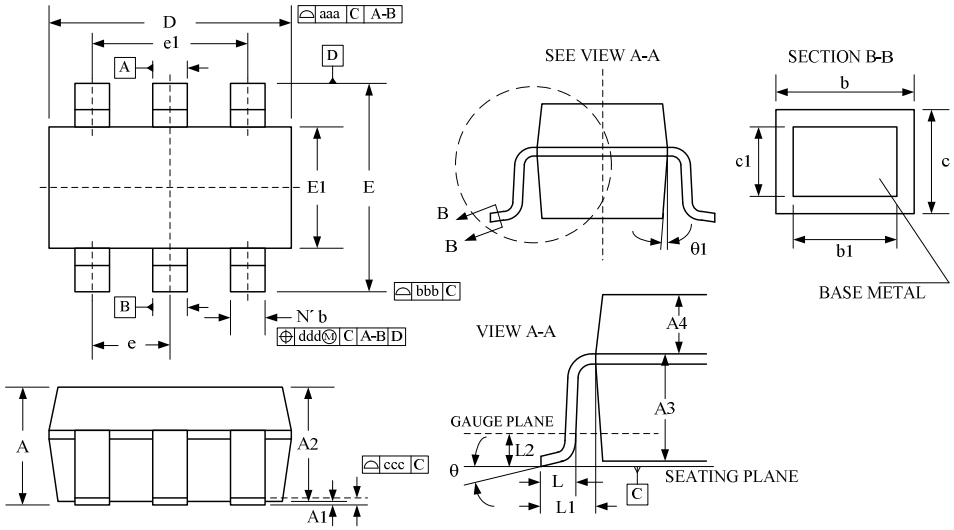
Differential Protection for 10M/100M Ethernet Interface with CS0809V



Differential and Common Mode Protection for 10M/100M Ethernet Interface with CS0809V

Package Outline

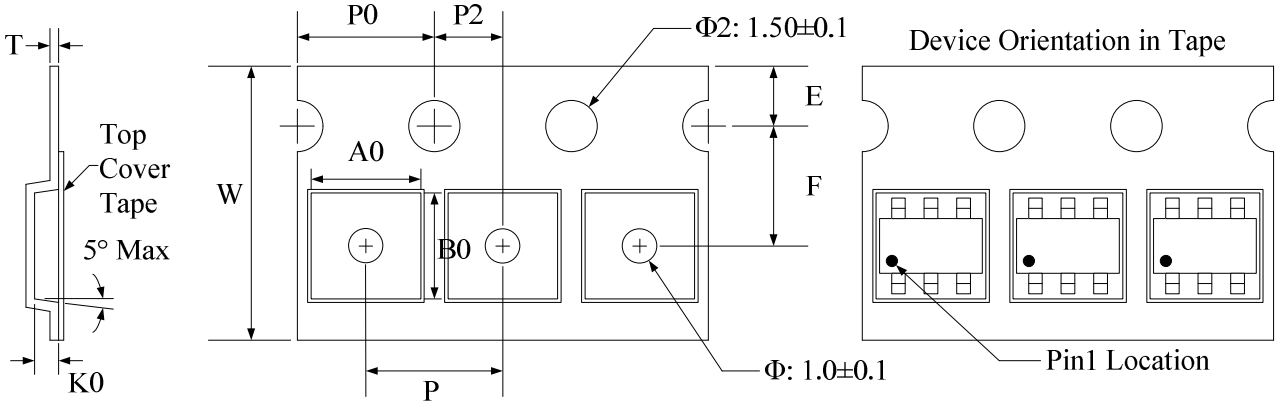
- SOT23-6L package
- MSL-3 level



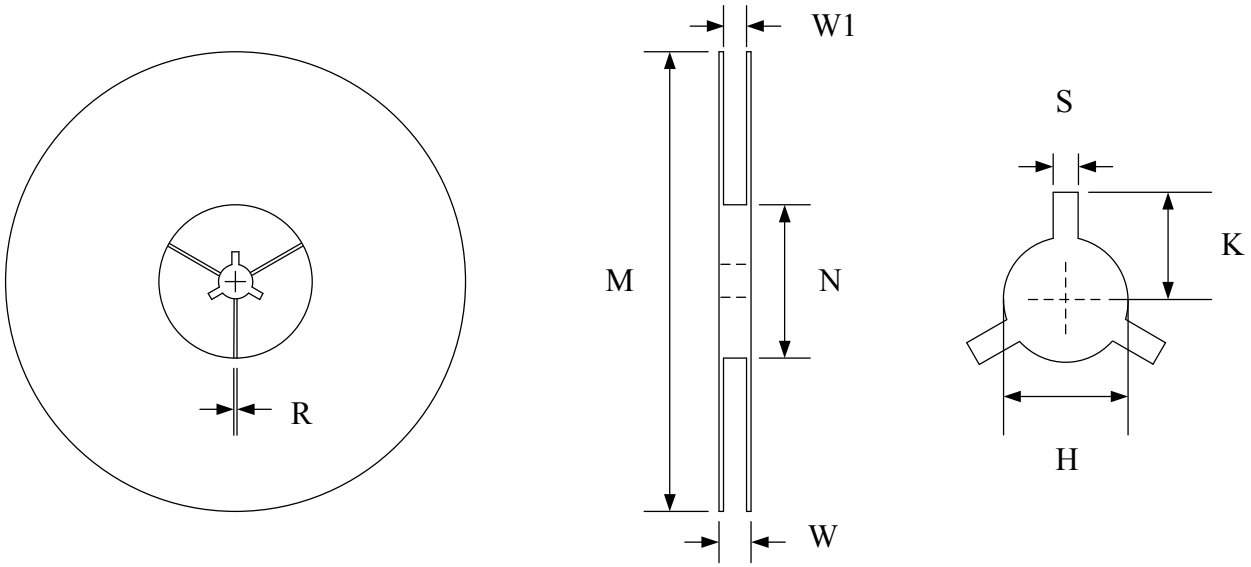
Package Dimensions (Controlling dimensions are in millimeters)

Symbol	Dimensions (mm)			Dimensions (Inches)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A	—	—	1.450	—	—	0.057
A1	0.000	—	0.150	0.000	—	0.006
A2	0.900	1.200	1.300	0.035	0.047	0.012
A3	0.637	0.787	0.837	0.025	0.031	0.033
A4	0.263	0.413	0.463	0.010	0.016	0.018
b	0.300	—	0.500	0.012	—	0.020
b1	0.300	0.400	0.450	0.012	0.016	0.018
c	0.080	—	0.220	0.003	—	0.009
c1	0.080	0.130	0.200	0.003	0.005	0.008
D	2.90 BSC			0.114 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
L	0.300	0.450	0.600	0.012	0.018	0.024
L1	0.600 REF			0.024 REF		
L2	0.250 BSC			0.010 BSC		
θ	0°	4°	8°	0°	4°	8°
θ1	5°	10°	15°	5°	10°	15°
aaa	0.150			0.006		
bbb	0.200			0.008		
ccc	0.100			0.004		
ddd	0.100			0.004		

Tape and Reel Specification

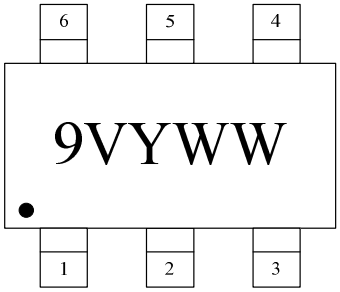


Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	8.00+0.3 -0.1	3.23±0.05	3.17±0.05	1.37±0.05	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1	2.0±0.05	0.25±0.02



Symbol	Reel Size	M	N	W	W1	H	S	K	R
Dimensions (mm)	Φ178	178.0±1.0	60.0±1.0	11.5±0.5	9.0±0.5	13.0±0.5	2.0±0.1	11.0±0.2	1.0±0.05

Marking Codes



Note:

(1) "9V" is part number, fixed.

(2) "YWW" is date code. "Y" is the assembly year (2011 is "1"); while "WW" is the assembly week in a year.

Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
CS0809V	5V	3,000	7 Inch