

Ultra-Low Bias Current *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 100fA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 10 μ V/°C max
- HIGH OPEN-LOOP GAIN: 94dB min
- LOW NOISE: 15nV/ $\sqrt{\text{Hz}}$ at 10kHz
- PLASTIC DIP AND SO PACKAGES

APPLICATIONS

- PHOTODETECTOR PREAMPS
- CHROMATOGRAPHY
- ELECTROMETER AMPLIFIERS
- MASS SPECTROMETERS
- pH PROBE AMPLIFIERS
- ION GAGE MEASUREMENT

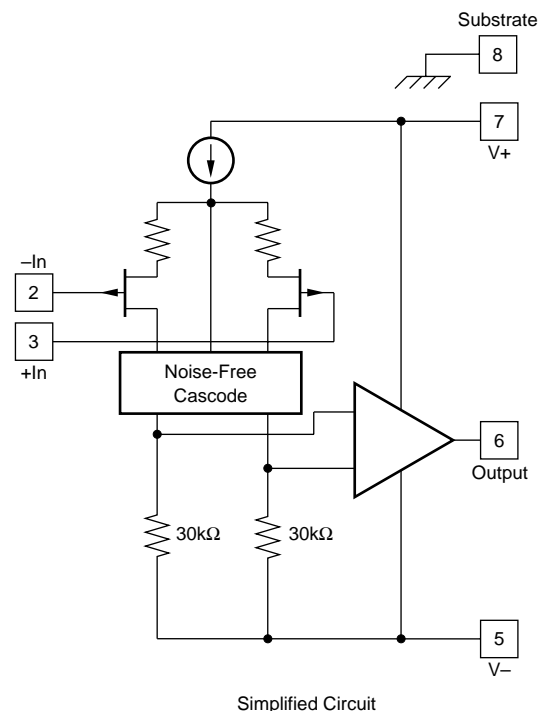
DESCRIPTION

The OPA129 is an ultra-low bias current monolithic operational amplifier offered in an 8-pin PDIP and SO-8 package. Using advanced geometry dielectrically-isolated FET (*Difet*[®]) inputs, this monolithic amplifier achieves a high performance level.

Difet fabrication eliminates isolation-junction leakage current—the main contributor to input bias current with conventional monolithic FETs. This reduces input bias current by a factor of 10 to 100. Very low input bias current can be achieved without resorting to small-geometry FETs or CMOS designs which can suffer from much larger offset voltage, voltage noise, drift, and poor power-supply rejection.

The OPA129 special pinout eliminates leakage current that occurs with other op amps. Pins 1 and 4 have no internal connection, allowing circuit board guard traces—even with the surface-mount package version.

OPA129 is available in 8-pin DIP and SO packages, specified for operation from –40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Difet is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

SPECIFICATIONS

ELECTRICAL

At $V_S = \pm 15V$ and $T_A = +25^\circ C$, unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITION	OPA129PB, UB			OPA129P, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BIAS CURRENT⁽¹⁾ vs Temperature	$V_{CM} = 0V$		± 30	± 100		*	± 250	fA
			Doubles every $10^\circ C$				*	
INPUT OFFSET CURRENT	$V_{CM} = 0V$		± 30			*		fA
OFFSET VOLTAGE Input Offset Voltage vs Temperature Supply Rejection	$V_{CM} = 0V$ $V_S = \pm 5V$ to $\pm 18V$		± 0.5 ± 3 ± 3	± 2 ± 10 ± 100		± 1 ± 5 *	± 5 *	mV $\mu V/^\circ C$ $\mu V/V$
NOISE Voltage Current	$f = 10Hz$ $f = 100Hz$ $f = 1kHz$ $f = 10kHz$ $f_B = 0.1Hz$ to $10Hz$ $f = 10kHz$		85 28 17 15 4 0.1			*		nV/\sqrt{Hz} nV/\sqrt{Hz} nV/\sqrt{Hz} nV/\sqrt{Hz} μV_{PP} fA/\sqrt{Hz}
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{15} \parallel 2$			*		$\Omega \parallel pF$ $\Omega \parallel pF$
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10V$	± 10 80	± 12 118		*	*		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	94	120		*	*		dB
FREQUENCY RESPONSE Unity Gain, Small Signal Full Power Response Slew Rate Settling Time: 0.1% 0.01% Overload Recovery, 50% Overdrive ⁽²⁾	$20V_{p-p}$, $R_L = 2k\Omega$ $V_O = \pm 10V$, $R_L = 2k\Omega$ $G = -1$, $R_L = 2k\Omega$, $10V$ Step $G = -1$	1	1 47 2.5 5 10 5		*	*		MHz kHz V/ μs μs μs μs
RATED OUTPUT Voltage Output Current Output Load Capacitance Stability Short-Circuit Current	$R_L = 2k\Omega$ $V_O = \pm 12V$ Gain = +1	± 12 ± 6	± 13 ± 10 1000 ± 35	± 55	*	*	*	V mA pF mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_O = 0mA$	± 5	± 15 1.2	± 18 1.8	*	*	*	V V mA
TEMPERATURE Specification Operating Storage Thermal Resistance DIP-8 SO-8	Ambient Temperature Ambient Temperature θ_{JA} , Junction-to-Ambient	-40 -40 -40		+85 +125 +125	*	*	*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$

NOTES: (1) High-speed automated test.

(2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Differential Input Voltage	V ₋ to V ₊
Input Voltage Range	V ₋ to V ₊
Storage Temperature Range	-40°C to +125°C
Operating Temperature Range	-40°C to +125°C
Output Short Circuit Duration ⁽¹⁾	Continuous
Junction Temperature (T _j)	+150°C

NOTE: (1) Short circuit may be to power supply common at +25°C ambient.



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

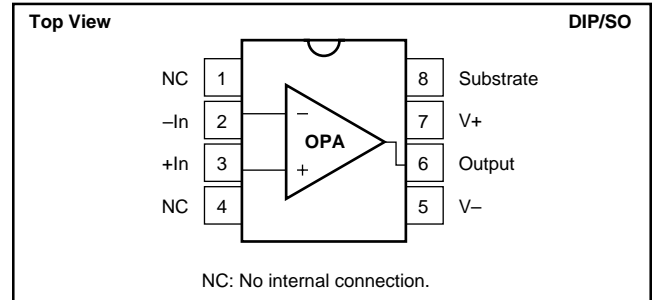
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR
OPA129P	DIP-8	P
OPA129PB	DIP-8	P
OPA129U	SO-8	D
OPA129UB	SO-8	D

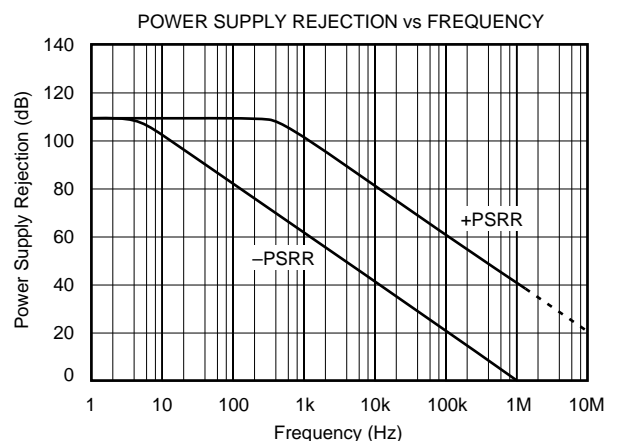
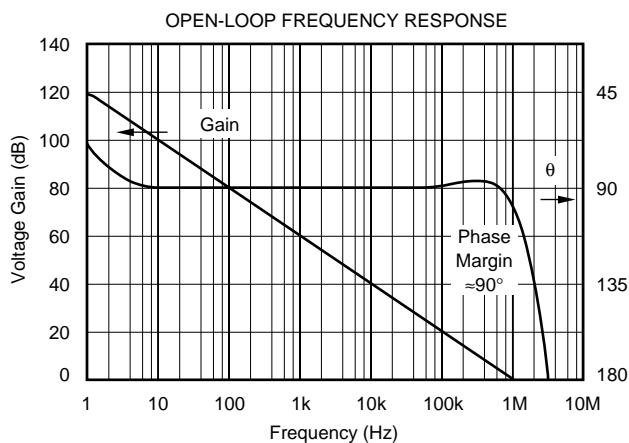
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

CONNECTION DIAGRAM



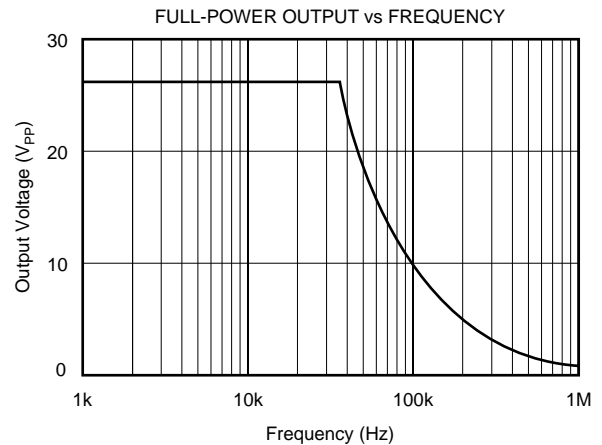
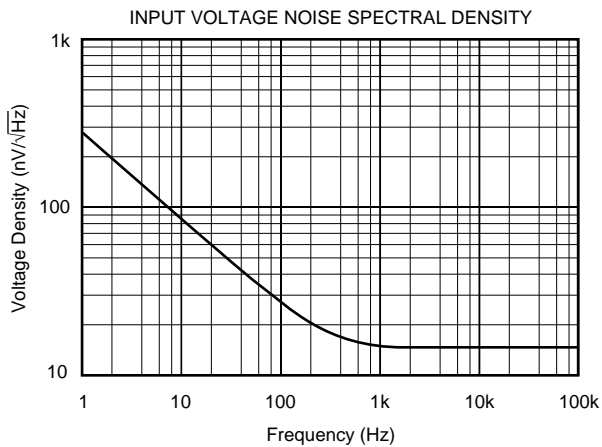
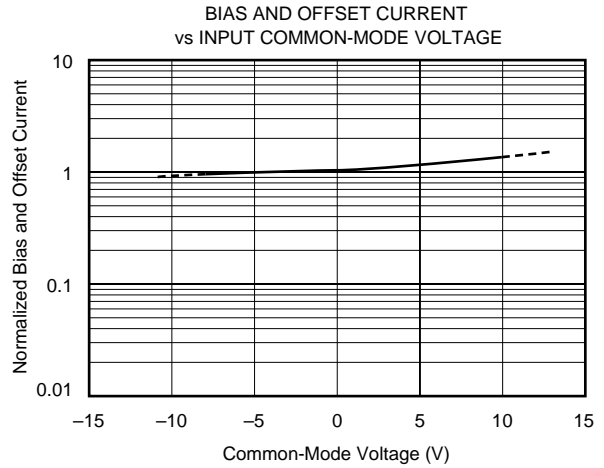
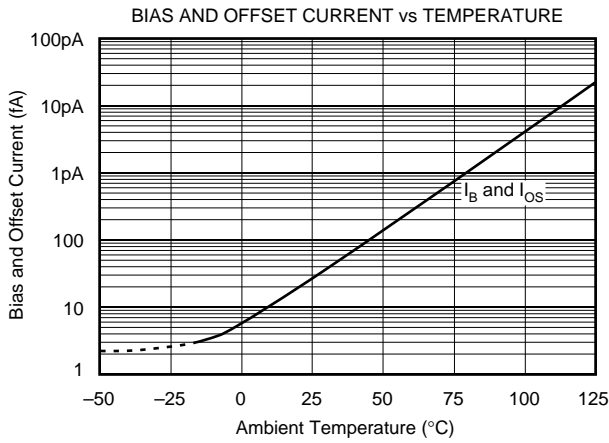
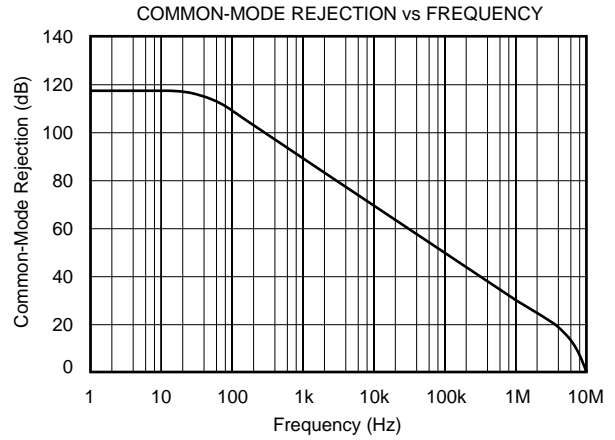
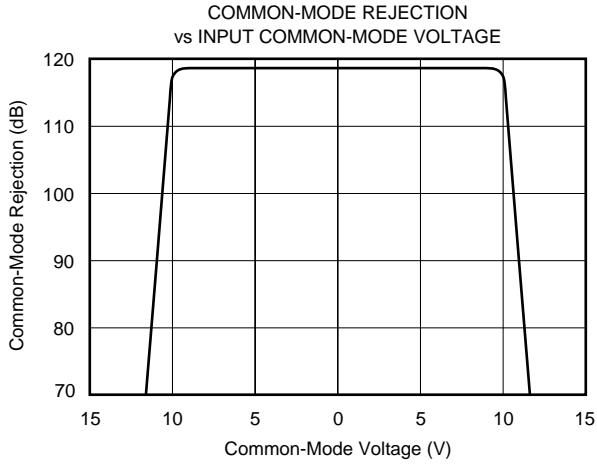
TYPICAL PERFORMANCE CURVES

At T_a = +25°C, +15VDC, unless otherwise noted.



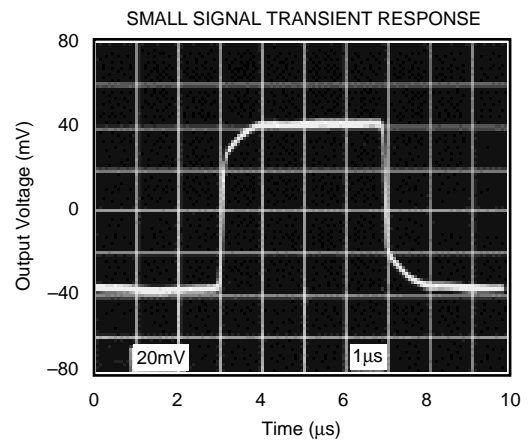
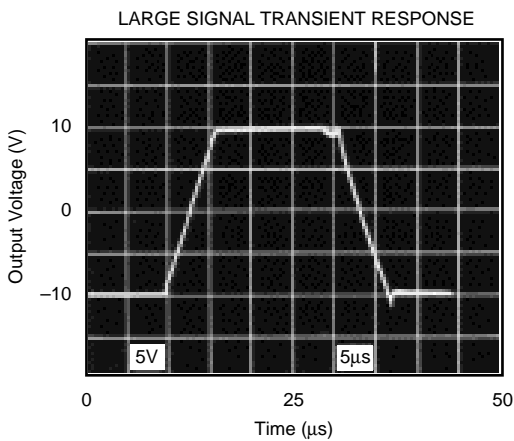
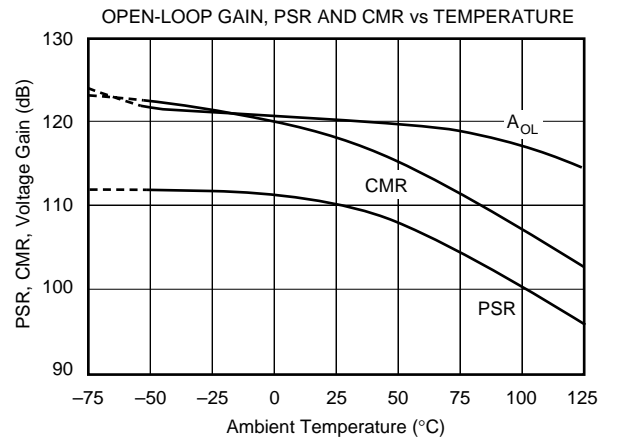
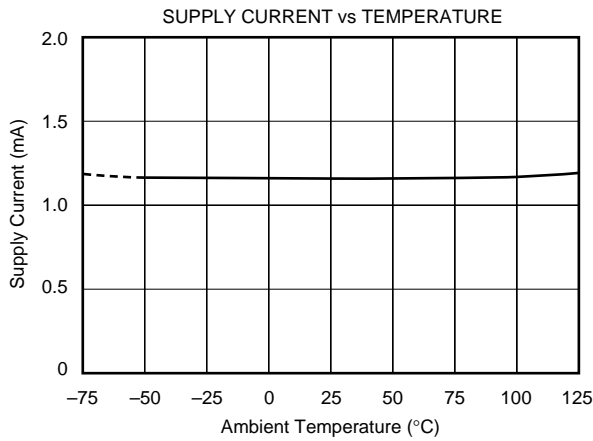
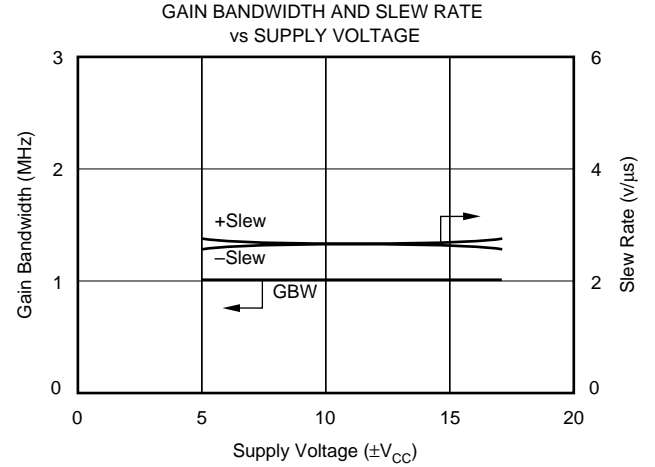
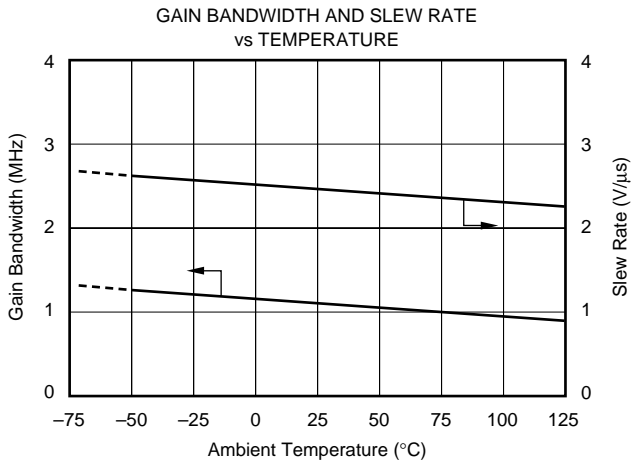
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$, $+15\text{VDC}$, unless otherwise noted.



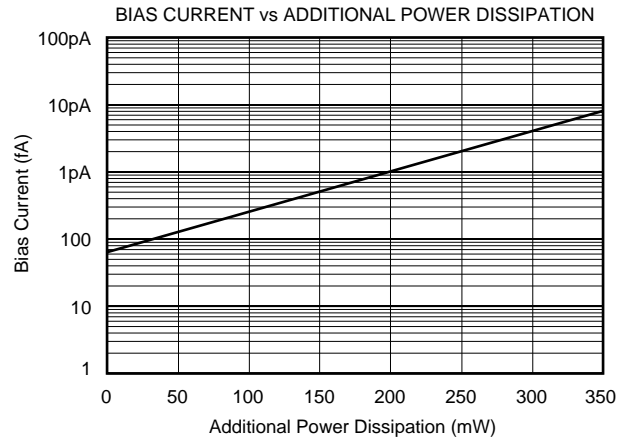
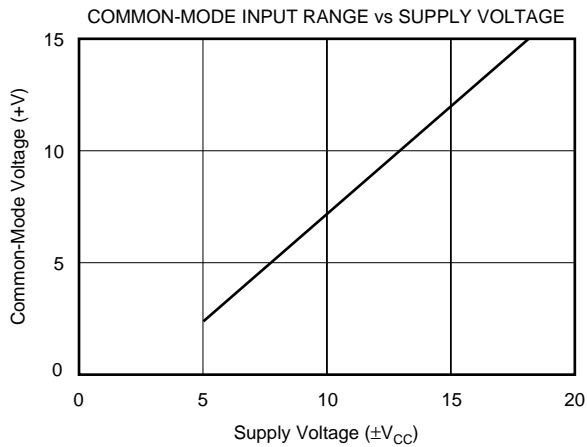
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$, $+15\text{VDC}$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, +15VDC, unless otherwise noted.



APPLICATIONS INFORMATION

NON-STANDARD PINOUT

The OPA129 uses a non-standard pinout to achieve lowest possible input bias current. The negative power supply is connected to pin 5—see Figure 1. This is done to reduce the leakage current from the V- supply (pin 4 on conventional op amps) to the op amp input terminals. With this new pinout, sensitive inputs are separated from both power supply pins.

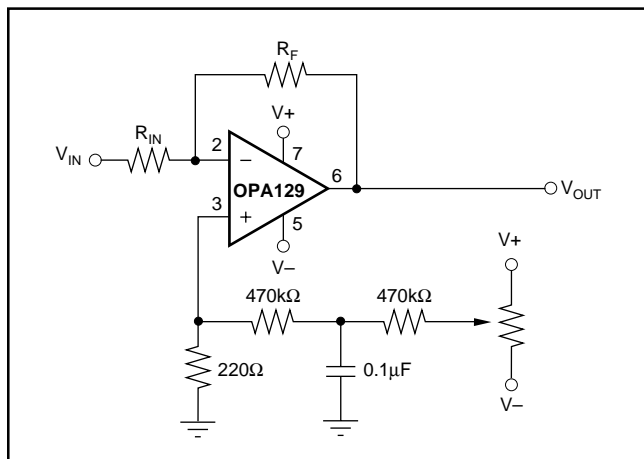


FIGURE 1. Offset Adjust Circuit.

OFFSET VOLTAGE TRIM

The OPA129 has no conventional offset trim connections. Pin 1, next to the critical inverting input, has no internal connection. This eliminates a source of leakage current and allows guarding of the input terminals. Pin 1 and pin 4, next to the two input pins, have no internal connection. This allows an optimized circuit board layout with guarding—see the *Circuit Board Layout* section.

Due to its laser-trimmed input stage, most applications do not require external offset voltage trimming. If trimming is required, the circuit shown in Figure 1 can be used. Power supply voltages are divided down, filtered and applied to the non-inverting input. The circuit shown is sensitive to variation in the supply voltages. Regulation can be added, if needed.

GUARDING AND SHIELDING

Ultra-low input bias current op amps require precautions to achieve best performance. Leakage current on the surface of circuit board can exceed the input bias current of the amplifier. For example, a circuit board resistance of $10^{12}\Omega$ from a power supply pin to an input pin produces a current of 15pA—more than 100 times the input bias current of the op amp.

To minimize surface leakage, a guard trace should completely surround the input terminals and other circuitry connecting to the inputs of the op amp. The DIP package should have a guard trace on both sides of the circuit board. The guard ring should be driven by a circuit node equal in potential to the op amp inputs—see Figure 2. The substrate, pin 8, should also be connected to the circuit board guard to assure that the amplifier is fully surrounded by the guard potential. This minimizes leakage current and noise pick-up.

Careful shielding is required to reduce noise pickup. Shielding near feedback components may also help reduce noise pick-up.

Triboelectric effects (friction-generated charge) can be a troublesome source of errors. Vibration of the circuit board, input connectors and input cables can cause noise and drift. Make the assembly as rigid as possible. Attach cables to avoid motion and vibration. Special low noise or low leakage cables may help reduce noise and leakage current. Keep all input connections as short possible. Surface-mount components may reduce circuit board size and allow a more rigid assembly.

CIRCUIT BOARD LAYOUT

The OPA129 uses a new pinout for ultra low input bias current. Pin 1 and pin 4 have no internal connection. This allows ample circuit board space for a guard ring surrounding the op amp input pins—even with the tiny SO-8 surface-mount package. Figure 3 shows suggested circuit board layouts. The guard ring should be connected to pin 8 (substrate) as shown. It should be driven by a circuit node equal in potential to the input terminals of the op amp—see Figure 2 for common circuit configurations.

TESTING

Accurately testing the OPA129 is extremely difficult due to its high performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current. Inaccurate bias current measurements can be due to:

1. Test socket leakage.
2. Unclean package.
3. Humidity or dew point condensations.
4. Circuit contamination from fingerprints or anti-static treatment chemicals.
5. Test ambient temperature.
6. Load power dissipation.
7. Mechanical stress.
8. Electrostatic and electromagnetic interference.

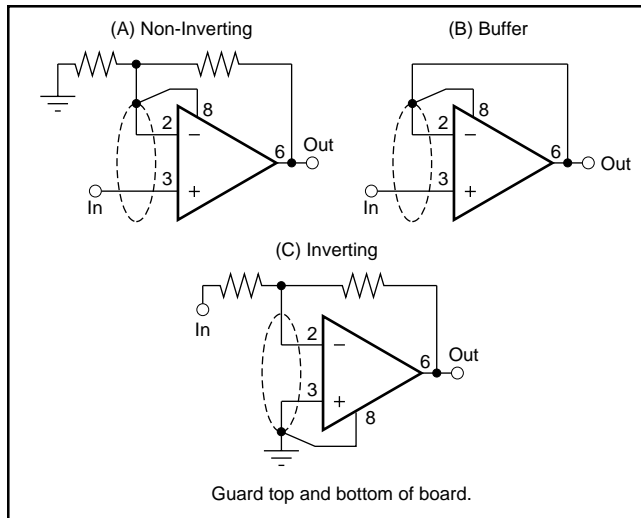


FIGURE 2. Connection of Input Guard.

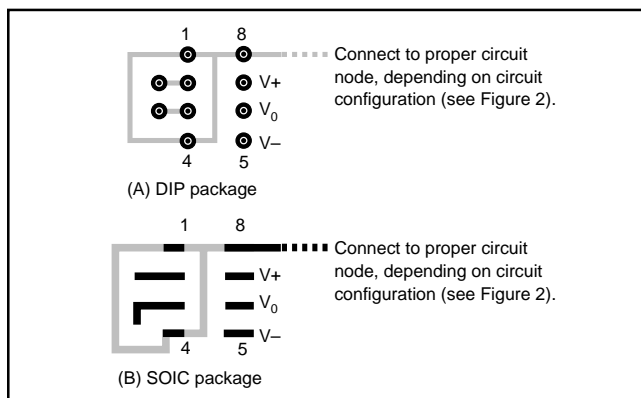


FIGURE 3. Suggested Board Layout for Input Guard.

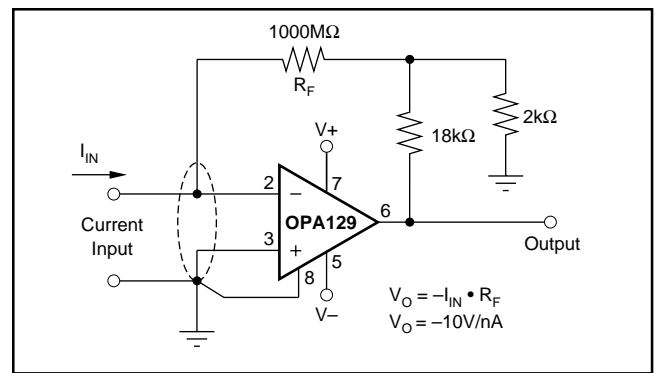


FIGURE 4. Current-to-Voltage Converter.

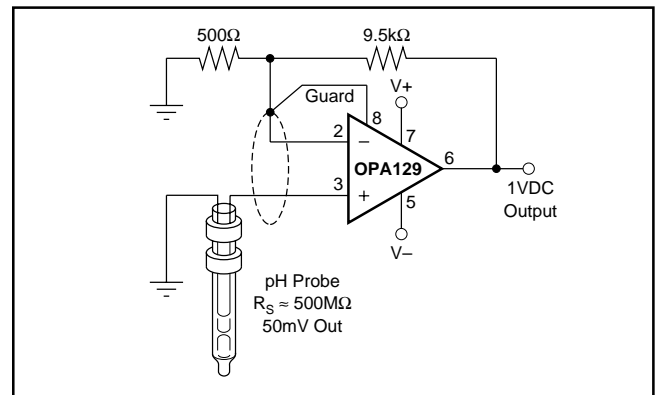


FIGURE 5. High Impedance ($10^{15}\Omega$) Amplifier.

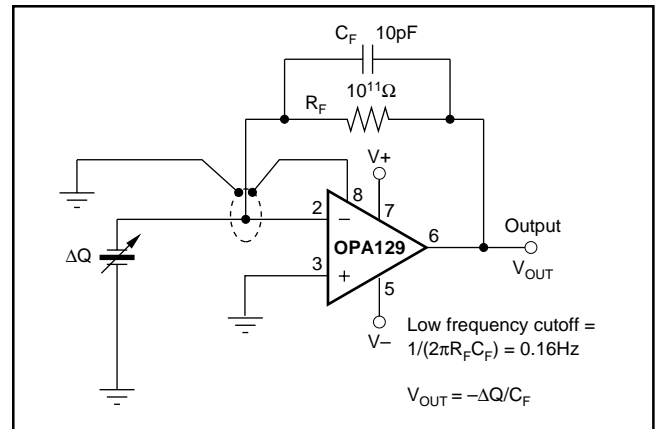


FIGURE 6. Piezoelectric Transducer Charge Amplifier.

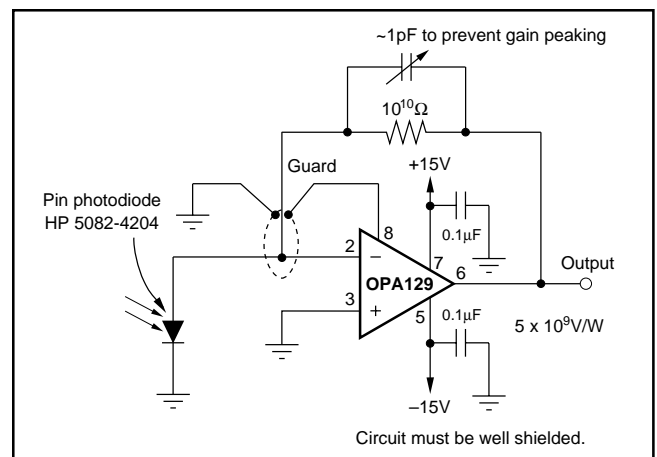


FIGURE 7. Sensitive Photodiode Amplifier.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA129U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 129U	Samples
OPA129UB	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 129U B	Samples
OPA129UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 129U B	Samples
OPA129UBE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 129U B	Samples
OPA129UBG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 129U B	Samples
OPA129UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 129U	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

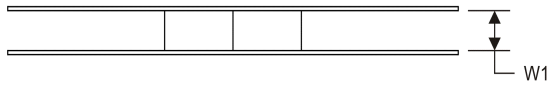
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA129UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA129UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.