TPL5110 用于电源门控的毫微功耗系统定时器

1 特性

- 电源电压范围：1.8V 至 5.5V
- 2.5V 电压下的电流消耗：35nA（典型值）
- 可选时间间隔范围：100ms 至 7200s
- 定时器精度：1%（典型值）
- 可通过电阻选择时间间隔
- 手动为 MOSFET 上电
- 单次触发功能

2 应用

- 电池供电系统
- 物联网 (IoT)
- 出入探测
- 篡改检测
- 家庭自动化传感器
- 温度调节装置
- 消费类电子产品
- 远程传感器
- 白色家电

3 说明

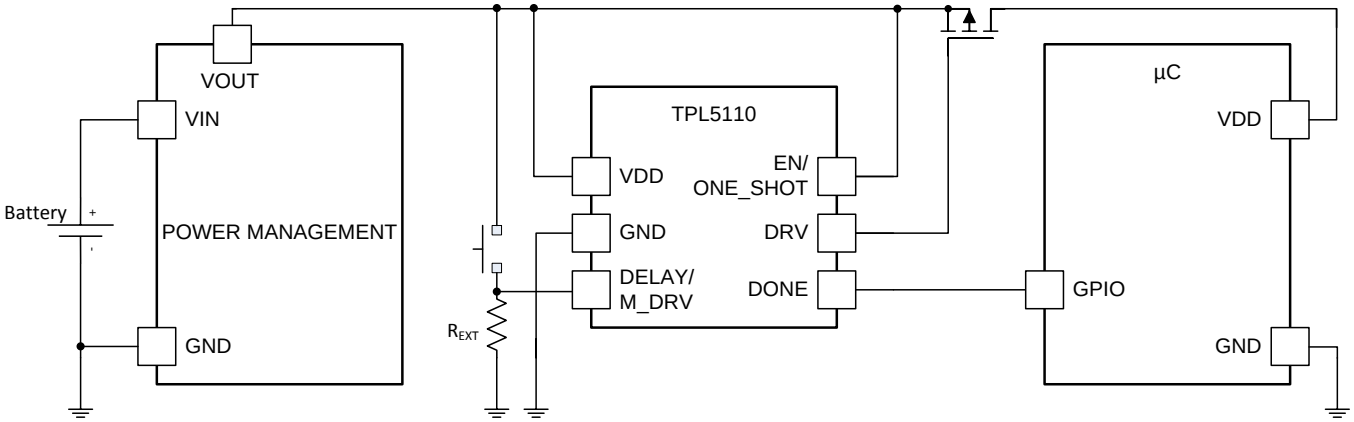
TPL5110 毫微定时器是一款集成 MOSFET 驱动器的低功耗系统定时器，非常适合占空比或电池供电类应用中的电源 门控。TPL5110 的流耗仅为 35nA，可用于启停电源线路，从而大幅降低休眠期间的总系统待机电流。这一节能特性可以明显缩小电池尺寸，因此 TPL5111 非常适合能量采集或无线传感器 应用。TPL5010 提供 100ms 至 7200s 的可选时间间隔，适用于电源门控 应用。此外，TPL5110 还具有独特的单次触发功能，可使定时器仅为 MOSFET 供电一个周期。TPL5110 采用 6 引脚小外形尺寸晶体管 (SOT23) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPL5110	SOT23 (6)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化应用电路原理图



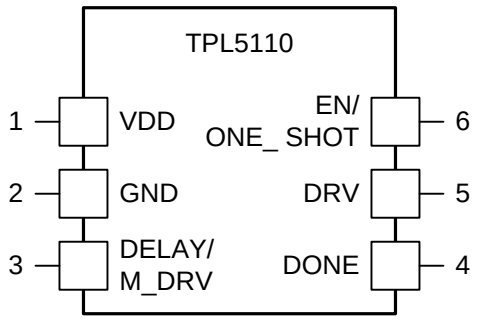
目录

5 修订历史记录

日期	修订版本	注释
2015 年 1 月	*	首次发布。

6 Pin Configuration and Functions

6-Lead
SOT-23
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VDD	P	Supply voltage	
2	GND	G	Ground	
3	DELAY/ M_DRV	I	Time interval set and manual MOSFET Power ON	Resistance between this pin and GND is used to select the time interval. The manual MOSFET power ON switch is also connected to this pin.
4	DONE	I	Logic Input for watchdog functionality	Digital signal driven by the µC to indicate successful processing.
5	DRV	O	Power Gating output signal generated every t_{IP}	The Gate of the MOSFET is connected to this pin. When DRV = LOW, the MOSFET is ON.
6	EN/ ONE_SHOT	I	Selector of mode of operation	When EN/ONE_SHOT = HIGH, the TPL5110 works as a TIMER. When EN/ONE_SHOT = LOW, the TPL5110 turns on the MOSFET one time for the programmed time interval. The next power on of the MOSFET is enabled by the manual power ON.

(1) G= Ground, P= Power, O= Output, I= Input.

7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	-0.3	6.0	V
Input Voltage at any pin(2)	-0.3	VDD + 0.3	V
Input Current on any pin	-5	+5	mA
Storage Temperature, T_{stg}	-65	150	°C
Junction Temperature, TJ(3)		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage between any two pins should not exceed 6V.
(3) The maximum power dissipation is a function of T_J(MAX), θJA, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = (T_J(MAX) - T_A)/ θJA. All numbers apply for packages soldered directly onto a PC board.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model, per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.5	V
Temperature Range	-40	105	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPL5110 SOT23 6 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	163	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	26	
$R_{θJB}$	Junction-to-board thermal resistance	57	
$ψ_{JT}$	Junction-to-top characterization parameter	7.5	
$ψ_{JB}$	Junction-to-board characterization parameter	57	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics(1)

Specifications are for T_A= 25°C, VDD-GND=2.5 V, unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY							
IDD	Supply current(4)	Operation mode			35	50	nA
		Digital conversion of external resistance (Rext)			200	400	µA
TIMER							
t_{IP}	Time interval Period	1650 selectable Time intervals	Min time interval		100		ms
			Max time interval		7200		s
	Time interval Setting Accuracy(5)	Excluding the precision of Rext			±0.6%		
	Time interval Setting Accuracy over supply voltage	1.8V ≤ VDD ≤ 5.5V			±25		ppm/V
t_{OSC}	Oscillator Accuracy			-0.5%		0.5%	
	Oscillator Accuracy over temperature(6)	-40°C ≤ T_A≤ 105°C			±100	±400	ppm/°C
	Oscillator Accuracy over supply voltage	1.8V ≤ VDD ≤ 5.5V			±0.4		%/V
	Oscillator Accuracy over life time(7)				±0.24%		
t_{DONE}	DONE Pulse width (6)			100			ns
t_{DRV}	DRV Pulse width	DONE signal not received			t_{IP}- 50ms		
t_Rext	Time to convert Rext				100	120	ms
DIGITAL LOGIC LEVELS							
VIH	Logic High Threshold DONE pin			0.7xVDD			V
VIL	Logic Low Threshold DONE pin					0.3xVDD	V
VOH	Logic output High Level DRV pin	Iout = 100 µA		VDD-0.3			V
		Iout = 1 mA		VDD-0.7			V
VOL	Logic output Low Level DRV pin	Iout = -100 µA				0.3	V
		Iout = -1 mA				0.7	V
VIH_{M_DRV}	Logic High Threshold DELAY/M_DRV pin			1.5			V

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current excludes load and pull-up resistor current. Input pins are at GND or VDD.
(5) The accuracy for time interval settings below 1second is ±100ms.
(6) This parameter is specified by design and/or characterization and is not tested in production.
(7) Operational life time test procedure equivalent to10 years.

7.6 Timing Requirements

			MIN(1)	NOM(2)	MAX(1)	UNIT
tr_{DRV}	Rise Time DRV(3)	Capacitive load 50 pF		50		ns
tf_{DRV}	Fall Time DRV(3)	Capacitive load 50 pF		50		ns
tD_{DONE}	DONE to DRV delay	Min delay(4)		100		ns
		Max delay (4)		t_{DRV}		
t_{M_DRV}	Valid manual MOSFET Power ON	Observation time 30ms	20			ms
t_{DB}	De-bounce manual MOSFET Power ON			20		ms

(1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) This parameter is specified by design and/or characterization and is not tested in production.
(4) from DRV falling edge.

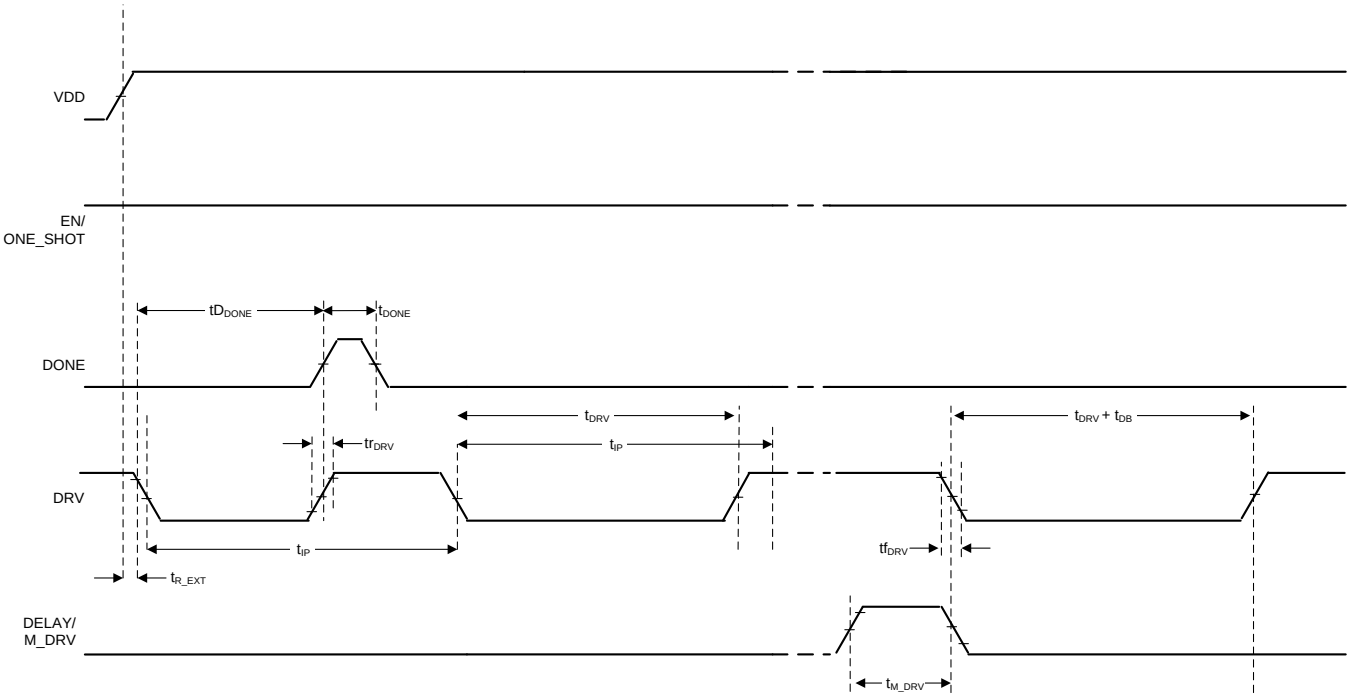


Figure 1. TPL5110 Timing

7.7 Typical Characteristics

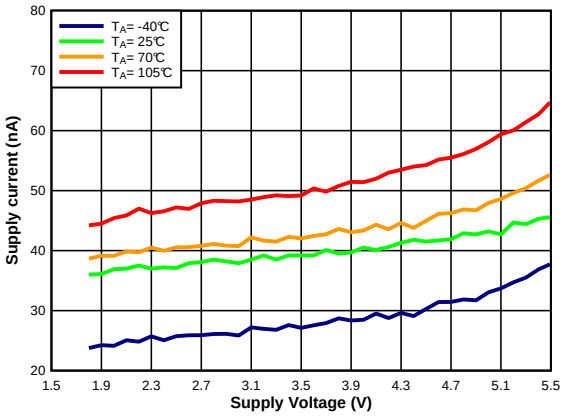


Figure 2. I_{DD} vs. V_{DD}

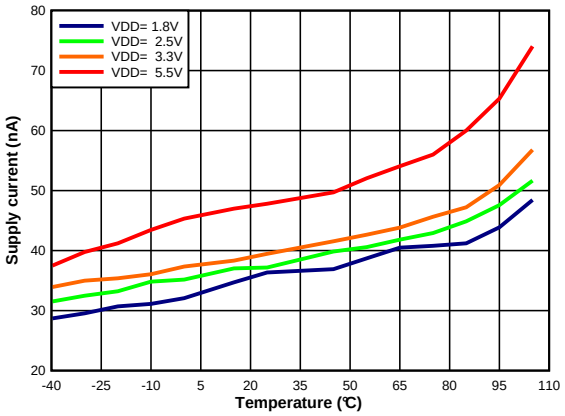


Figure 3. I_{DD} vs. Temperature

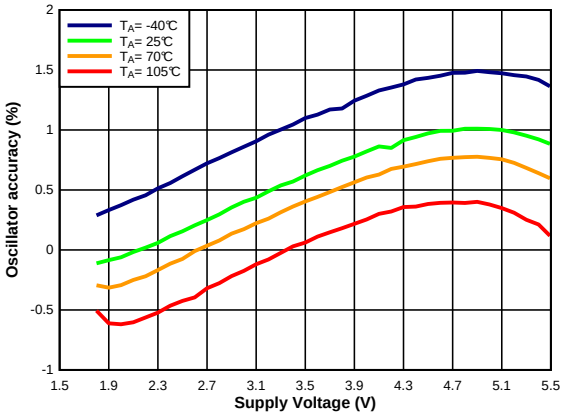


Figure 4. Oscillator Accuracy vs. V_{DD}

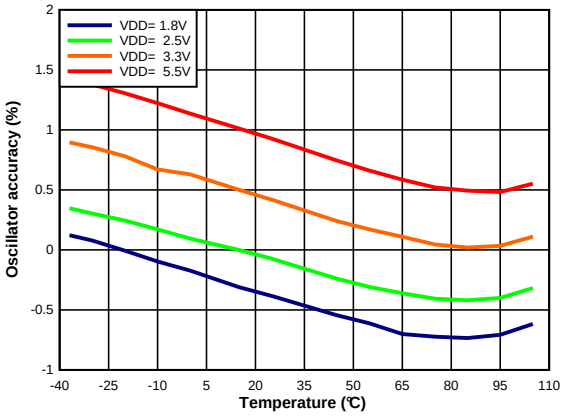


Figure 5. Oscillator Accuracy vs. Temperature

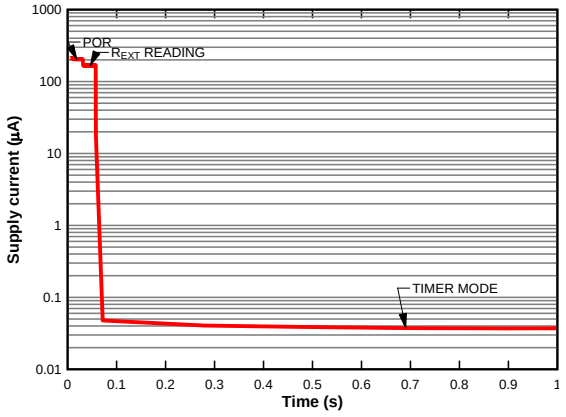
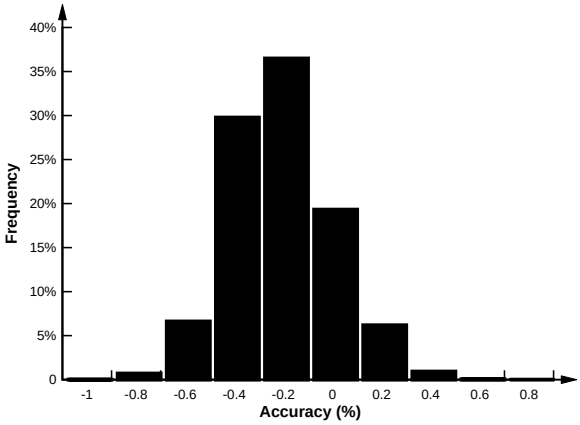


Figure 6. I_{DD} vs. Time



number of observations >20000

1s < t_{IP} ≤ 7200s

Figure 7. Time interval Setting Accuracy

8 Detailed Description

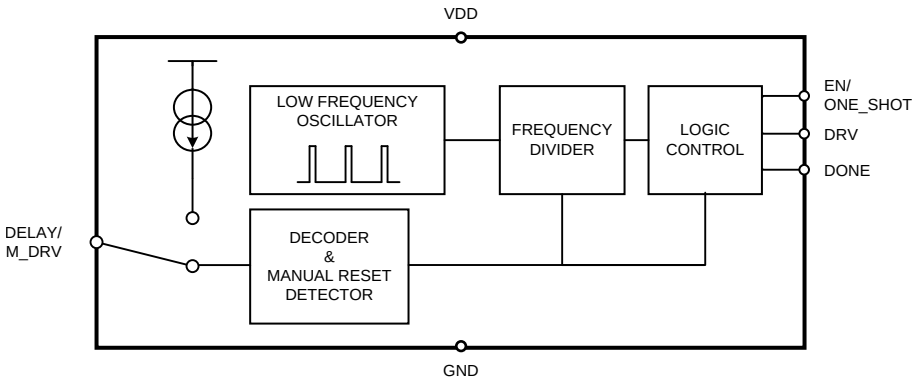
8.1 Overview

The TPL5110 is a timer with power gating feature. It is ideal for use in power-cycled applications and provides selectable timing from 100ms to 7200s.

Once configured in timer mode (EN/ONE_SHOT= HIGH) the TPL5110 periodically sends out a DRV signal to a MOSFET to turn on the µC. If the µC replies with a DONE signal within the programmed time interval (t_{DRV}) the TPL5110 turns off the µC, otherwise the TPL5110 keeps the µC in the on state for a time equal to t_{DRV}.

The TPL5110 can work also in a one shot mode (EN/ONE_SHOT= LOW). In this mode the DRV signal is sent out just one time at the power on of the TPL5110 to turn on the µC. If the µC replies with a DONE signal within the programmed time interval (t_{DRV}) the TPL5110 turns off the µC, otherwise the TPL5110 keeps the µC in the on state for a time equal to t_{DRV}.

8.2 Functional Block Diagram



8.3 Feature Description

The TPL5110 implements a periodical power gating feature or one shot power gating according to the EN/ONE_SHOT voltage. A manual MOSFET Power ON function is realized by momentarily pulling the DELAY/M_DRV pin to VDD.

8.3.1 DRV

The gate of the MOSFET is connected to the DRV pin. When DRV= LOW, the MOSFET is turned ON. The pulse generated at DRV is equal to the selected time interval period, minus 50ms. It is shorter in the case of a DONE signal received from the µC. If the DONE signal is not received within the programmed time interval (minus 50ms), the DRV signal will be high for the last 50ms of the time interval in order to turn off the MOSFET before the next cycle starts.

The default value (after resistance reading) is HIGH. The signal is sent out from the TPL5110 when the programmed time interval starts. When the DRV is LOW, the manual power ON signal is ignored.

8.3.2 DONE

The DONE pin is driven by a µC to signal that the µC is working properly. The TPL5110 recognizes a valid DONE signal as a low to high transition; if two or more DONE signals are received within the time interval, only the first DONE signal is processed. The minimum DONE signal pulse length is 100ns. When the TPL5110 receives the DONE signal it asserts DRV logic HIGH.

8.4 Device Functional Modes

8.4.1 Startup

During startup, after POR, the TPL5110 executes a one-time measurement of the resistance attached to the DELAY/M_DRV pin in order to determine the desired time interval for DRV. This measurement interval is t_{R_EXT}. During this measurement a constant current is temporarily flowing into R_{EXT}.

Once the reading of the external resistance is completed the TPL5110 enters automatically in one of the 2 modes according to the EN/ONE_SHOT value.The EN/ONE_SHOT pin needs to be hard wired to GND or VDD according to the required mode of operation.

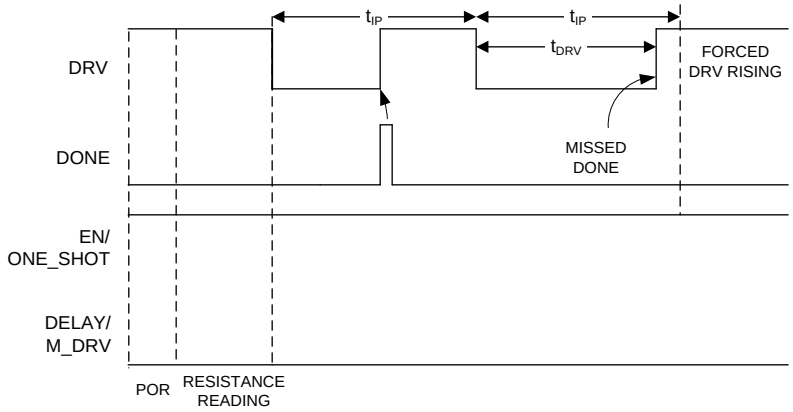


Figure 8. Startup - Timer mode

8.4.2 Timer Mode

During timer mode (EN/ONE_SHOT = HIGH), the TPL5110 asserts periodic DRV pulses according to the programmed time interval. The length of the DRV pulses is set by the receiving of a DONE pulse from the uC. See Figure 8.

8.4.3 One Shot Mode

During One shot mode (EN/ONE_SHOT = LOW), the TPL5110 generates just one pulse at the DRV pin which lasts according to the programmed time interval. In one-shot mode, other DRV pulses can be triggered using the DELAY/M_DRV pin. If a valid manual power ON occurs when EN/ONE_SHOT is LOW, the TPL5110 generates just one pulse at the DRV pin. The duration of the pulse is set by the programmed time interval. Also in this case, if a DONE signal is received within the programmed time interval (minus 50ms), the MOSFET connected to the DRV pin is turned off. See Figure 9 and Figure 10.

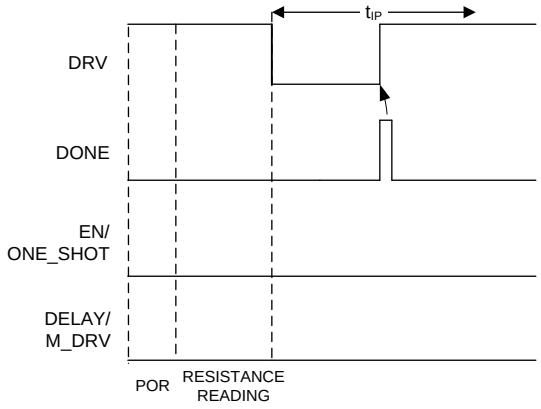


Figure 9. Startup One Shot Mode, (DONE received within t_{IP})

Device Functional Modes (continued)

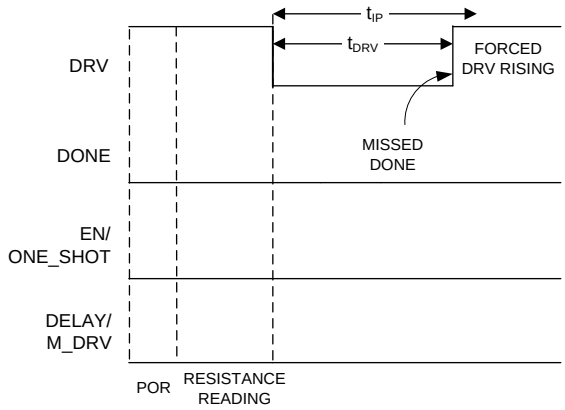


Figure 10. Startup One Shot Mode, (no DONE received within t_{IP})

8.5 Programming

8.5.1 Configuring the Time Interval with the DELAY/M_DRV Pin

The time interval between 2 adjacent DRV pulses (falling edges, in timer mode) is selectable through an external resistance (R_{EXT}) between the DELAY/M_DRV pin and ground. The resistance (R_{EXT}) must be in the range between 500Ω and 170kΩ. At least a 1% precision resistance is recommended. See section *Selection of the External Resistance* on how to set the time interval using R_{EXT}.

8.5.2 Manual MOSFET Power ON Applied to the DELAY/M_DRV Pin

If VDD is connected to the DELAY/M_DRV pin, the TPL5110 recognizes this as a manual MOSFET Power ON condition. In this case the time interval is not set. If the manual MOSFET Power ON is asserted during the POR or during the reading procedure, the reading procedure is aborted and is re-started as soon as the manual MOSFET Power ON switch is released. A pulse on the DELAY/M_DRV pin is recognized as a valid manual MOSFET Power ON only if it lasts at least 20ms (observation time is 30ms). The manual MOSFET Power ON may be implemented using a switch (momentary mechanical action).

If the DRV is already LOW (MOSFET ON) the manual MOSFET Power ON is ignored.

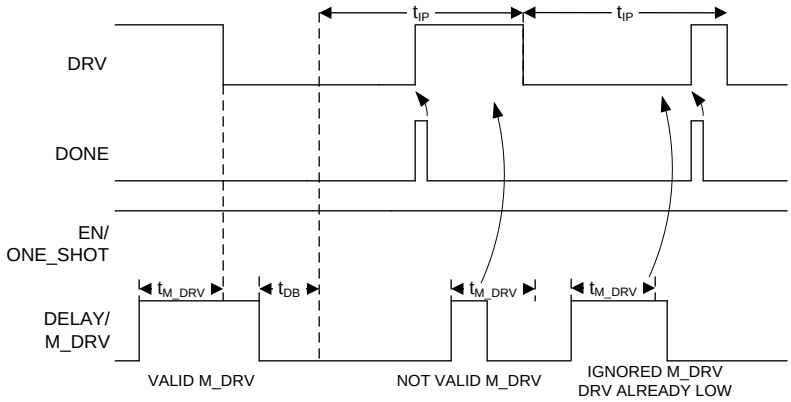


Figure 11. Manual MOSFET Power ON in Timer Mode

Programming (continued)

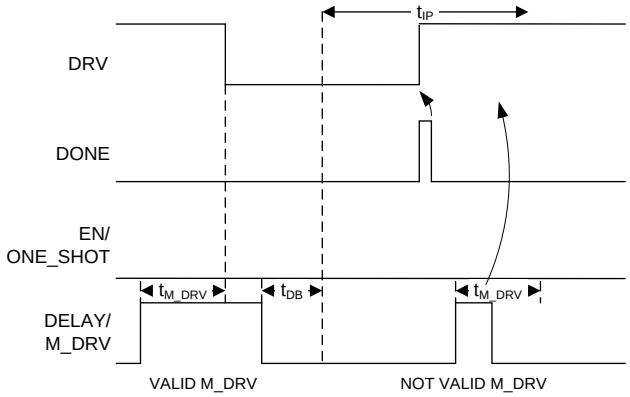


Figure 12. Manual MOSFET Power ON in One Shot Mode

8.5.2.1 DELAY/M_DRV

A resistance in the range between 500Ω and 170kΩ must to be connected to the DELAY/M_DRV pin in order to select a valid time interval. At the POR and during the reading of the resistance, the DELAY/M_DRV is connected to an analog signal chain through a mux. After the reading of the resistance, the analog circuit is switched off and the DELAY/M_DRV is connected to a digital circuit.

In this state, a logic HIGH applied to the DELAY/M_DRV pin is interpreted by the TPL5110 as a manual power ON. The manual power ON detection is provided with a de-bounce feature (on both edges) which makes the TPL5110 insensitive to the glitches on the DELAY/M_DRV.

The M_DRV must stay high for at least 20ms to be valid. Once a valid signal at DELAY/M_DRV is understood as a manual power on, the DRV signal will be asserted in the next 10ms. Its duration will be according to the programmed time interval (minus 50ms), or less if the DONE is received.

A manual power ON signal resets all the counters. The counters will restart as soon as a valid manual power ON signal is recognized and the signal at DELAY/M_DRV pin is asserted LOW. Due to the asynchronous nature of the manual power ON signal and its arbitrary duration, the LOW status of the DRV signal may be affected by an uncertainty of about ±5ms.

An extended assertion of a logic HIGH at the DELAY/M_DRV pin will turn on the MOSFET for a time longer than the programmed time interval. DONE signals received while the DELAY/M_DRV is HIGH are ignored. If the DRV is already LOW (MOSFET ON) the manual power ON is ignored.

8.5.2.2 Circuitry

The manual Power ON may be implemented using a switch (momentary mechanical action). The TPL5110 offers 2 possible approaches according to the power consumption constraints of the application.

Programming (continued)

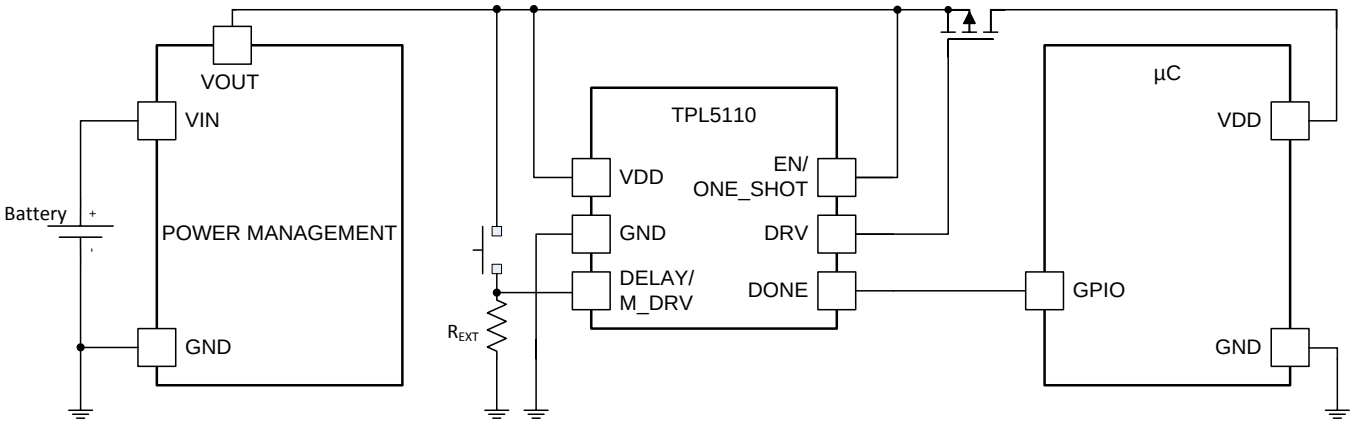


Figure 13. Manual MOSFET Power ON with SPST Switch

For use cases that do not require the lowest power consumption, using a single pole single throw switch may offer a lower cost solution. The DELAY/M_DRV pin may be directly connected to VDD with R_{EXT} in the circuit. The current drawn from the supply voltage during the manual power ON is given by VDD/R_{EXT}.

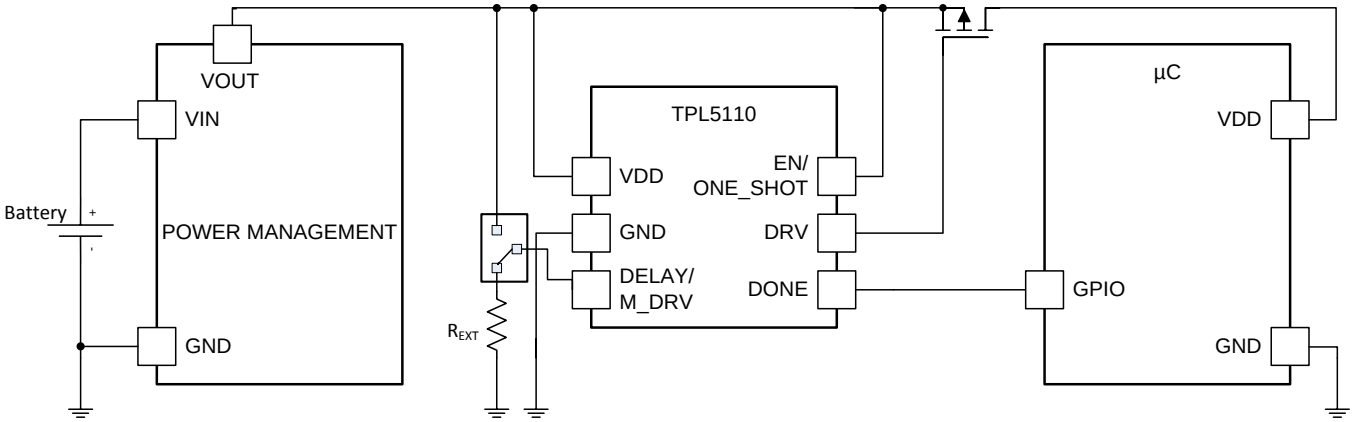


Figure 14. Manual MOSFET Power ON with SPDT Switch

The manual MOSFET Power ON function may also be asserted by switching DELAY/M_DRV from R_{EXT} to VDD using a single pole double throw switch, which will provide a lower power solution for the manual power ON, because no current flows.

8.5.3 Selection of the External Resistance

In order to set the time interval, the external resistance R_{EXT} is selected according the following formula:

$$R_{EXT} = 100 \left(\frac{-b + \sqrt{b^2 - 4a\left(c - 100\,T\right)}}{2a} \right) \quad (1)$$

Where:

- **T** is the desired time interval in seconds.
- **R_{EXT}** is the resistance value to use in Ω.
- **a**,**b**,**c** are coefficients depending on the range of the time interval.

Programming (continued)

Table 1. Coefficients for Equation 1

SET	Time Interval Range (s)	a	b	c
1	1 <T≤ 5	0.2253	-20.7654	570.5679
2	5 <T≤ 10	-0.1284	46.9861	-2651.8889
3	10 <T≤ 100	0.1972	-19.3450	692.1201
4	100 <T≤ 1000	0.2617	-56.2407	5957.7934
5	T> 1000	0.3177	-136.2571	34522.4680

EXAMPLE

Required time interval: 8s

The coefficient set to be selected is the number 2. The formula becomes

$$R_{EXT}=100\left(\frac{46.9861-\sqrt{46.9861^2+4*0.1284\left(-2561.8889-100*8\right)}}{2*0.1284}\right) \quad (2)$$

The resistance value is 10.18 kΩ.

The following Look-Up-Tables contain example values of t_{IP} and their corresponding value of R_{EXT}.

Table 2. First 9 Time Intervals

t_{IP} (ms)	Resistance (Ω)	Closest real value (Ω)	Parallel of two 1% tolerance resistors, (kΩ)
100	500	500	1.0 // 1.0
200	1000	1000	-
300	1500	1500	2.43 // 3.92
400	2000	2000	-
500	2500	2500	4.42 // 5.76
600	3000	3000	5.36 // 6.81
700	3500	3500	4.75 // 13.5
800	4000	4000	6.19 // 11.3
900	4500	4501	6.19 // 16.5

Table 3. Most Common Time Intervals Between 1s to 2h

t_{IP}	Calculated Resistance (kΩ)	Closest Real Value (kΩ)	Parallel of Two 1% Tolerance Resistors,(kΩ)
1s	5.20	5.202	7.15 // 19.1
2s	6.79	6.788	12.4 // 15.0
3s	7.64	7.628	12.7// 19.1
4s	8.30	8.306	14.7 // 19.1
5s	8.85	8.852	16.5 // 19.1
6s	9.27	9.223	18.2 // 18.7
7s	9.71	9.673	19.1 // 19.6
8s	10.18	10.180	11.5 // 8.87
9s	10.68	10.68	17.8 // 26.7
10s	11.20	11.199	15.0 // 44.2
20s	14.41	14.405	16.9 // 97.6
30s	16.78	16.778	32.4 // 34.8
40s	18.75	18.748	22.6 // 110.0
50s	20.047	20.047	28.7 // 66.5

Table 3. Most Common Time Intervals Between 1s to 2h (continued)

t_{IP}	Calculated Resistance (kΩ)	Closest Real Value (kΩ)	Parallel of Two 1% Tolerance Resistors,(kΩ)
1min	22.02	22.021	40.2 // 48.7
2min	29.35	29.349	35.7 // 165.0
3min	34.73	34.729	63.4 // 76.8
4min	39.11	39.097	63.4 // 102.0
5min	42.90	42.887	54.9 // 196.0
6min	46.29	46.301	75.0 // 121.0
7min	49.38	49.392	97.6 // 100.0
8min	52.24	52.224	88.7 // 127.0
9min	54.92	54.902	86.6 // 150.0
10min	57.44	57.437	107.0 // 124.0
20min	77.57	77.579	140.0 // 174.0
30min	92.43	92.233	182.0 // 187.0
40min	104.67	104.625	130.0 // 536.00
50min	115.33	115.331	150.0 // 499.00
1h	124.91	124.856	221.0 // 287.00
1h30min	149.39	149.398	165.0 // 1580.0
2h	170.00	170.00	340.0 // 340.0

8.5.4 Quantization Error

The TPL5110 can generate 1650 discrete timer intervals in the range of 100ms to 7200s. The first 9 intervals are multiples of 100ms. The remaining 1641 intervals cover the range between 1s to 7200s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to the following formula:

$$Err = 100\frac{\left(T_{DESIRED} - T_{ADC}\right)}{T_{DESIRED}} \tag{3}$$

Where:

$$T_{ADC} = INT\left[\frac{1}{100}\left(a\frac{R_D^{\,2}}{100^{\,2}} + b\frac{R_D}{100} + c\right)\right] \tag{4}$$

$$R_D = INT\left[\frac{R_{EXT}}{100}\right] \tag{5}$$

R_{EXT} is the resistance calculated with Equation 1 and a,b,c are the coefficients of the equation listed in Table 1.

8.5.5 Error Due to Real External Resistance

R_{EXT} is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical R_{EXT} using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of R_{EXT} (R_{EXT_MIN}, R_{EXT_MAX} with Equation 1 using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC\_MIN}[R_{EXT\_MIN}]$, $T_{ADC\_MAX}[R_{EXT\_MAX}]$) with Equation 4.
3. Find the errors using Equation 3 with T_{ADC_MIN}, T_{ADC_MAX}.

The results of the formula indicate the accuracy of the time interval.

The example below illustrates the procedure.

- Desired time interval , T_desired = 600s,

- Required R_{EXT}, from Equation 1, R_{EXT}= 57.44kΩ.

From Table 3 R_{EXT} can be built with a parallel combination of two commercial values with 1% tolerance: R1=107kΩ, R2=124kΩ. The uncertainty of the equivalent parallel resistance can be found using:

$$uR_{//} = R_{//}\sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2} \quad (6)$$

Where uRn (n=1,2) represent the uncertainty of a resistance,

$$u_{Rn} = Rn\frac{Tolerance}{\sqrt{3}} \quad (7)$$

The uncertainty of the parallel resistance is 0.82%, meaning the value of R_{EXT} may range between R_{EXT_MIN} = 56.96 kΩ and R_{EXT_MAX} = 57.90 kΩ.

Using these value of R_{EXT}, the digitized timer intervals calculated with Equation 4 are respectively T_{ADC_MIN} = 586.85 s and T_{ADC_MAX} = 611.3 s, giving an error range of -1.88% / +2.19%. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In battery powered applications one design constraint is the need for low current consumption. The TPL5110 is suitable in applications where there is a need to monitor environmental conditions at a fixed time interval. Often in these applications a watchdog or other internal timer in a µC is used to implement a wakeup function. Typically, the power consumption of these functions is not optimized. Using the TPL5110 to implement a periodical power gating of the µC or of the entire system the current consumption will be only tens of nA.

9.2 Typical Application

The TPL5110 can be used in environment sensor nodes such as humidity and temperature sensor node. The sensor node has to measure the humidity and the temperature and transmit the data through a low power RF micro such as the CC2531. Since the temperature and the humidity in home application do not change so fast, the measurement and the transmission of the data can be done at very low rate, such as every 30 seconds. The RF micro should spend most of the time in counting the elapsed time, but using the TPL5110 it is possible to complete turn off the RF micro and extend the battery life. The TPL5110 will turn on the RF micro when the programmed time interval elapses or for debug purpose with the manual MOSFET Power ON switch.

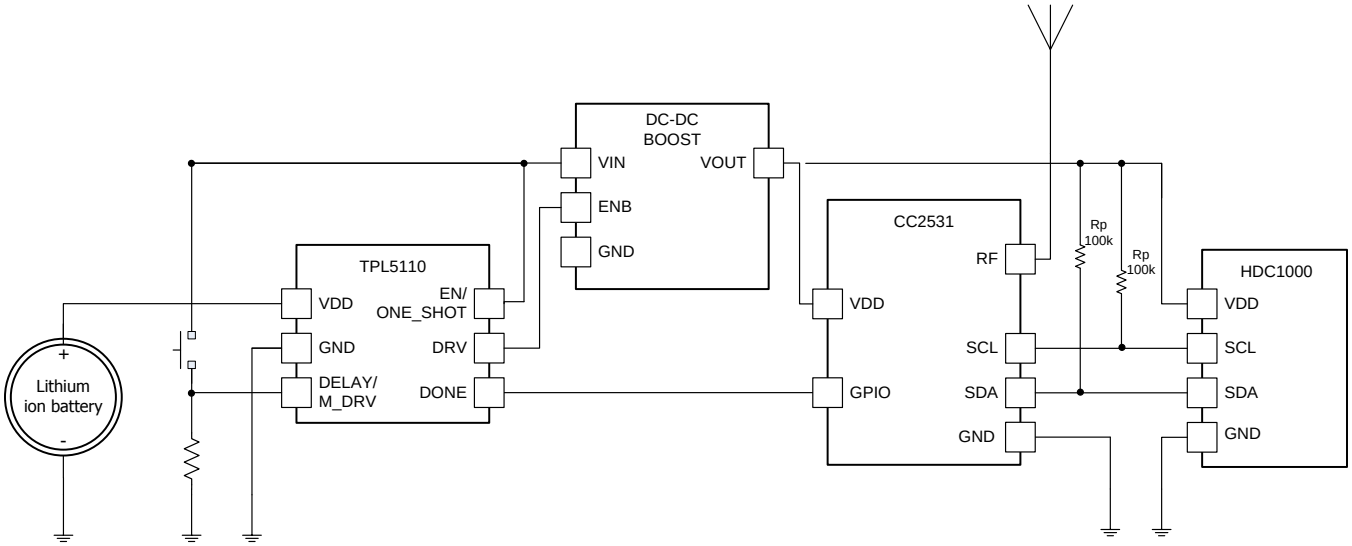


Figure 15. Sensor Node

9.2.1 Design Requirements

The Design is driven by the low current consumption constraint. The data are usually acquired on a rate which is in the range between 30s and 60s. The highest necessity is the maximization of the battery life. The TPL5110 helps achieve this goal because it allows turning off the RF micro.

9.2.2 Detailed Design Procedure

When the focal constraint is the battery life, the selection of a low power voltage regulator and low leakage MOSFET to power gate the µC is mandatory. The first step in the design is the calculation of the power consumption of each device in the different mode of operations. An example is the HDC1000, in measurement mode the RF micro is in normal operation and transmission. The different modes offer the possibility to select the appropriate time interval which respect the application constraint and maximize the life of the battery.

Typical Application (continued)

9.2.3 Application Curves

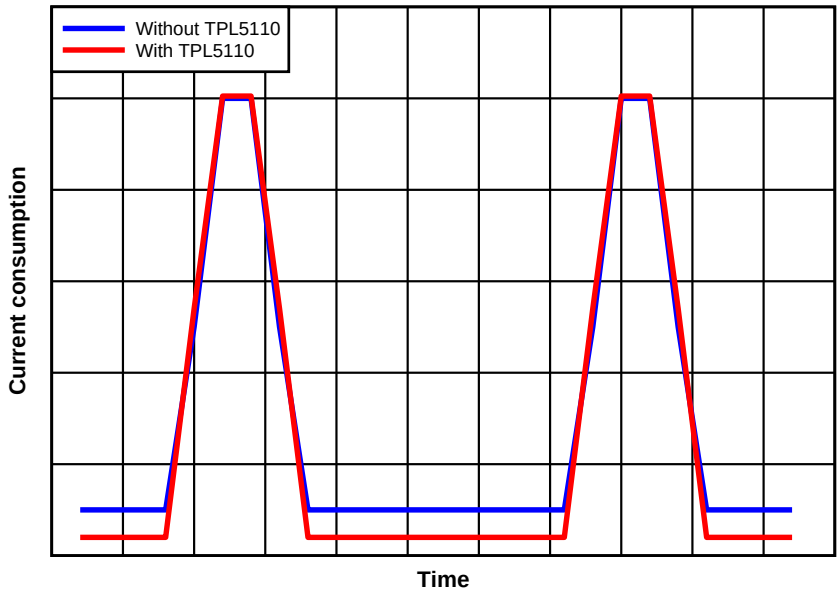


Figure 16. Effect of TPL5110 on Current Consumption

10 Power Supply Recommendations

The TPL5110 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1µF between VDD and GND pin is recommended.

11 Layout

11.1 Layout Guidelines

The DELAY/M_DRV pin is sensitive to parasitic capacitance. It is suggested that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the DRV pin is also improved by keeping the trace length between the TPL5110 and the gate of the MOSFET short to reduce the parasitic capacitance. The EN/ONE_SHOT needs to be tied to GND or VDD with short traces.

11.2 Layout Example

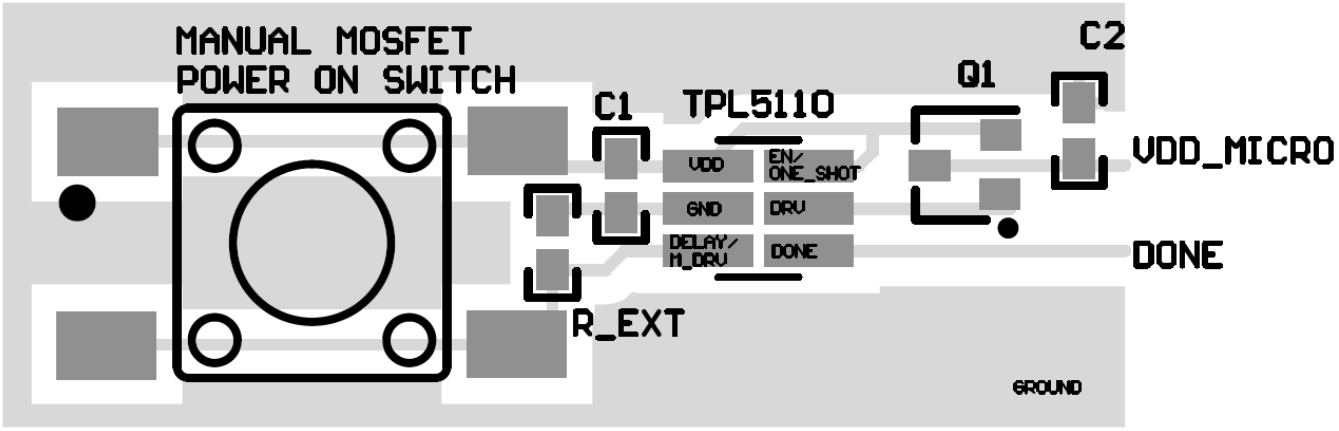


Figure 17. Layout

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL5110DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZALX	Samples
TPL5110DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZALX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

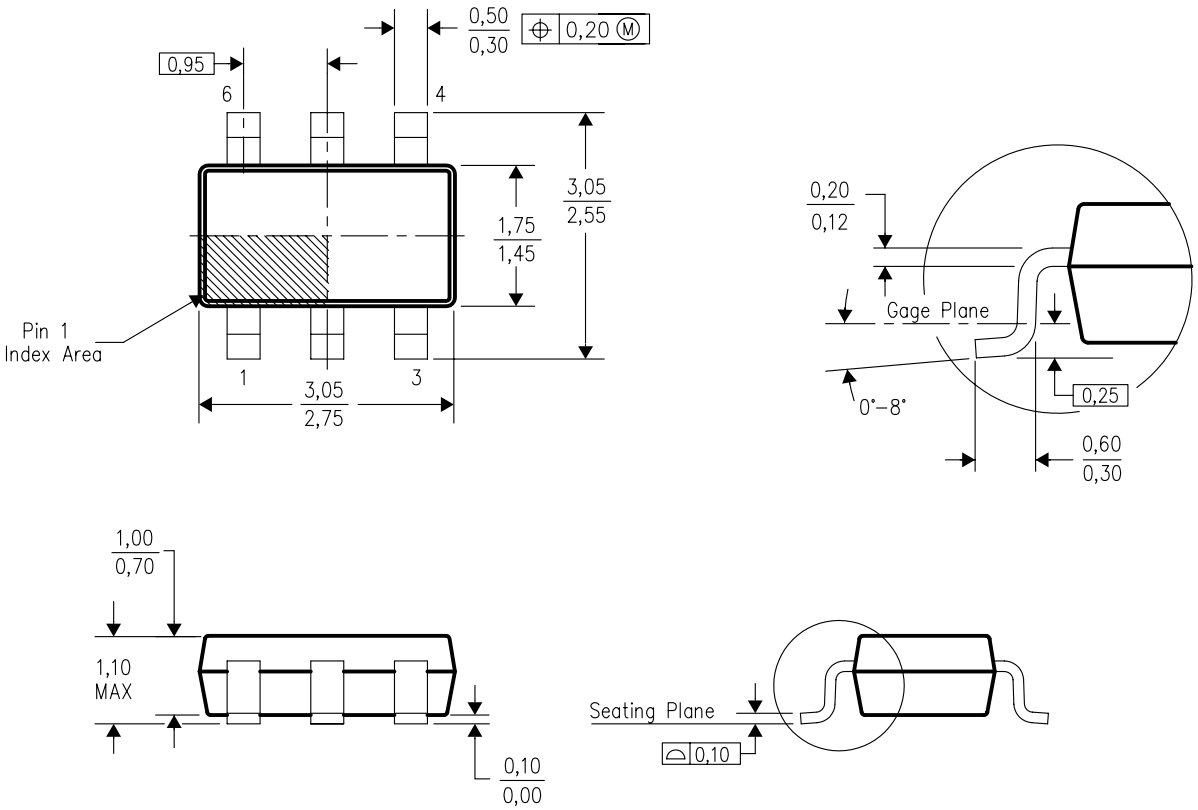
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

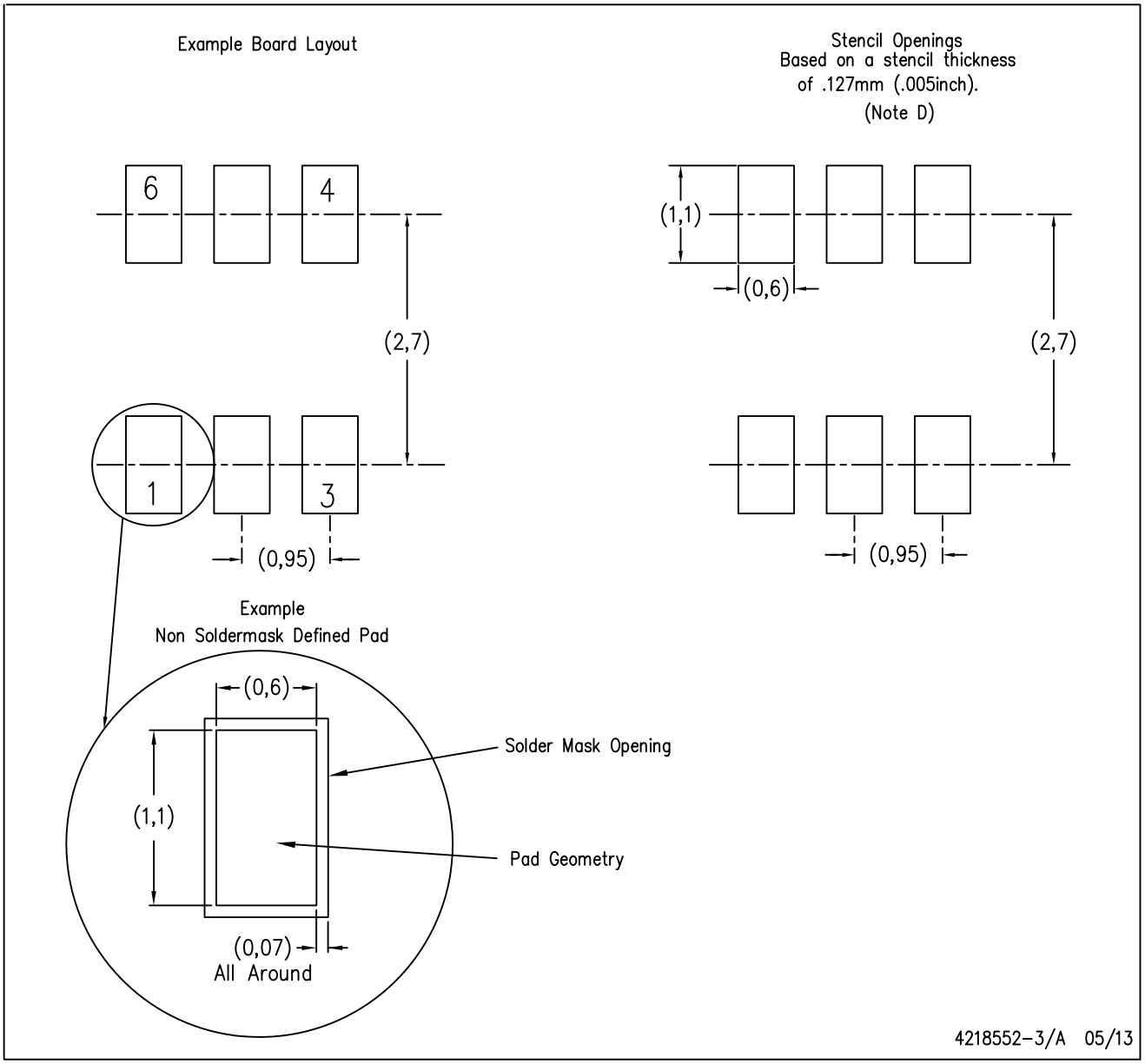
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (http://www.ti.com/sc/docs/stdterms.htm) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权 负责并确保 应用的安全性， 及设计人员的 应用 （包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的 应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何 应用前， 将彻底测试该等 应用和 该等应用中所用 TI 产品的 功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用， 如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122