

## TLV370x Family of Nanopower, Push-Pull Output Comparators

### 1 Features

- Low Supply Current ... 560 nA/Per Channel
- Input Common-Mode Range Exceeds the Rails ...  $-0.1\text{ V}$  to  $V_{CC} + 5\text{ V}$
- Supply Voltage Range ... 2.5 V to 16 V
- Reverse Battery Protection Up to 18 V
- Push-Pull CMOS Output Stage
- Specified Temperature Range
  - $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  – Commercial Grade
  - $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  – Industrial Grade
- Ultra-Small Packaging
  - 5-Pin SOT-23 (TLV3701)
  - 8-Pin MSOP (TLV3702)
- Universal Op-Amp EVM (Reference SLOU060 for More Information)

### 2 Applications

- Portable Battery Monitoring
- Consumer Medical Electronics
- Security Detection Systems
- Handheld Instruments
- Ultra-Low Power Systems

### 3 Description

The TLV370x is Texas Instruments' first family of nanopower comparators with only 560 nA per channel supply current, which make this device ideal for battery power and wireless handset applications.

The TLV370x has a minimum operating supply voltage of 2.7 V over the extended industrial temperature range ( $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ), while having an input common-mode range of  $-0.1$  to  $V_{CC} + 5\text{ V}$ . The low supply current makes it an ideal choice for battery-powered portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an overcurrent condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

#### Device Information<sup>(1)</sup>

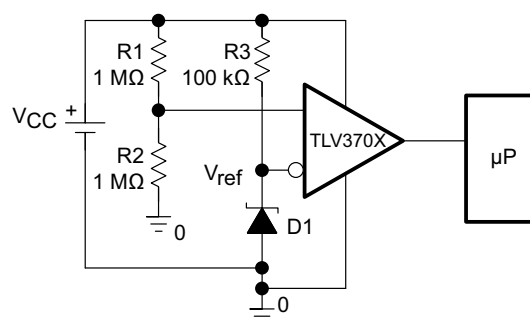
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV3701	SOT-23 (5)	2.90 mm x 1.60 mm
	SOIC (8)	4.90 mm x 3.91 mm
TLV3702	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	PDIP (8)	9.81 mm x 6.35 mm
TLV3704	SOIC (14)	8.65 mm x 3.91 mm
	PDIP (14)	19.30 mm x 6.35 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Supply Current vs Supply Voltage



#### High-Side Voltage Sense Circuit



Copyright © 2016, Texas Instruments Incorporated



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.3 Feature Description.....	<b>13</b>
<b>2 Applications</b> .....	<b>1</b>	8.4 Device Functional Modes.....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>14</b>
<b>4 Revision History</b> .....	<b>2</b>	9.1 Application Information.....	<b>14</b>
<b>5 Device Comparison Tables</b> .....	<b>3</b>	9.2 Typical Application .....	<b>14</b>
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>16</b>
<b>7 Specifications</b> .....	<b>6</b>	<b>11 Layout</b> .....	<b>16</b>
7.1 Absolute Maximum Ratings .....	<b>6</b>	11.1 Layout Guidelines .....	<b>16</b>
7.2 Recommended Operating Conditions .....	<b>6</b>	11.2 Layout Example .....	<b>16</b>
7.3 Thermal Information – TLV3701 .....	<b>7</b>	<b>12 Device and Documentation Support</b> .....	<b>17</b>
7.4 Thermal Information – TLV3702 .....	<b>7</b>	12.1 Device Support.....	<b>17</b>
7.5 Thermal Information – TLV3704 .....	<b>7</b>	12.2 Documentation Support .....	<b>17</b>
7.6 Electrical Characteristics.....	<b>8</b>	12.3 Related Links .....	<b>17</b>
7.7 Switching Characteristics .....	<b>9</b>	12.4 Receiving Notification of Documentation Updates	<b>17</b>
7.8 Dissipation Ratings .....	<b>9</b>	12.5 Community Resources.....	<b>18</b>
7.9 Typical Characteristics .....	<b>10</b>	12.6 Trademarks .....	<b>18</b>
<b>8 Detailed Description</b> .....	<b>13</b>	12.7 Electrostatic Discharge Caution.....	<b>18</b>
8.1 Overview .....	<b>13</b>	12.8 Glossary .....	<b>18</b>
8.2 Functional Block Diagram .....	<b>13</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>18</b>

## 4 Revision History

<b>Changes from Revision C (March 2017) to Revision D</b>	<b>Page</b>
• Changed Wording of Start-up time table note .....	<b>9</b>

<b>Changes from Revision B (August 2001) to Revision C</b>	<b>Page</b>
• Added <i>Device Information</i> table, <i>Device Comparison</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	<b>1</b>
• Changed VOH typical value from 0.08 to 80 to reflect proper units.....	<b>8</b>
• Changed Dissipation Ratings Table to reflect new package thermals.....	<b>9</b>
• Deleted extraneous "Open Collector Leakage" graph.....	<b>10</b>

## 5 Device Comparison Tables

**Table 1. Selection of Comparators<sup>(1)</sup>**

DEVICE	V <sub>CC</sub> (V)	V <sub>IO</sub> (μV)	I <sub>CC</sub> /Ch (μA)	I <sub>B</sub> (pA)	t <sub>PLH</sub> (μs)	t <sub>PHL</sub> (μs)	t <sub>r</sub> (μs)	t <sub>f</sub> (μs)	RAIL-TO-RAIL	OUTPUT STAG E
TLV370x	2.5 – 16	250	0.56	80	56	83	22	8	I	PP
TLV340x	2.5 – 16	250	0.47	80	55	30	5	—	I	OD
TLC3702/4	3 – 16	1200	9	5	1.1	0.65	0.5	0.125	—	PP
TLC393/339	3 – 16	1400	11	5	1.1	0.55	0.22	—	—	OD
TLC372/4	3 – 16	1000	75	5	0.65	0.65	—	—	—	OD

(1) All specifications are typical values measured at 5 V.

**Table 2. TLV3701 Available Options**

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D) <sup>(1)</sup>	SOT-23 (DBV) <sup>(2)</sup>	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	5000 μV	TLV3701CD	TLV3701CDBV	VBCC	—
–40°C to 125°C		TLV3701ID	TLV3701IDBV	VBCI	TLV3701IP

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV3701CDR).

(2) This package is only available taped and reeled. For standard quantities (3000 pieces per reel), add an R suffix (that is, TLV3701CDBVR). For small quantities (250 pieces per mini-reel), add a T suffix to the part number (for example, TLV3701CDBVT).

**Table 3. TLV3702 Available Options**

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D) <sup>(1)</sup>	MSOP (DGK)	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	5000 μV	TLV3702CD	TLV3702CDGK	xxTIAKC	—
–40°C to 125°C		TLV3702ID	TLV3702IDGK	xxTIAKD	TLV3702IP

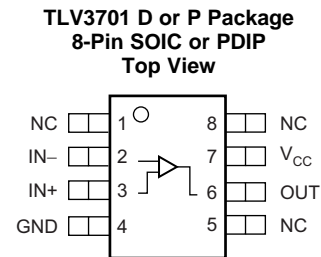
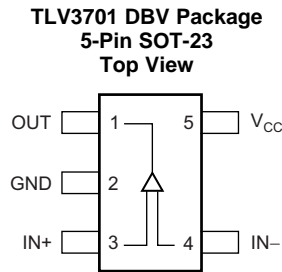
(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV3702CDR).

**Table 4. TLV3704 Available Options**

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D) <sup>(1)</sup>	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	5000 μV	TLV3704CD	—	TLV3704CPW
–40°C to 125°C		TLV3704ID	TLV3704IN	TLV3704IPW

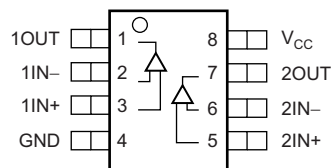
(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV3704CDR).

## 6 Pin Configuration and Functions


**TLV3701 Pin Functions**

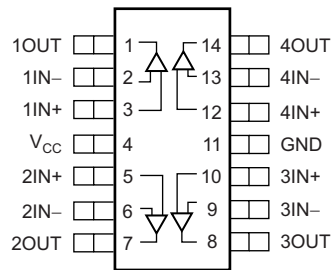
NAME	PIN		I/O	DESCRIPTION
	SOT-23	SOIC, PDIP		
GND	2	4	—	Ground
IN-	4	2	I	Negative (inverting) input
IN+	3	3	I	Positive (noninverting) input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V <sub>CC</sub>	5	7	—	Positive power supply

**TLV3702 D, DGK, or P Package**  
8-Pin SOIC, VSSOP, or PDIP  
Top View


**TLV3702 Pin Functions**

NAME	PIN		I/O	DESCRIPTION
	NO.			
GND	4		—	Ground
1IN-	2		I	Inverting input, channel 1
2IN-	6		I	Inverting input, channel 2
1IN+	3		I	Noninverting input, channel 1
2IN+	5		I	Noninverting input, channel 2
1OUT	1		O	Output, channel 1
2OUT	7		O	Output, channel 2
V <sub>CC</sub>	8		—	Positive power supply

**TLV3704 D, N, or PW Package  
14-Pin SOIC, PDIP, or TSSOP  
Top View**



**TLV3704 Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	11	—	Ground
1IN-	2	I	Inverting input, channel 1
2IN-	6	I	Inverting input, channel 2
3IN-	9	I	Inverting input, channel 3
4IN-	13	I	Inverting input, channel 4
1IN+	3	I	Noninverting input, channel 1
2IN+	5	I	Noninverting input, channel 2
3IN+	10	I	Noninverting input, channel 3
4IN+	12	I	Noninverting input, channel 4
1OUT	1	O	Output, channel 1
2OUT	7	O	Output, channel 2
3OUT	8	O	Output, channel 3
4OUT	14	O	Output, channel 4
V <sub>CC</sub>	4	—	Positive power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{CC}$ <sup>(2)</sup>		17	V
Differential input voltage, $V_{ID}$		±20	V
Input voltage, $V_I$ <sup>(2)(3)</sup>	0	$V_{CC} + 5$	V
Input current, $I_I$		±10	mA
Output current, $I_O$		±10	mA
Continuous total power dissipation	See <a href="#">Dissipation Ratings</a>		
Maximum junction temperature, $T_J$		150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature, $T_{stg}$	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to GND.

(3) Input voltage range is limited to 20 V maximum or  $V_{CC} + 5$  V, whichever is smaller.

### 7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, $V_{CC}$	Single supply	C-suffix	2.5	16	V
		I-suffix	2.7	16	
	Split supply	C-suffix	±1.25	±8	
		I-suffix	±1.35	±8	
Common-mode input voltage, $V_{ICR}$			–0.1	$V_{CC} + 5$	V
Operating free-air temperature, $T_A$	C-suffix		0	70	°C
	I-suffix		–40	125	

### 7.3 Thermal Information – TLV3701

THERMAL METRIC <sup>(1)</sup>		TLV3701			UNIT
		DBV (SOT-23)	D (SOIC)	P (PDIP)	
		5 PINS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.6	124.8	82.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.4	69.1	84.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	67.9	59.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	16.9	22.3	45.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	53.6	67.2	59.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.4 Thermal Information – TLV3702

THERMAL METRIC <sup>(1)</sup>		TLV3702			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	163.9	77.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.4	65.7	79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.2	85.3	54	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	14.6	9	39.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	59.5	83.9	53.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.5 Thermal Information – TLV3704

THERMAL METRIC <sup>(1)</sup>		TLV3704			UNIT
		D (SOIC)	N (PDIP)	PW (TSSOP)	
		14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.4	58.1	105.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.1	50.9	33.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.8	38	49.5	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	7.5	23.6	2.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	37.4	37.7	48.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Electrical Characteristics

 At specified operating free-air temperature range,  $V_{CC} = 2.7\text{ V}, 5\text{ V}, 15\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT
<b>DC PERFORMANCE</b>							
$V_{IO}$	Input offset voltage	$V_{IC} = V_{CC}/2, R_S = 50\ \Omega$	25°C	250	5000		$\mu\text{V}$
			Full range		7000		
$\alpha_{VIO}$	Offset voltage drift	$V_{IC} = V_{CC}/2, R_S = 50\ \Omega$	25°C		3		$\mu\text{V}/^\circ\text{C}$
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}, R_S = 50\ \Omega$	25°C	55	72		dB
			Full range		50		
		$V_{IC} = 0\text{ to }5\text{ V}, R_S = 50\ \Omega$	25°C	60	76		
			Full range		55		
		$V_{IC} = 0\text{ to }15\text{ V}, R_S = 50\ \Omega$	25°C	65	88		
			Full range		60		
$A_{VD}$	Large-signal differential voltage amplification		25°C		1000		V/mV
<b>INPUT/OUTPUT CHARACTERISTICS</b>							
$I_{IO}$	Input offset current	$V_{IC} = V_{CC}/2, R_S = 50\ \Omega$	25°C	20	100		pA
			Full range		1000		
$I_{IB}$	Input bias current	$V_{IC} = V_{CC}/2, R_S = 50\ \Omega$	25°C	80	250		pA
			Full range		1500		
$r_{i(d)}$	Differential input resistance		25°C		300		M $\Omega$
$V_{OH}$	High-level output voltage	$V_{IC} = V_{CC}/2, I_{OH} = 2\ \mu\text{A}, V_{ID} = 1\text{ V}$	25°C	$V_{CC} - 80$			mV
			Full range	$V_{CC} - 320$			
		$V_{IC} = V_{CC}/2, I_{OH} = -50\ \mu\text{A}, V_{ID} = 1\text{ V}$	Full range	$V_{CC} - 450$			
$V_{OL}$	Low-level output voltage	$V_{IC} = V_{CC}/2, I_{OH} = 2\ \mu\text{A}, V_{ID} = -1\text{ V}$	25°C	8			mV
			Full range	80		200	
		$V_{IC} = V_{CC}/2, I_{OH} = 50\ \mu\text{A}, V_{ID} = -1\text{ V}$	Full range	300			
<b>POWER SUPPLY</b>							
$I_{CC}$	Supply current (per channel)	Output state high	25°C	560	800		nA
			Full range		1000		
PSRR	Power supply rejection ratio	$V_{IC} = V_{CC}/2\text{ V}, \text{ No load}$	$V_{CC} = 2.7\text{ V to }5\text{ V}$	25°C	75	100	dB
				Full range		70	
			$V_{CC} = 5\text{ V to }15\text{ V}$	25°C	85	105	
				Full range		80	

(1) Full range is 0°C to 70°C for C suffix and -40°C to 125°C for I suffix. If not specified, full range is -40°C to 125°C.



## 7.7 Switching Characteristics

At specified operating free-air temperature range,  $V_{CC} = 2.7\text{ V}, 5\text{ V}, 15\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(PLH)}$	Propagation response time, low-to-high-level output <sup>(1)</sup>	$f = 10\text{ kHz}, V_{STEP} = 100\text{ mV}, C_L = 10\text{ pF}, V_{CC} = 2.7\text{ V}$	Overdrive = 2 mV	240		$\mu\text{s}$
			Overdrive = 10 mV	64		
			Overdrive = 50 mV	36		
$t_{(PHL)}$	Propagation response time, high-to-low-level output <sup>(1)</sup>	$f = 10\text{ kHz}, V_{STEP} = 100\text{ mV}, C_L = 10\text{ pF}, V_{CC} = 2.7\text{ V}$	Overdrive = 2 mV	167		$\mu\text{s}$
			Overdrive = 10 mV	67		
			Overdrive = 50 mV	37		
$t_r$	Rise time	$C_L = 10\text{ pF}, V_{CC} = 2.7\text{ V}$		7		$\mu\text{s}$
$t_f$	Fall time	$C_L = 10\text{ pF}, V_{CC} = 2.7\text{ V}$		9		$\mu\text{s}$
$t_{su}$	Start-up time (TLV3701 Only)	$V_{CC} = 2.7\text{ to }15\text{V}^{(2)}$	25°C	7	15	ms
			Full range	14	30	

- (1) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V. Propagation responses are longer at higher supply voltages, refer to **Figures 12 – 17** for further details.
- (2) The definition of start-up time is the time period between the supply voltage reaching minimum supply ( $V_{CCmin}$ ) and the device IQ activating ( $I_{CCmin}$ ) with a valid device output voltage. Single device only.

## 7.8 Dissipation Ratings

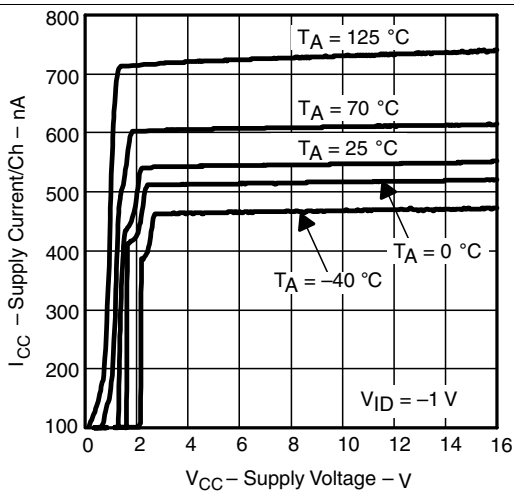
PACKAGE	$\theta_{JC}$ (°C/W)	$\theta_{JA}$ (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	69.1	124.8	1001 mW	200 mW
D (14)	38.1	81.4	1536 mW	307 mW
DBV (5)	102.4	193.6	646 mW	129 mW
DGK (8)	65.7	163.9	763 mW	153 mW
N (14)	50.9	58.1	2151 mW	430 mW
P (8)	84.8	82.8	1510 mW	302 mW
PW (14)	33.9	105.7	1183 mW	237 mW

### 7.9 Typical Characteristics

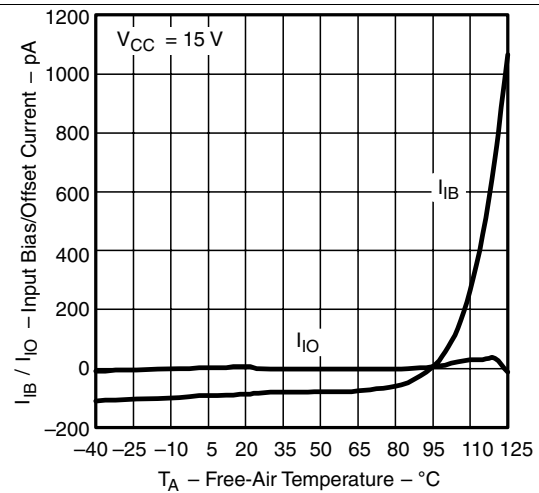
At specified operating conditions (unless otherwise noted).

**Table 5. Table of Graphs**

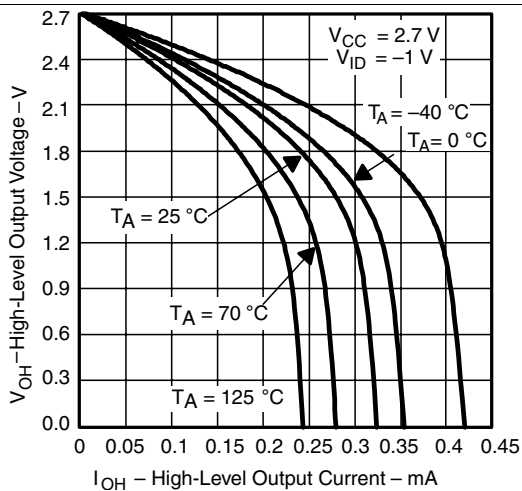
		FIGURE
	Input bias/offset current	vs Free-air temperature
$V_{OL}$	Low-level output voltage	vs Low-level output current
$V_{OH}$	High-level output voltage	vs High-level output current
$I_{CC}$	Supply current	vs Supply voltage
		Free-air temperature
	Output fall time/rise time	vs Supply voltage
	Low-to-high level output response for various input overdrives	Figure 11, Figure 13, Figure 15
	High-to-low level output response for various input overdrives	Figure 12, Figure 14, Figure 16



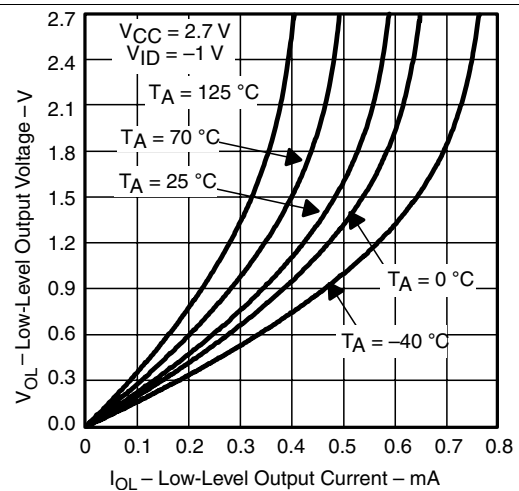
**Figure 1. Supply Current vs Supply Voltage**



**Figure 2. Input Bias/Offset Current vs Free-Air Temperature**



**Figure 3. High-Level Output Voltage vs High-Level Output Current**



**Figure 4. Low-Level Output Voltage vs Low-Level Output Current**

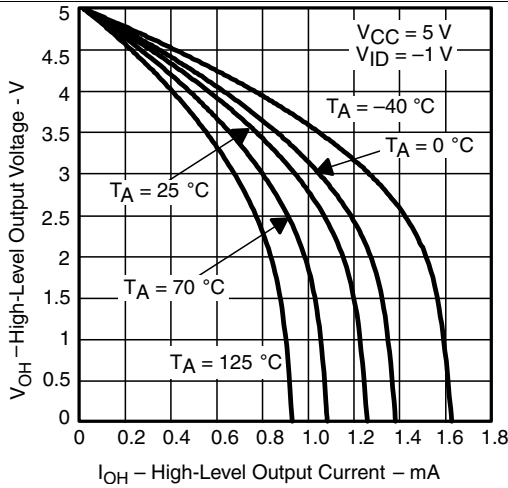


Figure 5. High-Level Output Voltage vs High-Level Output Current

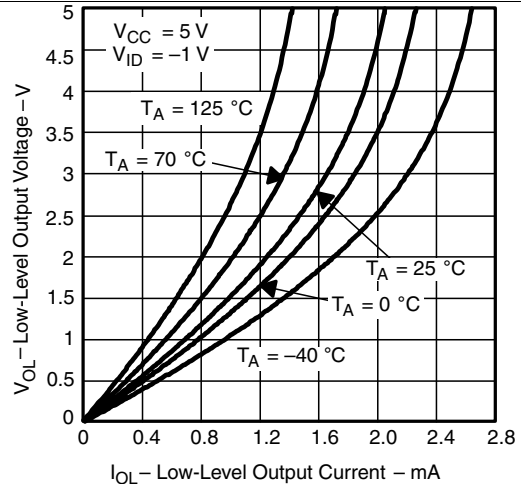


Figure 6. Low-Level Output Voltage vs Low-Level Output Current



Figure 7. High-Level Output Voltage vs High-Level Output Current



Figure 8. Low-Level Output Voltage vs Low-Level Output Current

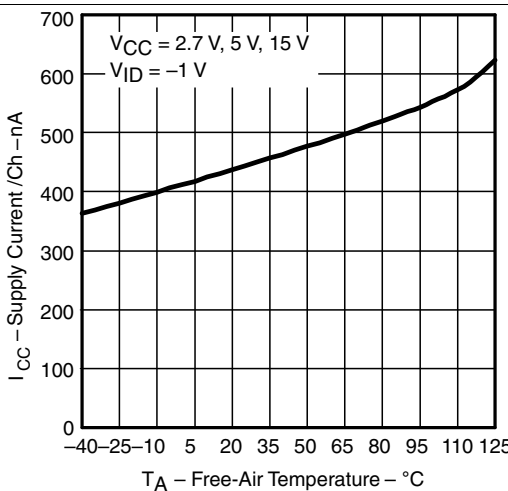


Figure 9. Supply Current vs Free-Air Temperature

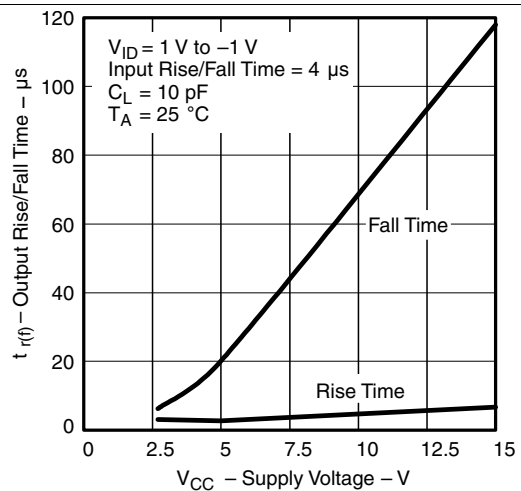
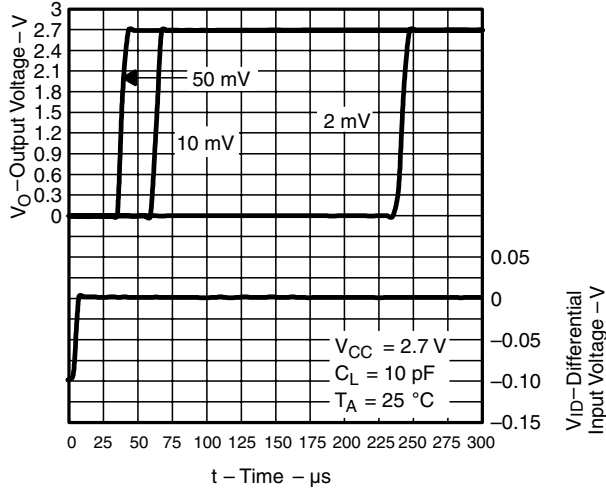
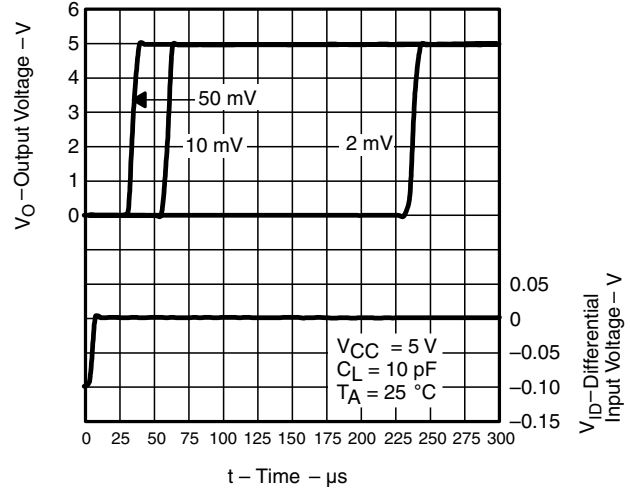
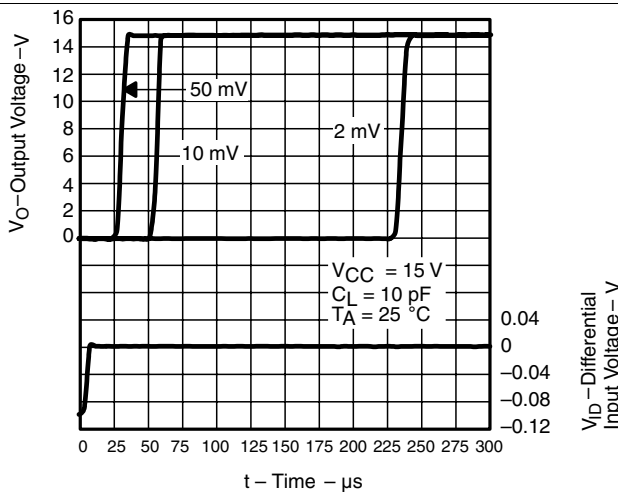
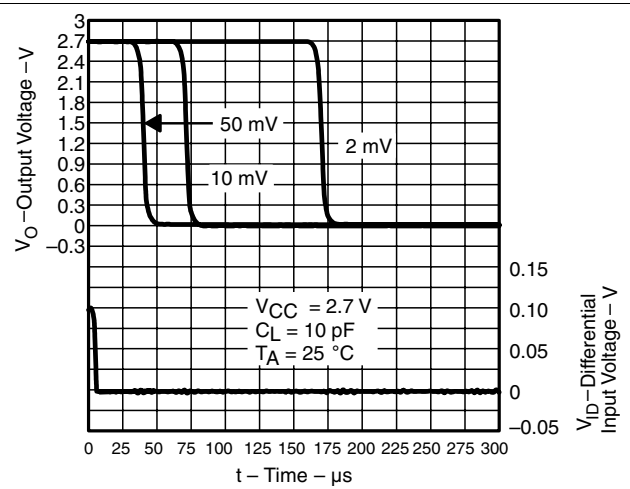
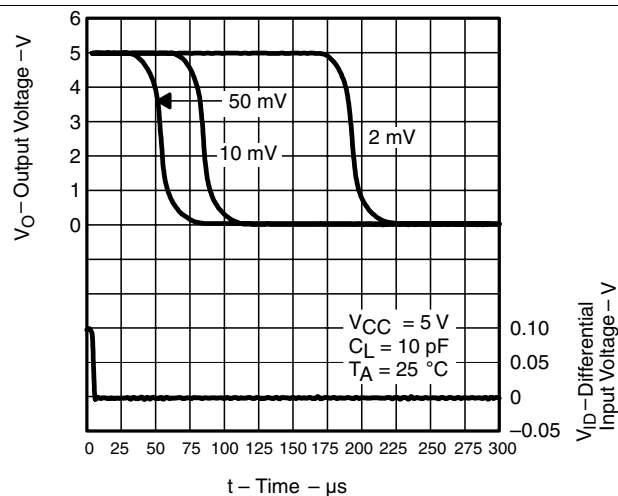
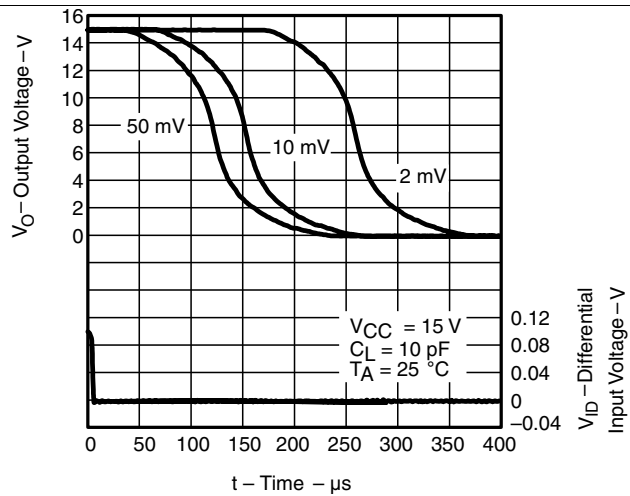


Figure 10. Output Rise/Fall Time vs Supply Voltage

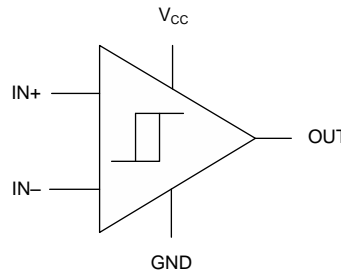

**Figure 11. Low-to-High Output Response for Various Input Overdrives**

**Figure 12. High-to-Low Level Output Response for Various Input Overdrives**

**Figure 13. Low-to-High Level Output Response for Various Input Overdrives**

**Figure 14. High-to-Low Level Output Response for Various Input Overdrives**

**Figure 15. Low-to-High Level Output Response for Various Input Overdrives**

**Figure 16. High-to-Low Level Output Response for Various Input Overdrives**

## 8 Detailed Description

### 8.1 Overview

The TLV370x is a family of nanopower comparators drawing only 560 nA per channel supply current. Having a minimum operating supply voltage of 2.7 V over the extended industrial temperature range ( $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ), while having an input common-mode range of  $-0.1$  to  $V_{CC} + 5$  V makes this device ideal for battery-powered and wireless handset applications.

### 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

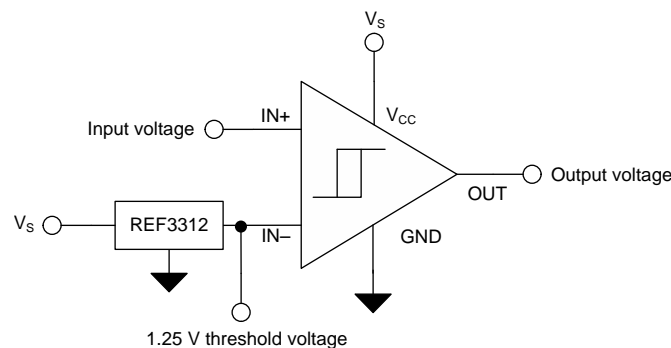
### 8.3 Feature Description

#### 8.3.1 Operating Voltage

The TLV340x comparators are specified for use on a single supply from 2.5 V to 16 V (or a dual supply from  $\pm 1.25$  V to  $\pm 16$  V) over a temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

#### 8.3.2 Setting the Threshold

Using a low-power, stable reference is important when setting the transition point for the TLV340x devices. The REF3312, as shown in Figure 17, provides a 1.25-V reference voltage with low drift and only 3.9  $\mu\text{A}$  of quiescent current.



Copyright © 2016, Texas Instruments Incorporated

Figure 17. Setting the Threshold

### 8.4 Device Functional Modes

The TLV370x has a single functional mode and is operational when the power supply voltage applied ranges from 2.5 V ( $\pm 1.25$  V) to 16 V ( $\pm 8$  V).

## 9 Application and Implementation

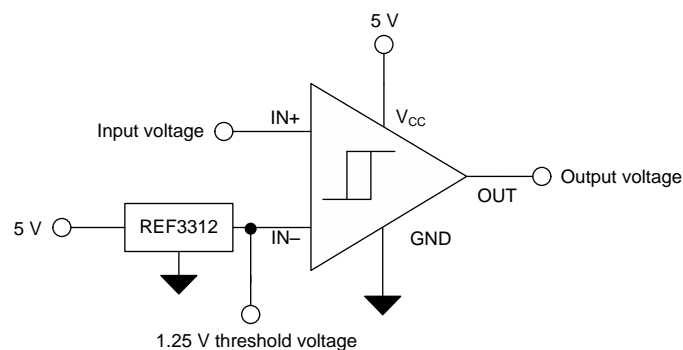
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Many applications require the detection of a signal (voltage or current) that exceeds a particular threshold voltage or current. Using a comparator to make that threshold detection is the easiest, lowest power and highest speed way to make a threshold detection.

### 9.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

**Figure 18. 1.25-V Threshold Detector**

#### 9.2.1 Design Requirements

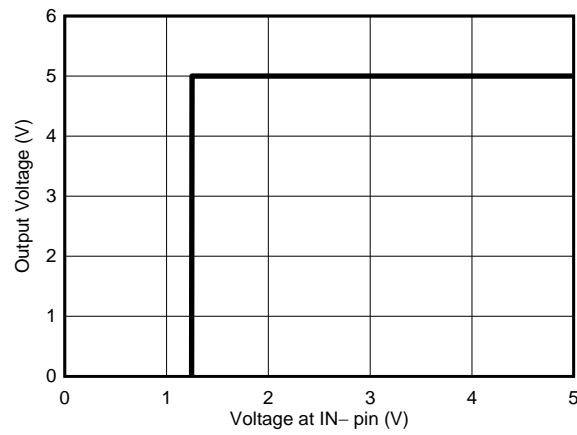
- Detect when a signal is above or below 1.25 V
- Operate from a single 5-V power supply
- Rail-to-rail input voltage range from 0 to 5 V
- Rail-to-rail output voltage range from 0 to 5 V

#### 9.2.2 Detailed Design Procedure

The input voltage range in the circuit illustrated in [Figure 18](#) is limited only by the power supply applied to the TV3701. In this example with the selection of a 5-V, single-supply power supply, the input voltage range is limited to 0 to  $V_S + 5$  V, or 0 to 10 V. The threshold voltage of 1.25 V can be derived in a variety of ways. As the TLV3701 is a very low-power device, it is desirable to also use very low power to create the threshold voltage. The REF3312 series voltage reference is selected for its stable output voltage of 1.25 V and its low power consumption of only 3.9  $\mu$ A. The TLV3701 is a push-pull output comparator, and does not require a pullup resistor to save power.

## Typical Application (continued)

### 9.2.3 Application Curve



**Figure 19. Transfer Function for the Threshold Detector**

## 10 Power Supply Recommendations

The TLV340x device is specified for operation from 2.5 V to 16 V ( $\pm 1.25$  to  $\pm 8$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Typical Characteristics](#).

## 11 Layout

### 11.1 Layout Guidelines

**Figure 20** shows the typical connections for the TLV340x. To minimize supply noise, power supplies must be capacitively decoupled by a 0.01- $\mu\text{F}$  ceramic capacitor in parallel with a 10- $\mu\text{F}$  electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (the use of a ground plane) helps to maintain the specified performance of the TLV340x family.

For best results, maintain the following layout guidelines:

1. Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1- $\mu\text{F}$  ceramic, surface-mount capacitor) as close as possible to  $V_{\text{CC}}$ .
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The top-side ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

### 11.2 Layout Example



Copyright © 2016, Texas Instruments Incorporated

**Figure 20. TLV3701 SOT-23 Layout Example**



## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

##### 12.1.1.1 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (8-pin SOIC), PW (8-pin TSSOP), DGK (8-pin MSOP), DBV (6-pin SOT-23, 5-pin SOT23, and 3-pin SOT-23), DCK (6-pin SC-70 and 5-pin SC-70), and DRL (6-pin SOT-563). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

##### 12.1.1.2 Universal Op Amp EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP, and SOT-23 packages are all supported.

---

#### NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

---

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

The following documents are relevant for using the TLV340x devices and are recommended for reference. All are available for download at [www.ti.com](http://www.ti.com) (unless otherwise noted):

- [Universal Op Amp EVM User Guide](#) (SLOU060)
- [Hardware Pace Using Slope Detection](#) (SLAU511)
- [Bipolar High-voltage Differential Interface for Low-Voltage Comparators](#) (TIDU039)
- [AC-Coupled Single Supply Comparator](#) (SLAU505)
- [ECG Implementation on the TMS320VC5505 DSP Medical Development Kit](#) (SPRAB36)
- [REF33xx 3.9- \$\mu\$ A, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/ \$^{\circ}\$ C Drift Voltage Reference](#) (SBOS392)

#### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 6. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV3701	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV3702	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV3704	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.6 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 12.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3701CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3701C	<a href="#">Samples</a>
TLV3701CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VBCC	<a href="#">Samples</a>
TLV3701CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VBCC	<a href="#">Samples</a>
TLV3701CDBVBT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VBCC	<a href="#">Samples</a>
TLV3701CDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	VBCC	<a href="#">Samples</a>
TLV3701ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3701I	<a href="#">Samples</a>
TLV3701IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBCI	<a href="#">Samples</a>
TLV3701IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBCI	<a href="#">Samples</a>
TLV3701IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBCI	<a href="#">Samples</a>
TLV3701IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBCI	<a href="#">Samples</a>
TLV3701IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3701I	<a href="#">Samples</a>
TLV3701IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3701I	<a href="#">Samples</a>
TLV3701IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV3701I	<a href="#">Samples</a>
TLV3701IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV3701I	<a href="#">Samples</a>
TLV3702CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3702C	<a href="#">Samples</a>
TLV3702CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3702C	<a href="#">Samples</a>
TLV3702CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AKC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3702CDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AKC	<a href="#">Samples</a>
TLV3702CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AKC	<a href="#">Samples</a>
TLV3702CDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AKC	<a href="#">Samples</a>
TLV3702ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702I	<a href="#">Samples</a>
TLV3702IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702I	<a href="#">Samples</a>
TLV3702IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKD	<a href="#">Samples</a>
TLV3702IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKD	<a href="#">Samples</a>
TLV3702IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKD	<a href="#">Samples</a>
TLV3702IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKD	<a href="#">Samples</a>
TLV3702IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702I	<a href="#">Samples</a>
TLV3702IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702I	<a href="#">Samples</a>
TLV3702IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV3702I	<a href="#">Samples</a>
TLV3702IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV3702I	<a href="#">Samples</a>
TLV3704CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3704C	<a href="#">Samples</a>
TLV3704CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3704C	<a href="#">Samples</a>
TLV3704CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3704C	<a href="#">Samples</a>
TLV3704ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>
TLV3704IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3704IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>
TLV3704IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>
TLV3704IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLV3704I	<a href="#">Samples</a>
TLV3704IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>
TLV3704IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>
TLV3704IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>
TLV3704IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3704I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV3701, TLV3702 :**

- Automotive: [TLV3701-Q1](#), [TLV3702-Q1](#)
- Enhanced Product: [TLV3701-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3701CDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV3701CDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV3701IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV3701IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV3701IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3702CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3702IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3702IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3704IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV3704IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3701CDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV3701CDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV3701IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV3701IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV3701IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV3702CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV3702IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV3702IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV3704IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV3704IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0



## GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073253/P

DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

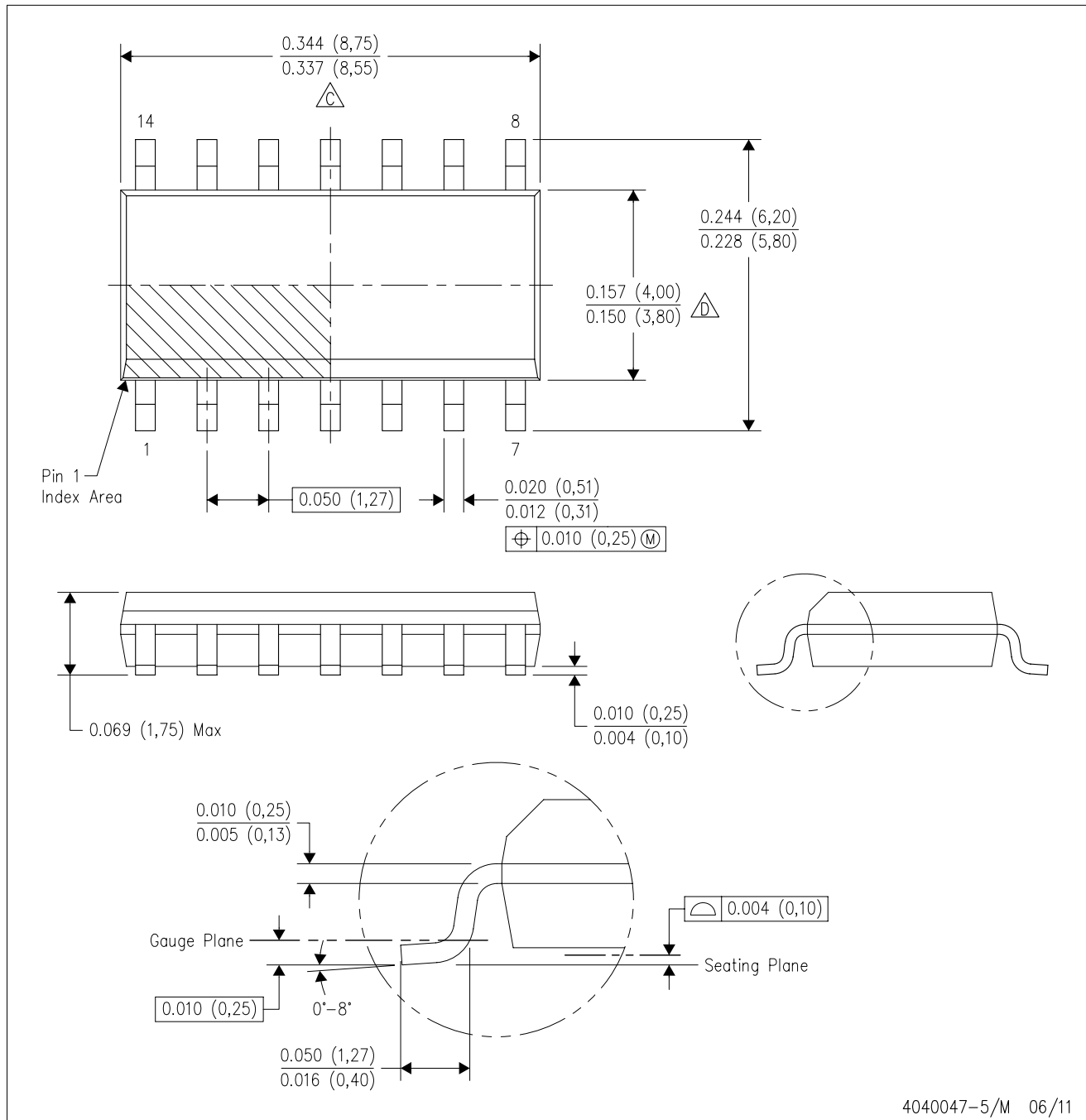
4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.