LM7301 Low Power, 4-MHz GBW, Rail-to-Rail Input-Output Operational Amplifier in SOT-23 Package

1 Features

- At V_S = 5 V (Typical Unless Otherwise Noted)
- Tiny, Space-Saving, 5-Pin SOT-23 Package
- Greater than Rail-to-Rail Input CMVR: −0.25 V to 5.2 V
- Rail-to-Rail Output Swing: 007 V to 4.93 V
- Wide Gain-Bandwidth: 4 MHz
- Low Supply Current: 0.6 mA
- Wide Supply Range: 1.8 V to 32 V
- High PSRR: 104 dB
- High CMRR: 93 dB
- Excellent Gain: 97 dB

2 Applications

- Portable Instrumentation
- Signal Conditioning Amplifiers/ADC Buffers
- Active Filters
- Modems
- PCMCIA Cards

3 Description

The LM7301 provides high performance in a wide range of applications. The LM7301 offers greater than rail-to-rail input range, full rail-to-rail output swing, large capacitive load driving ability, and low distortion.

With only 0.6-mA supply current, the 4-MHz gain-bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

The LM7301 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Operating on supplies of 1.8 V to 32 V, the LM7301 is excellent for a very wide range of applications in low power systems.

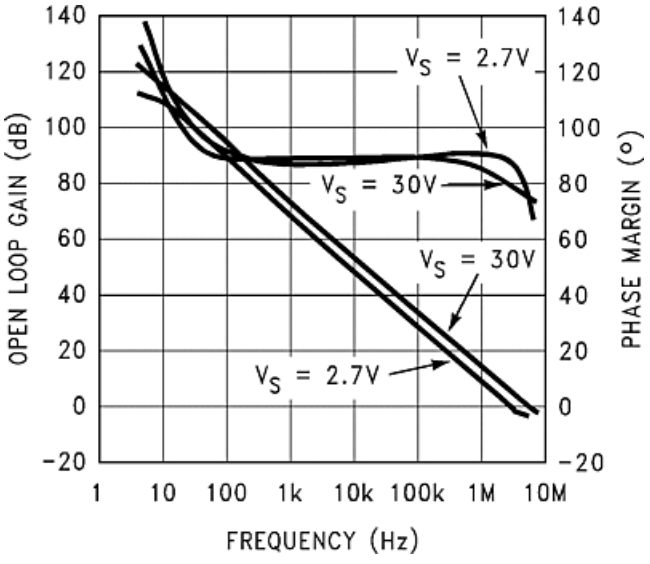
Placing the amplifier right at the signal source reduces board size and simplifies signal routing. The LM7301 fits easily on low profile PCMCIA cards.

Device Information(1)

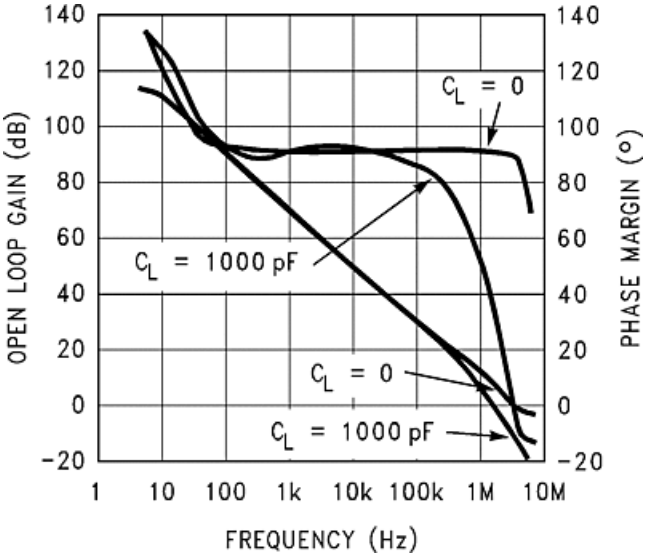
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM7301	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Gain and Phase



Gain and Phase, 2.7-V Supply



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2013) to Revision I **Page**

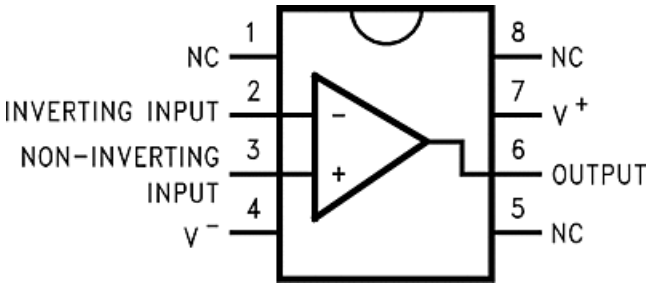
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed 58°C to 42°C in *Power Dissipation* ... 15
- Changed 113°C to 59°C in *Power Dissipation* ... 15
- Changed 29°C to 21°C in *Power Dissipation* ... 15
- Changed 57°C to 30°C in *Power Dissipation* ... 15

Changes from Revision G (March 2013) to Revision H **Page**

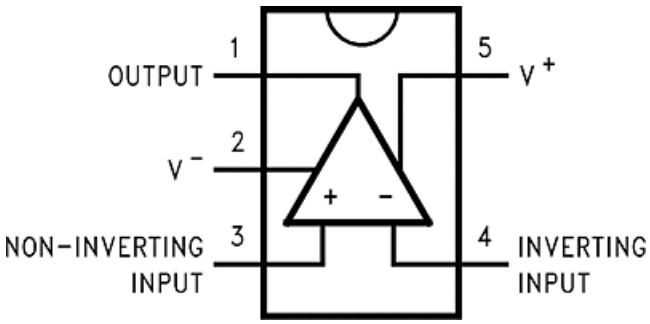
- Changed layout of National Semiconductor Data Sheet to TI format ... 16

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
–IN	2	4	I	Inverting input voltage
+IN	3	3	I	Noninverting input voltage
N/C	1, 5, 8	—	—	No connection
OUT	6	1	O	Output
V–	4	2	I	Negative supply
V+	7	5	I	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Differential input voltage		15	V
Voltage at input and output pin	(V^+) + 0.3	(V^-) – 0.3	V
Supply voltage $(V^+ - V^-)$		35	V
Current at input pin		±10	mA
Current at output pin(3)		±20	mA
Current at power supply pin		25	mA
Junction temperature, T_J(4)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V

(1) JEDEC document JEP155 states that 2500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Supply voltage		1.8		32	V
Operating temperature (2)		–40		85	°C
Package thermal resistance ($R_{\theta JA}$)(2)	5-pin SOT-23	325		325	°C/W
	8-pin SOIC	165		165	°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.4 Thermal Information

THERMAL METRIC(1)		LM7301		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169	120	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122	65	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17	16	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: 5-V DC

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1MΩ to $V^+/2$ unless noted that limits apply at the temperature extremes.(1) (2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A = 25°C			0.03	6	mV
		$T_A = T_J$				8	
TCV_{OS}	Input offset voltage average drift	$T_A = T_J$			2		µV/°C
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		90	200	nA
			$T_A = T_J$			250	
		V_{CM} = 5 V	T_A = 25°C		−40	−75	
			$T_A = T_J$			−85	
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		0.7	70	nA
			$T_A = T_J$			80	
		V_{CM} = 5 V	T_A = 25°C		0.7	55	
			$T_A = T_J$			65	
R_{IN}	Input resistance, CM	0 V ≤ V_{CM} ≤ 5 V			39		MΩ
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 5 V	T_A = 25°C	70	88		dB
			$T_A = T_J$	67			
		0 V ≤ V_{CM} ≤ 3.5 V			93		
PSRR	Power supply rejection ratio	2.2 V ≤ V^+ ≤ 30 V	T_A = 25°C	87	104		dB
			$T_A = T_J$	84			
V_{CM}	Input common-mode voltage range	CMRR ≥ 65 dB			5.1		V
					−0.1		
A_V	Large signal voltage gain	R_L = 10 kΩ V_O = 4 V_{PP}	T_A = 25°C	14	71		V/mV
			$T_A = T_J$	10			
V_O	Output swing	R_L = 10 kΩ	T_A = 25°C		0.07	0.12	V
					4.93		
			$T_A = T_J$	4.88		0.15	
				4.85			
		R_L = 2 kΩ	T_A = 25°C		0.14	0.2	
						0.22	
			$T_A = T_J$	4.80	4.87		
				4.78			
I_{SC}	Output short-circuit current	Sourcing	T_A = 25°C	8	11		mA
			$T_A = T_J$	5.5			
		Sinking	T_A = 25°C	6	9.5		
			$T_A = T_J$	5			
I_S	Supply current	T_A = 25°C			0.6	1.1	mA
		$T_A = T_J$				1.24	

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that $T_J = T_A$. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

6.6 Electrical Characteristics: AC

T_A = 25°C, V^+ = 2.2 V to 30 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$ (1)

PARAMETER		TEST CONDITIONS	TYP (2)	UNIT
SR	Slew rate	±4-V Step at V_S ±6 V	1.25	V/µs
GBW	Gain-bandwidth product	f = 100 kHz, R_L = 10 kΩ	4	MHz
e_n	Input-referred voltage noise	f = 1 kHz	36	nV/√Hz
i_n	Input-referred current noise	f = 1 kHz	0.24	pA/√Hz
T.H.D.	Total harmonic distortion	f = 10 kHz	0.006%	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that T_J = T_A. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.7 Electrical Characteristics: 2.2-V DC

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 2.2 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$ unless noted that limits apply at the temperature. (1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A = 25°C			0.04	6	mV
		T_A = T_J				8	
TCV_{OS}	Input offset voltage average drift	T_A = T_J			2		µV/°C
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		89	200	nA
			T_A = T_J			250	
		V_{CM} = 2.2 V	T_A = 25°C	−75	−35		
			T_A = T_J	−85			
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		0.8	70	nA
			T_A = T_J			80	
		V_{CM} = 2.2 V	T_A = 25°C		0.4	55	
			T_A = T_J			65	
R_{IN}	Input resistance	0 V ≤ V_{CM} ≤ 2.2 V			18		MΩ
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 2.2 V	T_A = 25°C	60	82		dB
			T_A = T_J	56			
PSRR	Power supply rejection ratio	2.2 V ≤ V^+ ≤ 30 V	T_A = 25°C	87	104		dB
			T_A = T_J	84			
V_{CM}	Input common-mode voltage range	CMRR > 60 dB			2.3		V
					–0.1		
A_V	Large signal voltage gain	R_L = 10 kΩ V_O = 1.6 V_{PP}	T_A = 25°C	6.5	46		V/mV
			T_A = T_J	5.4			
V_O	Output swing	R_L = 10 kΩ	T_A = 25°C		0.05	0.08	V
					2.15		
			T_A = T_J			0.1	
		R_L = 2 kΩ	T_A = 25°C		0.09	0.13	
			T_A = T_J			0.14	

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(2) All limits are ensured by testing or statistical analysis.

Electrical Characteristics: 2.2-V DC (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 2.2 V, V^- = 0 V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2 unless noted that limits apply at the temperature. (1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SC}	Output short-circuit current	Sourcing	T_A = 25°C	8	10.9		mA
			T_A = T_J	5.5			
		Sinking	T_A = 25°C	6	7.7		
			T_A = T_J	5			
I_S	Supply current	T_A = 25°C			0.57	0.97	mA
		T_A = T_J				1.24	

6.8 Electrical Characteristics: 30-V DC

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 30 V, V^- = 0 V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ to V^+/2 unless noted that limits apply at the temperature(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage				0.04	6	mV
						8	
TCV_{OS}	Input offset voltage average drift	T_A = T_J			2		µV/°C
I_B	Input bias current	V_{CM} = 0 V	T_A = 25°C		103	300	nA
			T_A = T_J			500	
		V_{CM} = 30 V	T_A = 25°C	−100	−50		
			T_A = T_J	−200			
I_{OS}	Input offset current	V_{CM} = 0 V	T_A = 25°C		1.2	90	nA
			T_A = T_J			190	
		V_{CM} = 30 V	T_A = 25°C		0.5	65	
			T_A = T_J			135	
R_{IN}	Input resistance	0 V ≤ V_{CM} ≤ 30 V			200		MΩ
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 30 V	T_A = 25°C	80	104		dB
			T_A = T_J	78			
		0 V ≤ V_{CM} ≤ 27 V	T_A = 25°C	90	115		
			T_A = T_J	88			
PSRR	Power supply rejection ratio	2.2 V ≤ V^+ ≤ 30 V	T_A = 25°C	87	104		dB
			T_A = T_J	84			
V_{CM}	Input common-mode voltage range	CMRR > 80 dB			30.1		V
					−0.1		
A_V	Large signal voltage gain	R_L = 10 kΩ V_O = 28 V_{PP}	T_A = 25°C	30	105		V/mV
			T_A = T_J	20			
V_O	Output swing	R_L = 10 kΩ	T_A = 25°C		0.16	0.275	V
			T_A = T_J			0.375	
			T_A = 25°C	29.75	29.8		
			T_A = T_J	28.65			
I_{SC}	Output short-circuit current	Sourcing(2)	T_A = 25°C	8.8	11.7		mA
			T_A = T_J	6.5			
		Sinking(2)	T_A = 25°C	8.2	11.5		
			T_A = T_J	6			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the devices such that T_J = T_A. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = ($T_{J(MAX)}$ − T_A)/$R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

Electrical Characteristics: 30-V DC (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 30 V, V^- = 0 V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$ unless noted that limits apply at the temperature[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Supply current	T_A = 25°C		0.72	1.3	mA
		$T_A = T_J$			1.35	

6.9 Typical Characteristics

T_A = 25°C, R_L = 1 MΩ unless otherwise specified

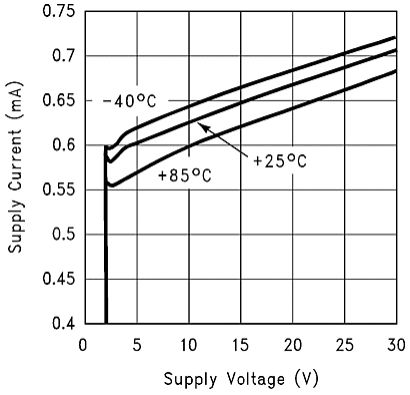


Figure 1. Supply Current vs Supply Voltage

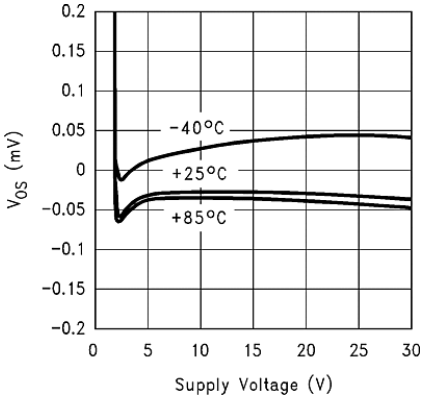


Figure 2. V_{OS} vs Supply Voltage

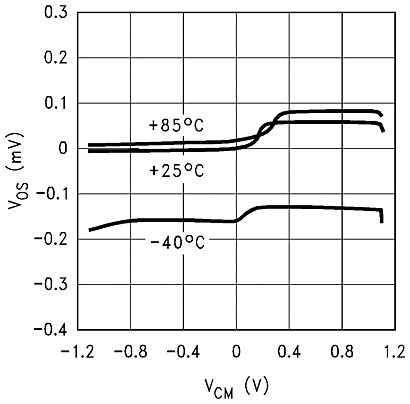


Figure 3. V_{OS} vs V_{CM} V_S = ±1.1 V

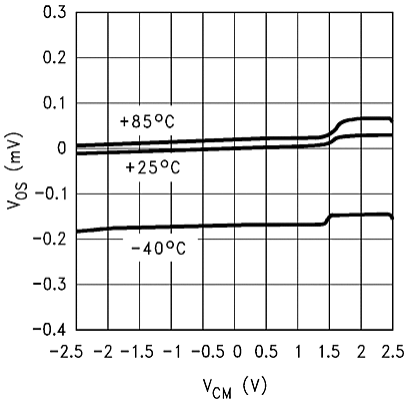


Figure 4. V_{OS} vs V_{CM} V_S = ±2.5 V

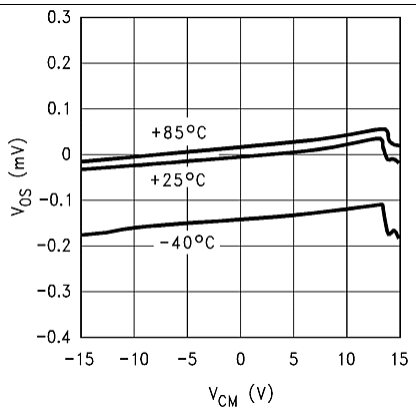


Figure 5. V_{OS} vs V_{CM} V_S = ±15 V

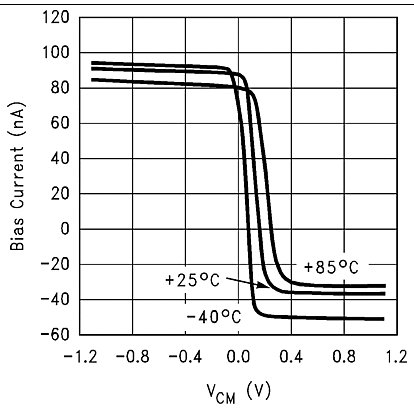


Figure 6. Inverting Input Bias Current vs Common Mode Voltage V_S = ±1.1 V

Typical Characteristics (continued)

T_A = 25°C, R_L = 1 MΩ unless otherwise specified

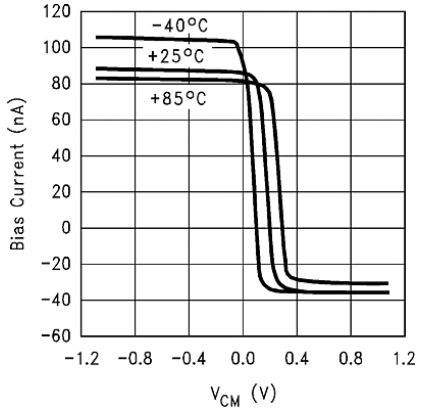


Figure 7. Noninverting Input Bias Current vs Common Mode Voltage V_S = ±1.1 V

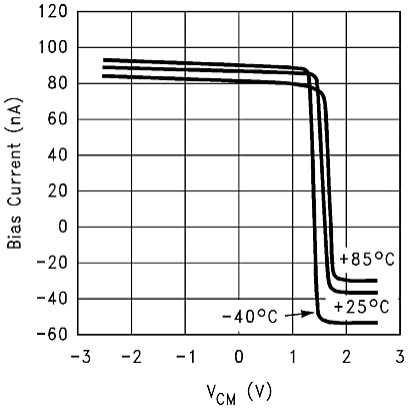


Figure 8. Inverting Input Bias Current vs Common Mode Voltage V_S = ±2.5 V

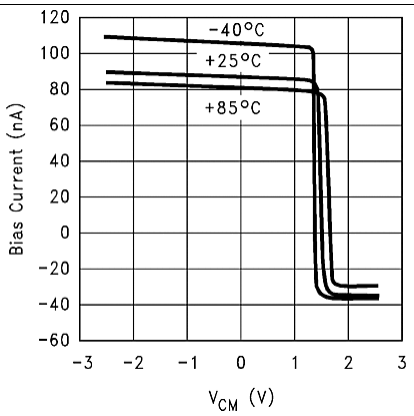


Figure 9. Noninverting Input Bias Current vs Common Mode Voltage V_S = ±2.5 V

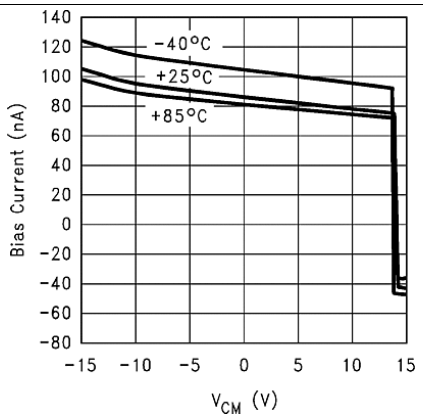


Figure 10. Noninverting Input Bias Current vs Common Mode Voltage V_S = ±15 V

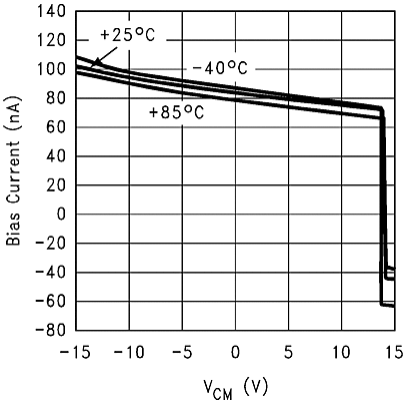


Figure 11. Inverting Input Bias Current vs Common Mode Voltage V_S = ±15 V

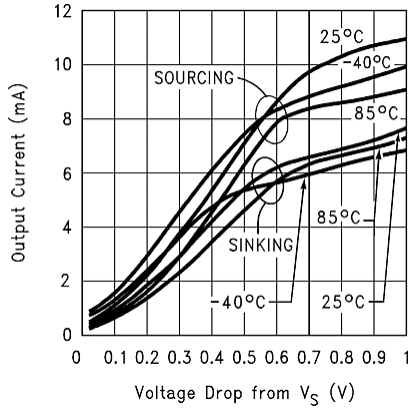


Figure 12. V_O vs I_O V_S = ±1.1 V

Typical Characteristics (continued)

T_A = 25°C, R_L = 1 MΩ unless otherwise specified

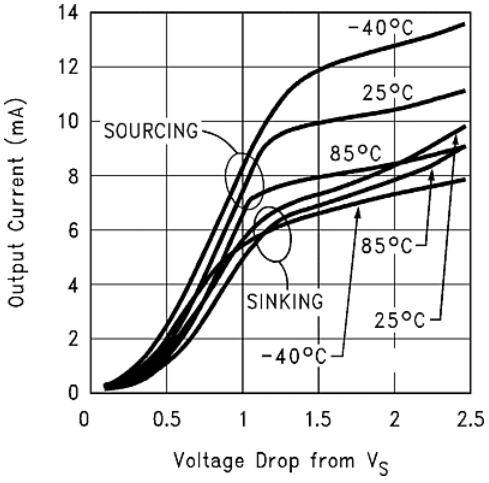


Figure 13. V_O vs I_O V_S = ±2.5 V

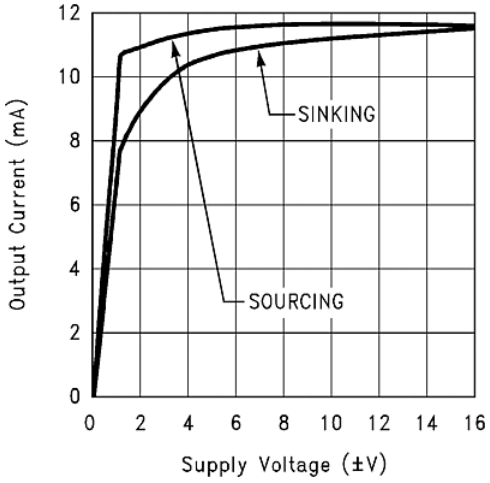


Figure 14. Short-Circuit Current vs Supply Voltage

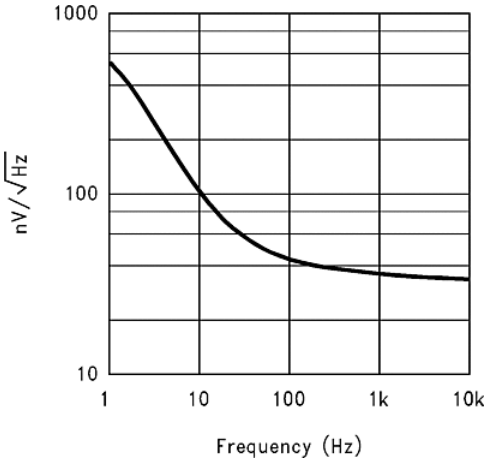


Figure 15. Voltage Noise vs Frequency

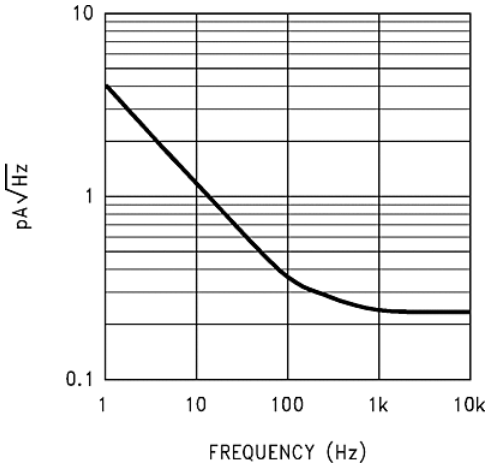


Figure 16. Current Noise vs Frequency

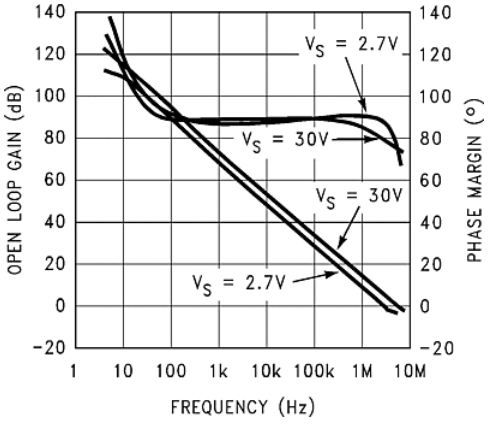


Figure 17. Gain and Phase

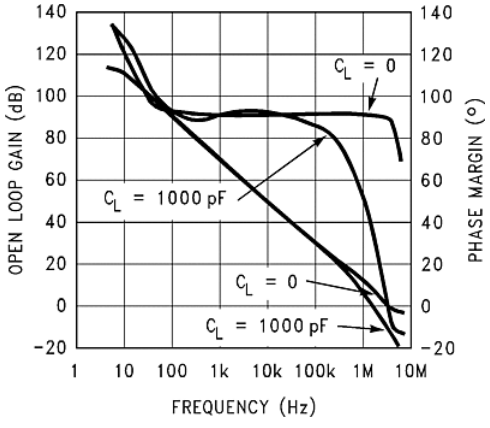


Figure 18. Gain and Phase, 2.7-V Supply

7 Detailed Description

7.1 Overview

Low supply current, wide bandwidth, input common mode voltage range that includes both rails, rail-to-rail output, good capacitive load driving ability, wide supply voltage (1.8 V to 32 V), and low distortion all make the LM7301 ideal for many diverse applications.

The high common-mode rejection ratio and full rail-to-rail input range provides precision performance when operated in noninverting applications where the common-mode error is added directly to the other system errors.

7.2 Feature Description

7.2.1 Capacitive Load Driving

The LM7301 has the ability to drive large capacitive loads. For example, 1000 pF only reduces the phase margin to about 25°.

7.2.2 Transient Response

The LM7301 offers a very clean, well-behaved transient response. Figure 19, Figure 20, Figure 22, and Figure 23 show the response when operated at gains of +1 and −1 when handling both small and large signals. The large phase margin, typically 70° to 80°, assures clean and symmetrical response. In the large signal scope photos, Figure 19 and Figure 22, the input signal is set to 4.8 V. The output goes to within 100 mV of the supplies cleanly and without overshoot. In the small signal samples, the response is clean, with only slight overshoot when used as a follower. Figure 21 and Figure 24 are the circuits used to make these photos.

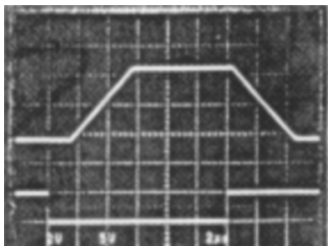


Figure 19. A_V = –1 V/V, Large Signal Behavior (1 V/div, 2 µs/div)

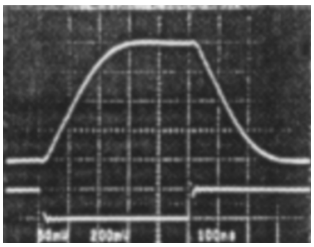


Figure 20. A_V = –1 V/V, Small Signal Behavior (0.2 V/div, 100 µs/div)

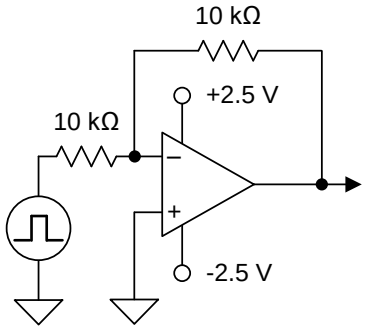


Figure 21. A_V = –1 V/V Schematic

Feature Description (continued)

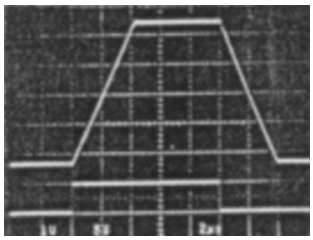


Figure 22. A_V = 1 V/V, Large Signal Behavior (1 V/div, 2 us/div)

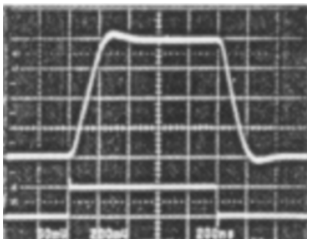


Figure 23. A_V = 1 V/V, Small Signal Behavior (0.2 V/div, 200 µs/div)

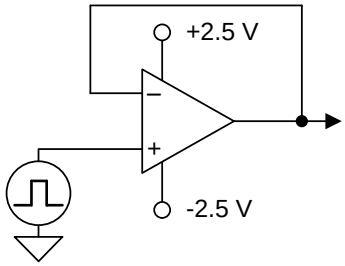


Figure 24. A_V = 1-V/V Schematic

7.2.3 Wide Supply Range

The high power-supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) provide precision performance when operated on battery or other unregulated supplies. This advantage is further enhanced by the very wide supply range (2.2 V to 30 V, ensured) offered by the LM7301. In situations where highly variable or unregulated supplies are present, the excellent PSRR and wide supply range of the LM7301 benefit the system designer with continued precision performance, even in such adverse supply conditions.

7.2.4 Specific Advantages of 5-Pin SOT-23 (TinyPak)

The obvious advantage of the 5-pin SOT-23, TinyPak, is that it can save board space, a critical aspect of any portable or miniaturized system design. The need to decrease overall system size is inherent in any handheld, portable, or lightweight system application.

Furthermore, the low profile can help in height limited designs, such as consumer hand-held remote controls, sub-notebook computers, and PCMCIA cards.

An additional advantage of the tiny package is that it allows better system performance due to ease of package placement. Because the tiny package is so small, it can fit on the board right where the operational amplifier must be placed for optimal performance, unconstrained by the usual space limitations. This optimal placement of the tiny package allows for many system enhancements that are not easily achieved with the constraints of a larger package. For example, problems such as system noise due to undesired pickup of digital signals can be easily reduced or mitigated. This pickup problem is often caused by long wires in the board layout going to or from an operational amplifier. By placing the tiny package closer to the signal source and allowing the LM7301 output to drive the long wire, the signal becomes less sensitive to such pickup. An overall reduction of system noise results.

Often times system designers try to save space by using dual or quad op amps in their board layouts. This causes a complicated board layout due to the requirement of routing several signals to and from the same place on the board. Using the tiny operational amplifier eliminates this problem.

Additional space savings parts are available in tiny packages from Texas Instruments, including low-power amplifiers, precision-voltage references, and voltage regulators.

Feature Description (continued)

7.2.5 Low-Distortion, High-Output Drive Capability

The LM7301 offers superior low-distortion performance, with a total-harmonic-distortion-plus-noise of 0.06% at f = 10 kHz. The advantage offered by the LM7301 is its low distortion levels, even at high output current and low load resistance. See *Stability Considerations* for methods used to ensure stability under all load conditions.

7.3 Device Functional Modes

7.3.1 Stability Considerations

Rail-to-rail output amplifiers like the LM7301 use the collector of the drive transistor(s) at the output pin, as shown in Figure 25. This allows the load to be driven as close as possible towards either supply rail.

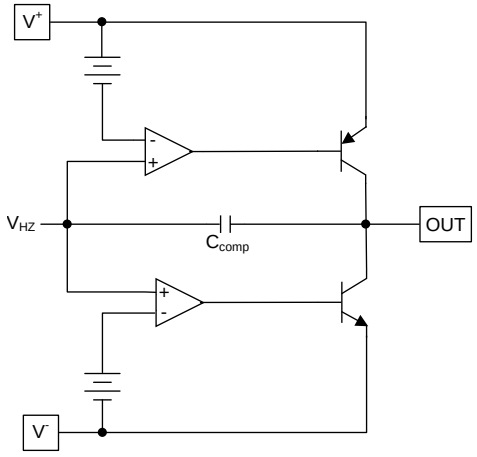


Figure 25. Simplified Output Stage Block Diagram

While this architecture maximizes the load voltage swing range, it increases the dependence of loop gain and subsequently stability, on load impedance and DC load current, compared to a non-rail-to-rail architecture. Thus, with this type of output stage, it is even more crucial to ensure stability by meticulous bench verification under all load conditions, and to apply the necessary compensation or circuit modifications to overcome any instability, if necessary. Any such bench verification should also include temperature, supply voltage, input common mode and output bias point variations as well as capacitive loading.

For example, one set of conditions for which stability of the LM7301 amplifier may be compromised is when the DC output load is larger than ±0.5 mA, with input and output biased to mid-rail. Under such conditions, it may be possible to observe open-loop gain response peaking at a high frequency (for example, 200 MHz), which is beyond the expected frequency range of the LM7301 (4 MHz GBW). Without taking any precautions against gain peaking, it is possible to see increased settling time or even oscillations, especially with low closed loop gain and / or light AC loading. It is possible to reduce or eliminate this gain peaking by using external compensation components. One possible scheme that can be applied to reduce or eliminate this gain peaking is shown in Figure 26.

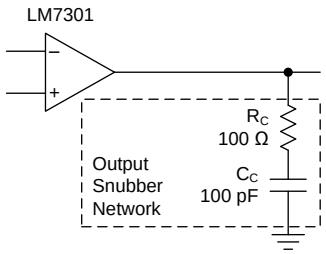


Figure 26. Non-Dissipating Snubber Network to Reduce Gain Peaking

Device Functional Modes (continued)

The non-dissipating snubber, consisting of R_c and C_c, acts as AC load to reduce high-frequency gain peaking with no DC loading so that total power dissipation is not increased. The increased AC load effectively reduces loop gain at higher frequencies thereby reducing gain peaking due to the possible causes stated in the previous sentence. For the particular set of R_c and C_c values shown in Figure 26, loop gain peaking is reduced by about 25 dB under worst case peaking conditions (I_source= 2mA DC at around 180 MHz) thus confining loop gain to less than 0 dB and eliminating any possible instability. For best results, it may be necessary to *tune* the values of R_c and C_c in a particular application to consider other subtleties and tolerances.

7.3.2 Power Dissipation

Although the LM7301 has internal output current limiting, shorting the output to ground when operating on a 30-V power supply will cause the operational amplifier to dissipate about 350 mW. This is a worst-case example. In the 8-pin SOIC package, this will cause a temperature rise of 42°C. In the 5-pin SOT-23 package, the higher thermal resistance will cause a calculated rise of 59°C. This can raise the junction temperature to greater than the absolute maximum temperature of 150°C.

Operating from split supplies greatly reduces the power dissipated when the output is shorted. Operating on ±15-V supplies can only cause a temperature rise of 21°C in the 8-pin SOIC and 30°C in the 5-pin SOT-23 package, assuming the short is to ground.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Handheld Remote Controls

The LM7301 offers outstanding specifications for applications requiring good speed/power trade-off. In applications such as remote control operation, where high bandwidth and low power consumption are needed, the LM7301 performance can easily meet these requirements.

8.1.2 Remote Microphone in Personal Computers

Remote microphones in Personal Computers often use a microphone at the top of the monitor which must drive a long cable in a high noise environment. One method often used to reduce the nose is to lower the signal impedance, which reduces the noise pickup. In this configuration, the amplifier usually requires 30 db to 40 db of gain, at bandwidths higher than most low-power CMOS parts can achieve. The LM7301 offers the tiny package, higher bandwidths, and greater output drive capability than other rail-to-rail input/output parts can provide for this application.

8.1.3 Optical Line Isolation for Modems

The combination of the low distortion and good load driving capabilities of the LM7301 make it an excellent choice for driving opto-coupler circuits to achieve line isolation for modems. This technique prevents telephone line noise from coupling onto the modem signal. Superior isolation is achieved by coupling the signal optically from the computer modem to the telephone lines; however, this also requires a low distortion at relatively high currents. Due to its low distortion at high-output drive currents, the LM7301 fulfills this need, in this and in other telecom applications. See *Stability Considerations* for methods used to ensure stability under all load conditions.

8.2 Typical Applications

The circuit shown in Figure 27 uses the wide supply voltage range (1.8 V to 32 V), rail-to-rail input and output voltage capability, and the unity gain stability of the LM7301 to sense the current flow from the power supply to a load, such as a battery being charged, or any other load. The circuit creates a ground-referenced output voltage, which varies linearly with the load current, for easy interface to the rest of the circuitry to create fault-protection, current and power metering, or current regulation functions.

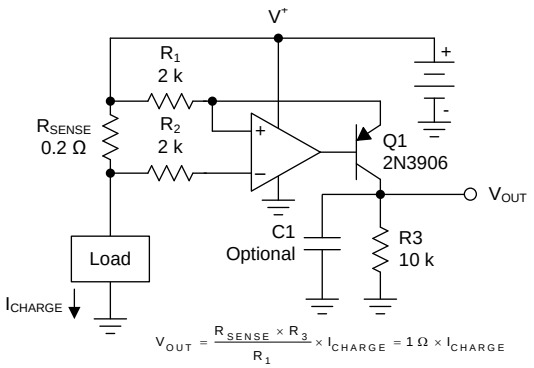


Figure 27. High Side Current Sensing

Typical Applications (continued)

8.2.1 Design Requirements

The output port is designed for easy interface; it is ground-referenced and it produces 0 V with 0 A of load current. A typical stage that follows this stage, an ADC which samples the load current for example, is easily connected to the Q1 collector with no level shifting or additional biasing required.

Apart from a wide supply voltage capability, the operational amplifier used in Figure 27 must have an input voltage range that includes the V+ rail voltage to allow *high side* current sensing. Furthermore, it should be unity gain stable and have an output voltage range which is less than one V_{be} from V+. The LM7301 has all these requirements.

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting R_{SENSE}

Pick the value of R_{SENSE} low enough to minimize its heat / voltage loss while observing Equation 1 for minimum detectable load current, I_{CHARGE_MIN} , and device offset voltage, V_{OS}:

$$R_{SENSE} > \frac{V_{OS}}{I_{CHARGE\_MIN}} \tag{1}$$

With the schematic values shown and LM7301's V_{OS} limit of 6 mV:

$$I_{CHARGE\_MIN} > 30\ mA \tag{2}$$

If the system has the ability to be initialized and corrected for initial readings, it may be possible to lower the value of R_{SENSE}.

8.2.2.2 Selecting R1, and R3 Values

Pick the R3 / R1 ratio to get the proper full-scale V_{OUT} when the maximum load current, I_{CHARGE_MAX}, flows:

$$\frac{R3}{R1} = \frac{V_{OUT}}{R_{SENSE} \times I_{CHARGE\_MAX}} \tag{3}$$

For example, to get 3-V output with 3 A of load current when R_{SENSE} = 0.2 Ω results in:

$$\frac{R3}{R1} = 5 \tag{4}$$

Ensure that the resulting transfer function also satisfies the application's need when the minimum load current, I_{CHARGE_MIN} is being sensed. In this example, the minimum output voltage will be 30 mV (when I_{CHARGE_MIN} = 30 mA).

With the R3/R1 ratio determined, pick the value of R3 for Q1 collector current less than 1 mA at the maximum V_{OUT}, and determine R1 from that.

8.2.2.3 R1, R2 Selection

Normally, R2 is set equal to R1 to cancel out the error term due to the input bias current, I_B (approximately 200 nA for the LM7301).

8.2.2.4 Error Terms Expressions

Here are the expressions for the output change caused by various parameter shifts, evaluated for Figure 27 values with I_{CHARGE_MAX}= 3 A:

Offset Voltage, ΔV_{OS}:

$$\Delta V_{OUT} = \frac{\Delta V_{OS} \times R3}{R1} = 5\Delta V_{OS} \tag{5}$$

Offset current, I_{OS}:

$$\Delta V_{OUT} = \frac{\Delta I_{OS} \times R2 \times R3}{R1} = I_{OS} \times 10\ k \tag{6}$$

Typical Applications (continued)

Self-heating of R_{SENSE} causing ΔR_{SENSE} with I_{CHARGE_MAX} flowing:

$$\Delta V_{OUT} = \Delta R_{SENSE} \times I_{CHARGE\_MAX} \times \frac{R3}{R1} = \Delta R_{SENSE} \times 15 \quad (7)$$

8.2.2.5 Frequency Response

Depending on the application, it may be useful to have the means to control the upper end of the circuit's frequency response. An example is limiting the circuit's response to high-frequency load current spikes or switching frequencies so that the circuit only reacts to DC or lower frequencies. Capacitor C1 in Figure 27 can be used to accomplish just that. The original circuit has a –3-dB bandwidth close to 4.5 MHz which can be reduced by increasing the value of C1, as shown in Figure 28.

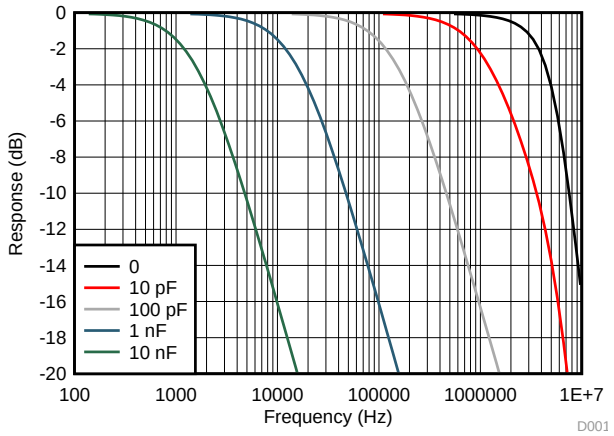
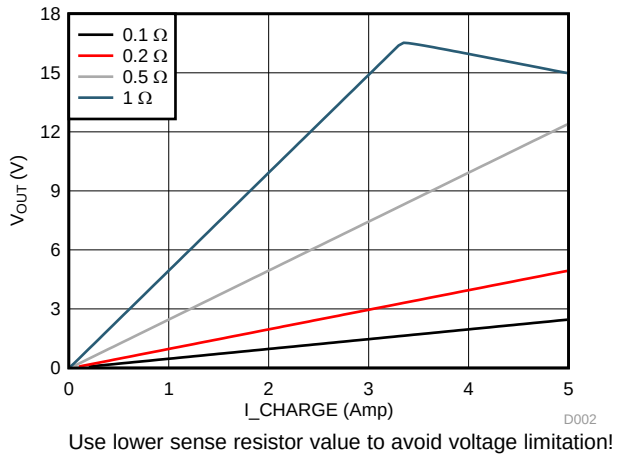


Figure 28. Current Sense Frequency Response vs C1 Value

8.2.3 Application Curves

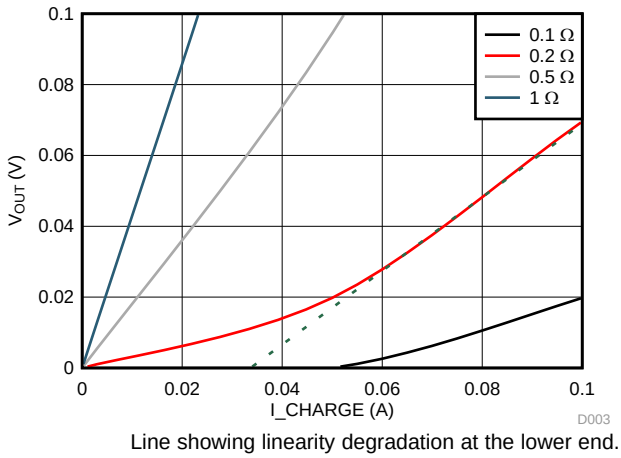
Figure 29 shows the transfer function of the circuit for several values of R_{SENSE}. Notice that with 1 Ω, the output is limited to approximately 16 V because of the additional drop across the sense resistor at higher load currents.

Figure 30 shows the low-end of the load current is more non-linear for low RSENSE values, as noted in *Selecting R_{SENSE}* due to V_{OS}. Higher R_{SENSE} values help with this at the expense of a higher loss and voltage drop.



Use lower sense resistor value to avoid voltage limitation!

Figure 29. Current Sense Transfer Function for Various R_{SENSE} Values



Line showing linearity degradation at the lower end.

Figure 30. Low-End Transfer Function for Various R_{SENSE}

9 Power Supply Recommendations

The LM7301 is specified for operation from 1.8 V to 32 V (±0.9 V to ±16 V). Being a rail-to-rail input and output device, any operating voltage conditions within the supply voltage range can be accommodated.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, TI recommends good printed-circuit board (PCB) layout practices. Low-loss, 0.1-μF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single supply applications.

10.2 Layout Example

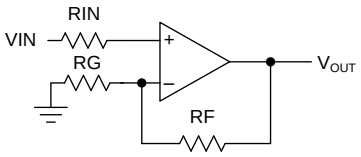


Figure 31. Schematic Representation

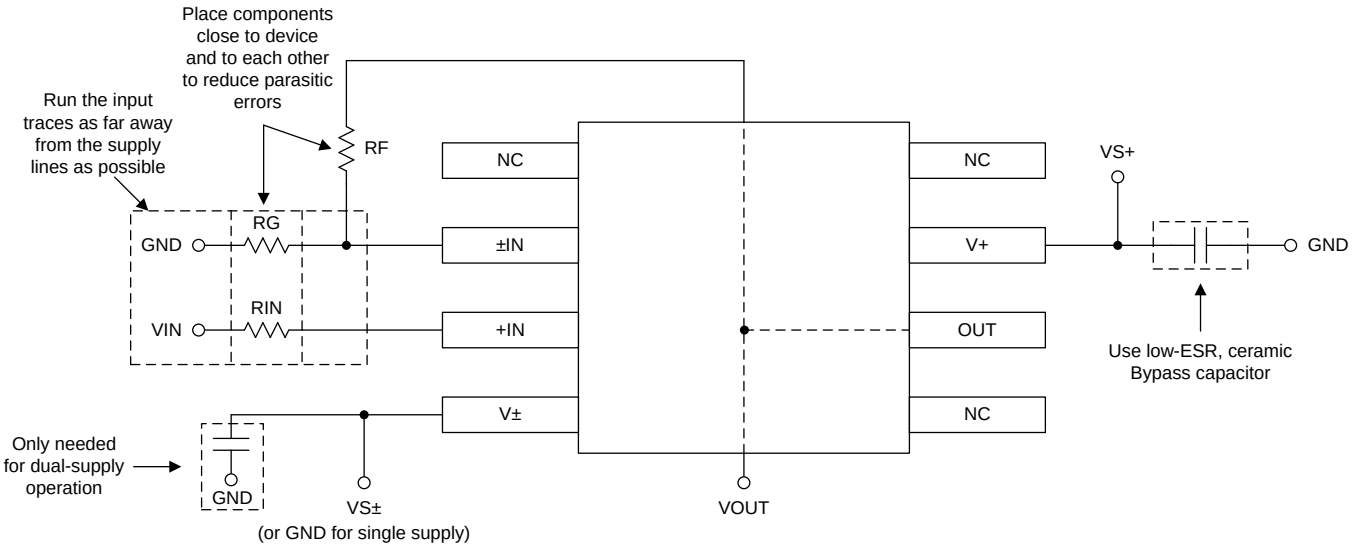


Figure 32. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7301IM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM73 01IM	
LM7301IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM73 01IM	Samples
LM7301IM5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A04A	
LM7301IM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A04A	Samples
LM7301IM5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A04A	
LM7301IM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A04A	Samples
LM7301IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM73 01IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

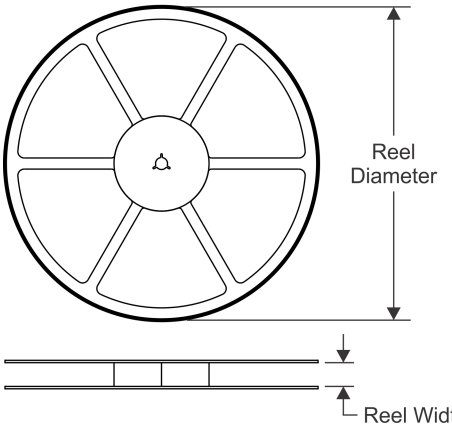
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

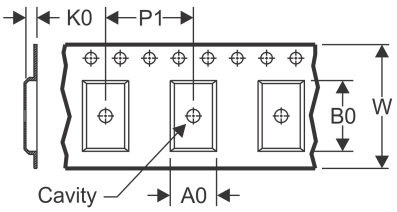
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

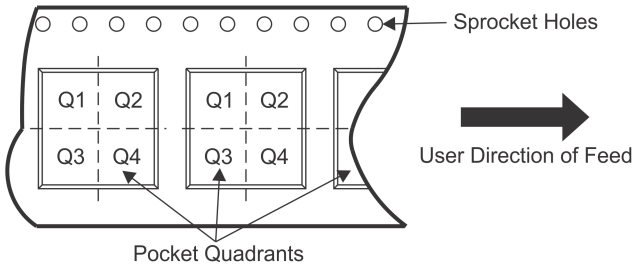


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

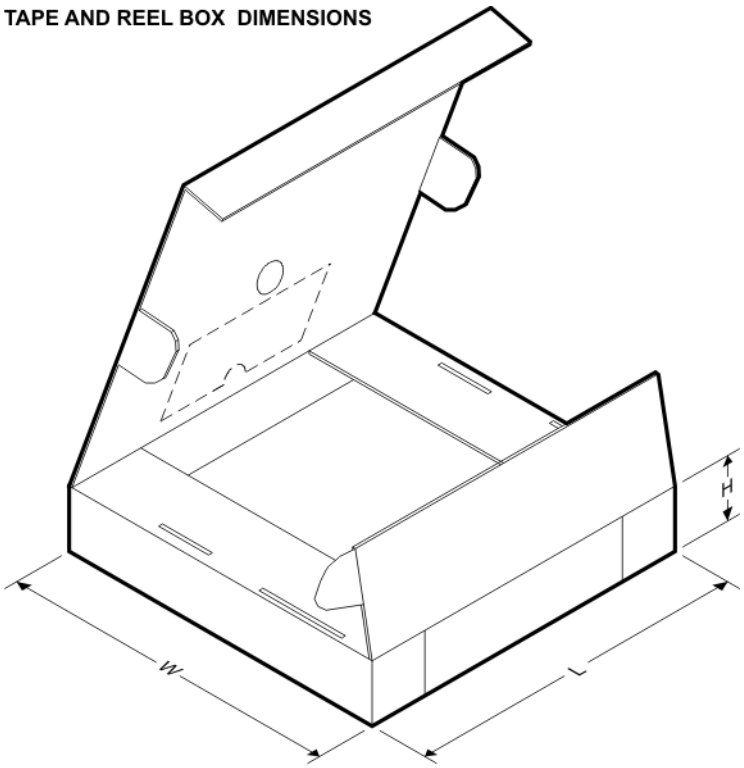
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7301IM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7301IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

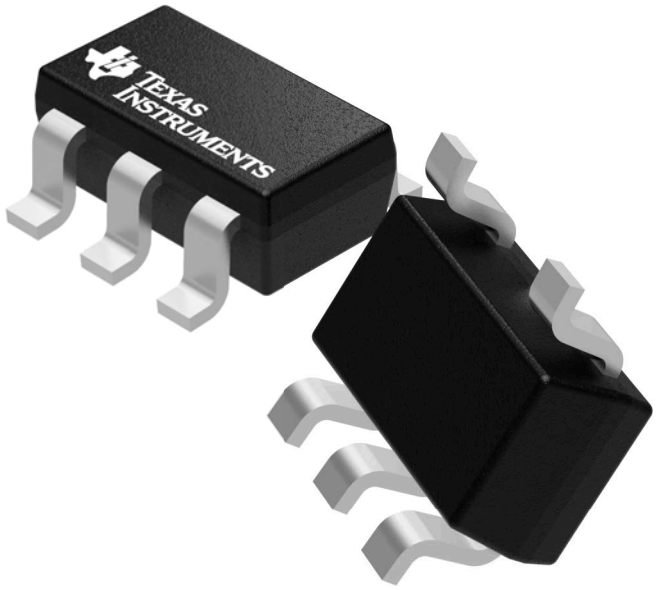


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7301IM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM7301IM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM7301IM5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7301IM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7301IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



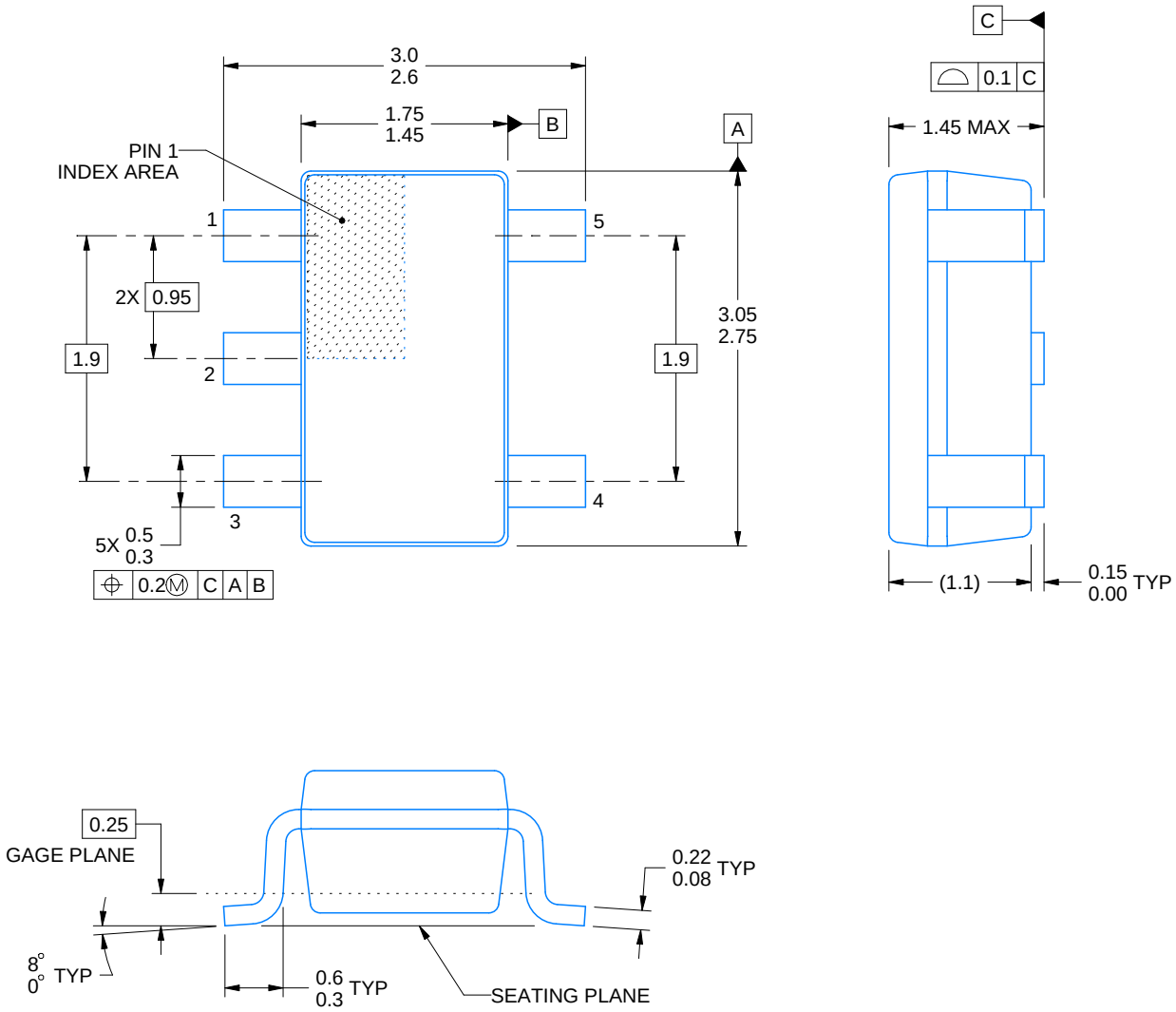
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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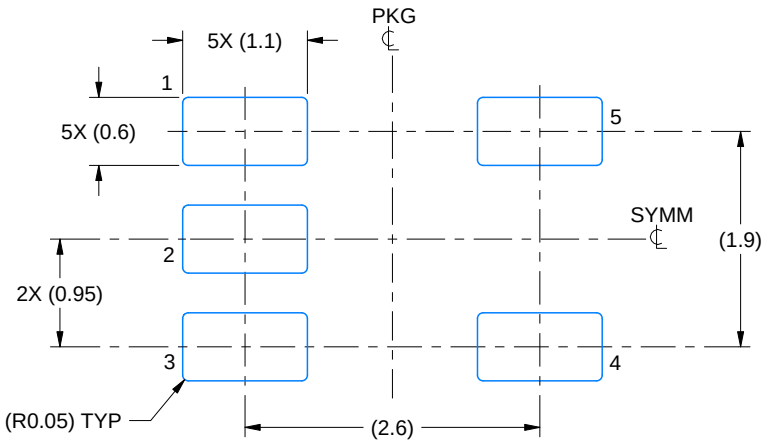
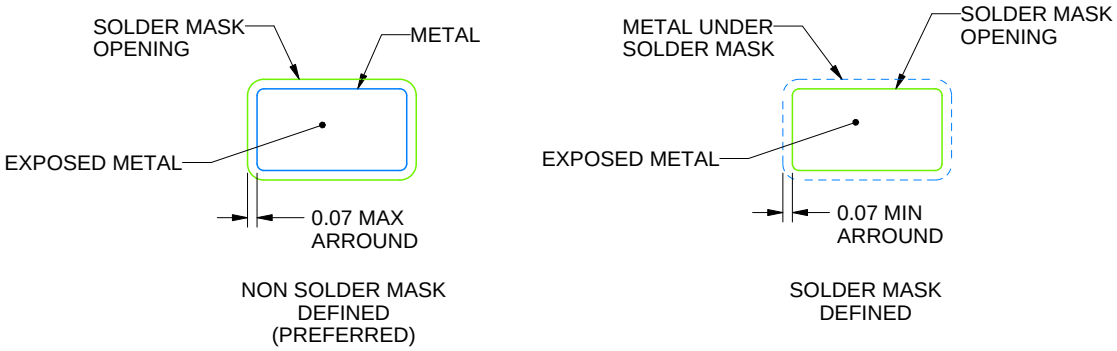
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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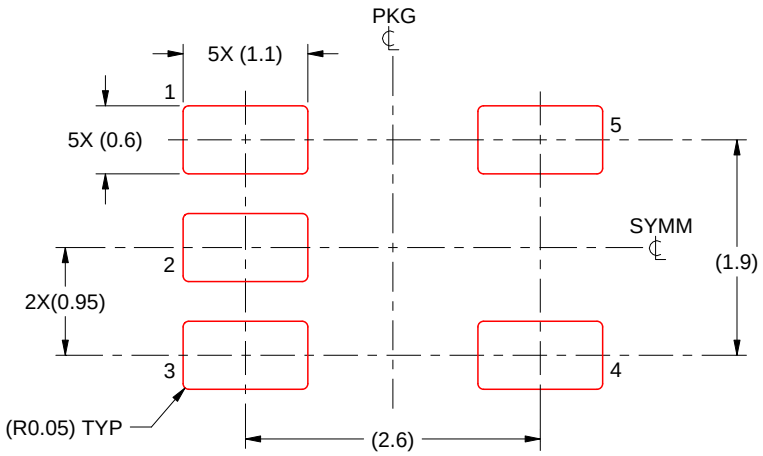
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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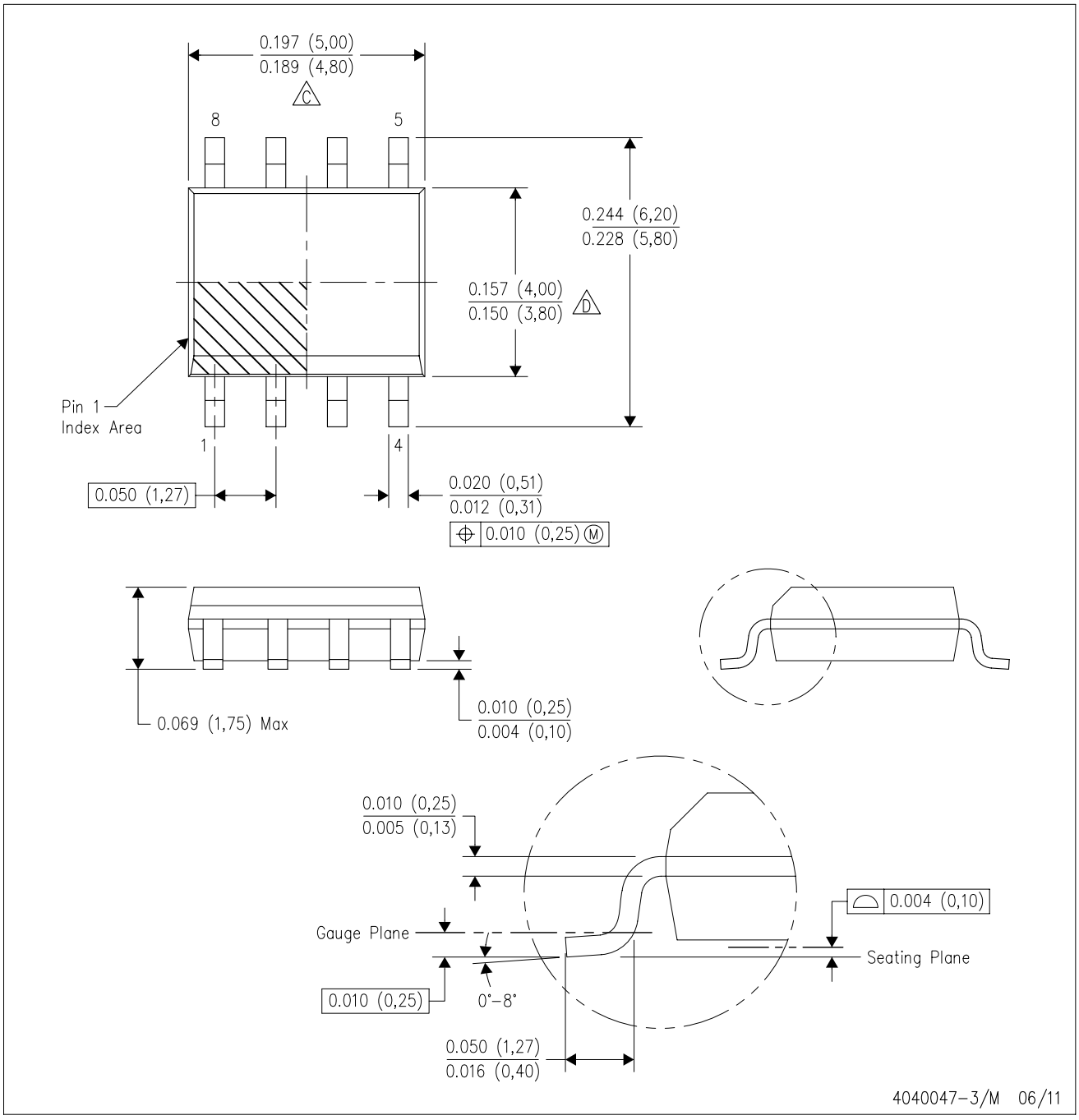
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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