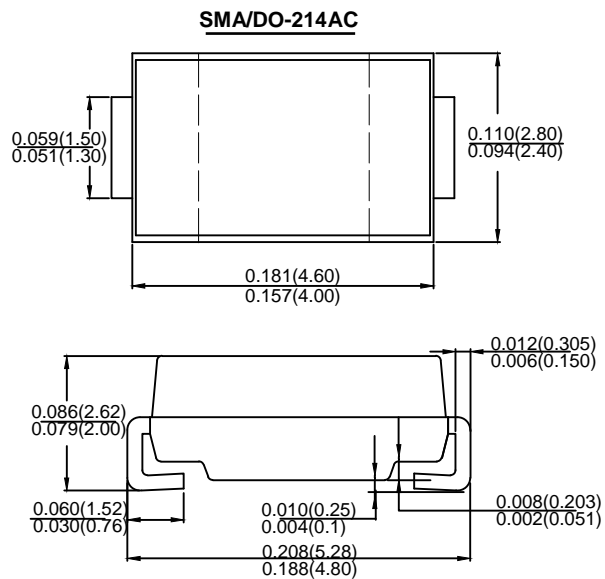


Features

- Schottky Brier Chip
- Low Power Loss,High Efficiency
- Ideally Suited for Automatic Assembly
- Surge Overload Rating to 100APeak
- Plastic Case Material has UL Flammability Classification Rating 94V-0

Mechanical Data

- Case: Molded plastic SMA
- Terminals: Plated leads solderable per MIL-STD-750,Method 2026 guaranteed
- Polarity: Color band denotes cathode end
- Mounting Position: Any
- Making: Type Number



Dimensions in inches and (millimeters)

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load

For capacitive load derate current by 20%

Type Number	SYMBOL	SS 52	SS 53	SS 54	SS 545	SS 55	SS 56	SS 58	SS 510	SS 515	SS 520	SS 525	Unit	
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	20	30	40	45	50	60	80	100	150	200	250	V	
Maximum RMS Voltage	V_{RMS}	14	21	28	31	35	42	56	70	105	140	175	V	
Maximum DC Blocking Voltage	V_{DC}	20	30	40	45	50	60	80	100	150	200	250	V	
Average Rectified Output Current @ $T_L = 100^\circ C$	$I_F(AV)$	5.0											A	
Peak Forward Surge Current 8.3ms Single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	100											A	
Rating for fusing ($t < 8.3ms$)	$I^2 t$	41.50											A ² s	
Forward Voltage @ $I_F = 5.0A$ (Note 1)	V_{FM}	0.55			0.7		0.85		0.92		0.95		V	
Peak Reverse Current @ $T_A = 25^\circ C$	I_R	0.1						0.05						mA
At Rated DC Blocking Voltage @ $T_A = 100^\circ C$		10						5						
Typical Junction Capacitance	C_J	28											pF	
Typical Thermal Resistance per leg (Note 2)	$R_{\theta JA}$	88											°C/W	
Operating Temperature Range	T_J	-55 to +150											°C	
Storage Temperature Range	T_{STG}	-55 to +150											°C	

Note: 1. Pulse Test with PW=300usec, 1%Duty Cycle.

2. Mounted on P.C.Board with 5.0 mm² (0.13mm thick) copper pad areas.

Fig. 1 Forward Current Derating Curve

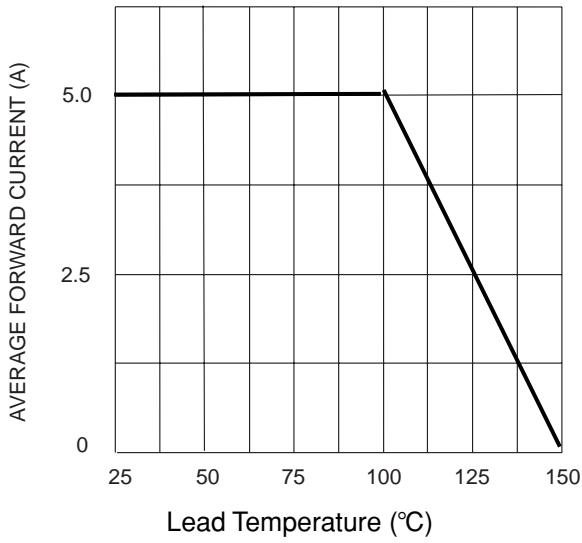


Fig. 2 Typ. Forward Characteristics

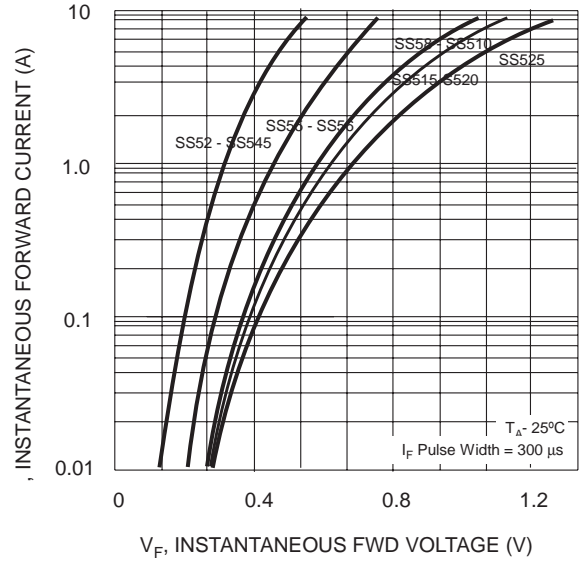


Fig. 3 Max Non-Repetitive Peak Fwd Surge Current

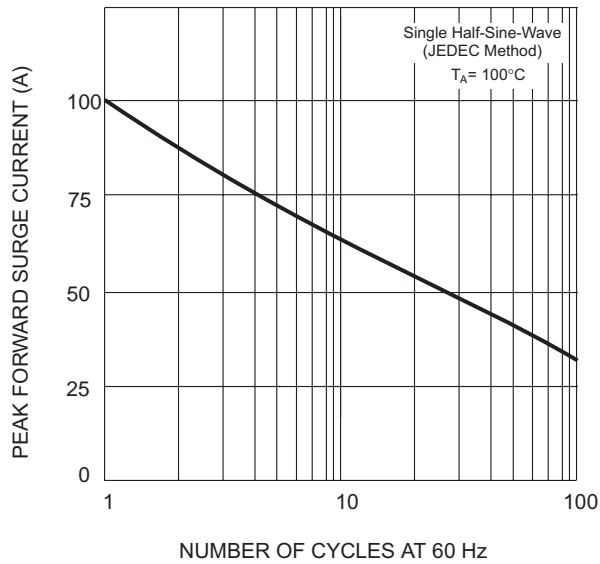
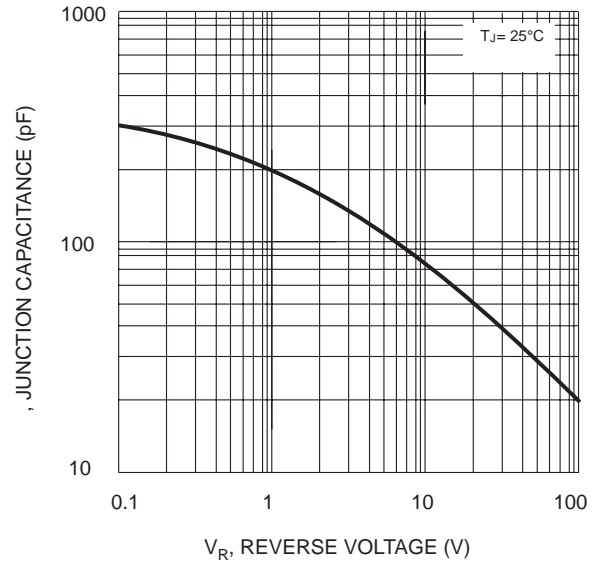
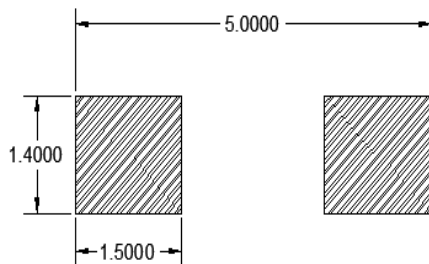


Fig. 4 Typical Junction Capacitance



SMA PAD LAYOUT



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