Wideband, Fixed Gain Video BUFFER AMPLIFIER With Disable

FEATURES

- FLEXIBLE SUPPLY RANGE:
  +5V to +12V Single Supply
  ±2.5V to ±6V Dual Supplies
- INTERNALLY FIXED GAIN: +2 or ±1
- HIGH BANDWIDTH (G = +2): 225MHz
- LOW SUPPLY CURRENT: 5.1mA
- LOW DISABLED CURRENT: 150µA
- HIGH OUTPUT CURRENT: 190mA
- OUTPUT VOLTAGE SWING: ±4.0V
- SOT23-6 AVAILABLE

APPLICATIONS

- BROADBAND VIDEO LINE DRIVERS
- MULTIPLE LINE VIDEO DA
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS

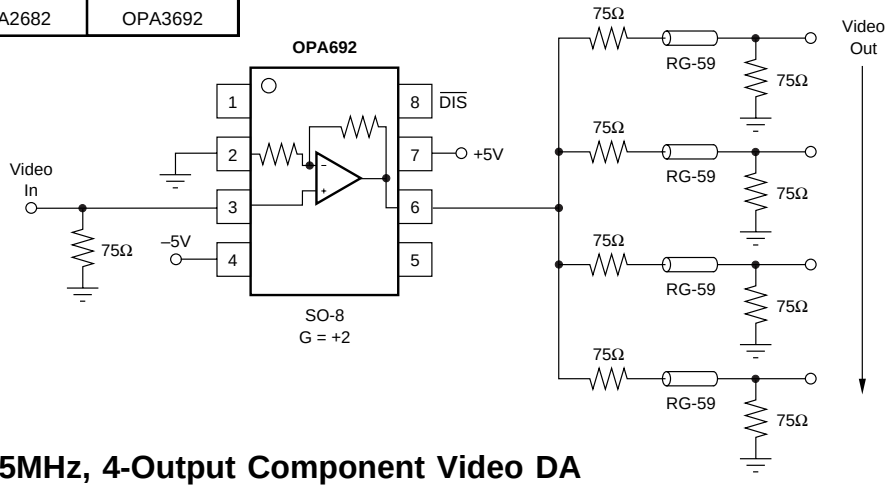
OPA692 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage-Feedback	OPA690	OPA2690	OPA3690
Current-Feedback	OPA691	OPA2691	OPA3691
Fixed Gain	OPA682	OPA2682	OPA3692

DESCRIPTION

The OPA692 provides an easy to use, broadband fixed gain video buffer amplifier. Depending on the external connections, the internal resistor network may be used to provide either a fixed gain of +2 video buffer or a gain of +1 or –1 voltage buffer. Operating on a very low 5.1mA supply current, the OPA692 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers high output current with minimal headroom and crossover distortion. This gives exceptional single-supply operation. Using a single +5V supply, the OPA692 can deliver a 1V to 4V output swing with over 120mA drive current and > 200MHz bandwidth. This combination of features makes the OPA692 an ideal RGB line driver or single-supply Analog-to-Digital Converter (ADC) input driver.

The low 5.1mA supply current for the OPA692 is precisely trimmed at +25°C. This trim, along with low drift over temperature, ensures a lower maximum supply current than competing products that report only a room temperature nominal supply current. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA692 supply current drops to less than 150µA while the I/O pins go into a high-impedance state.



225MHz, 4-Output Component Video DA

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation(2)	See Thermal Information
Differential Input Voltage(3)	±1.2V
Input Voltage Range	±V_S
Storage Temperature Range: D, DVB	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C
ESD Resistance: HBM	2kV
MM	200V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed. (3) Noninverting input to internal inverting node.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

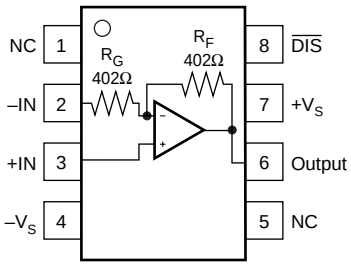
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA692ID	SO-8 Surface-Mount	D	–40°C to +85°C	OPA692	OPA692ID	Rails, 100
"	"	"	"	"	OPA692IDR	Tape and Reel, 2500
OPA692IDBV	SOT23-6	DBV	–40°C to +85°C	OAGI	OPA692IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA692IDBVR	Tape and Reel, 3000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

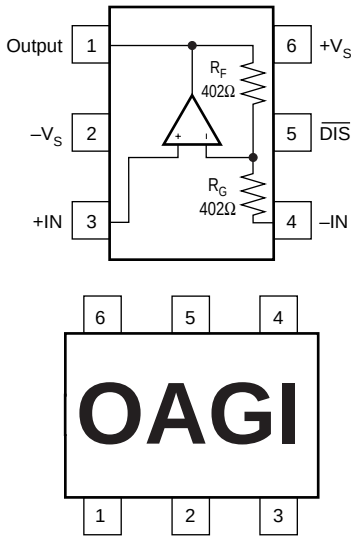
PIN CONFIGURATION

Top View **SO**



NC: No Connection

Top View **SOT**



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

G = +2 (–IN grounded) and $R_L = 100\Omega$ (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA692ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth ($V_O < 0.5V_{PP}$)	G = +1	280				MHz	typ	C
	G = +2	225	185	180	170	MHz	min	B
	G = –1	220				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O < 0.5V_{PP}$	120	40	35	30	MHz	min	B
Peaking at a Gain of +1	$V_O < 0.5V_{PP}$	0.2	1	1.5	2	dB	max	B
Large-Signal Bandwidth	G = +2, $V_O = 5V_{PP}$	220				MHz	typ	C
Slew Rate	G = +2, 4V Step	2000	1400	1375	1350	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.6				ns	typ	C
	G = +2, V_O = 5V Step	1.9				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–69	–62	–59	–57	dBc	max	B
	$R_L \geq 500\Omega$	–79	–70	–67	–65	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–76	–72	–70	–68	dBc	max	B
	$R_L \geq 500\Omega$	–94	–87	–82	–78	dBc	max	B
Input Voltage Noise	f > 1MHz	1.7	2.5	2.9	3.1	nV/$\sqrt{Hz}$	max	B
Noninverting Input Current Noise	f > 1MHz	12	14	15	15	pA/$\sqrt{Hz}$	max	B
Inverting Input Current Noise	f > 1MHz	15	17	18	19	pA/$\sqrt{Hz}$	max	B
Differential Gain	NTSC, $R_L = 150\Omega$	0.07				%	typ	C
	NTSC, $R_L = 37.5\Omega$	0.17				%	typ	C
Differential Phase	NTSC, $R_L = 150\Omega$	0.02				deg	typ	C
	NTSC, $R_L = 37.5\Omega$	0.07				deg	typ	C
DC PERFORMANCE[3]								
Gain Error	G = +1	±0.2				%	typ	C
	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	max	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G								
Maximum		402	**457**	462	464	Ω	max	A
Minimum		402	**347**	342	340	Ω	min	A
Average Drift			0.13	0.13	0.13	%/C°	max	B
Input Offset Voltage	V_{CM} = 0V	±0.5	**±2.5**	±3.2	±3.9	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+15	**+35**	+43	+45	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			–300	–300	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±5	**±25**	±30	±40	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±90	±200	nA°C	max	B
INPUT								
Common-Mode Input Range		±3.5	**±3.4**	±3.3	±3.2	V	min	B
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing		+190	**+160**	+140	+100	mA	min	A
Sinking		–190	**–160**	–140	–100	mA	min	A
Short-Circuit Current	V_O = 0	±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.12				Ω	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications. (2) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

Boldface limits are tested at **+25°C.**

G = +2 (–IN grounded) and R_L = 100Ω (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA692ID, IDBV						TEST LEVEL(2)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	
DISABLE/POWER DOWN ($\overline{DIS}$ Pin)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–150	**–300**	–350	–400	µA	max	A
Disable Time	V_{IN} = +1V_{DC}	1				µs	typ	C
Enable Time	V_{IN} = +1V_{DC}	25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω	±50				mV	typ	C
Turn-Off Glitch	G = +2, R_L= 150Ω	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current	$V_{\overline{DIS}}$ = 0	75	**130**	150	160	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Maximum Quiescent Current	V_S = ±5V	5.1	**5.3**	5.5	5.8	mA	max	A
Minimum Quiescent Current	V_S = ±5V	5.1	**4.9**	4.5	4.25	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	58	**52**	50	49	dB	min	A
TEMPERATURE RANGE								
Specification: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications. (2) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

G = +2 (–IN grounded though 0.1µF) and R_L = 100Ω to V_S/2 (see Figure 2 for AC performance only), unless otherwise noted.

		OPA692ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(1)	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL(2)
AC PERFORMANCE (see Figure 2)								
Small-Signal Bandwidth (V_O < 0.5V_{PP})	G = +1	240				MHz	typ	C
	G = +2	190	168	160	140	MHz	min	B
	G = –1	195				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}	90	40	30	25	MHz	min	B
Peaking at a Gain of +1	V_O < 0.5V_{PP}	0.2	1	2.5	3	dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	210				MHz	typ	C
Slew Rate	G = +2, 2V Step	830	600	575	550	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	2.0				ns	typ	C
	G = +2, V_O = 2V Step	2.3				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	14				ns	typ	C
0.1%	G = +2, V_O = 2V Step	10				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–66	–58	–57	–56	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–73	–65	–63	–62	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–72	–68	–67	–65	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–77	–72	–70	–69	dBc	max	B
Input Voltage Noise	f > 1MHz	1.7	2.5	2.9	3.1	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	12	14	15	15	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	15	17	18	19	pA/√Hz	max	B
DC PERFORMANCE(3)								
Gain Error	G = +1	±0.2				%	typ	C
	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	max	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G								
Maximum		402	457	462	464	Ω	max	B
Minimum		402	347	342	340	Ω	min	B
Average Drift			0.13	0.13	0.13	%/C°	max	B
Input Offset Voltage	V_{CM} = 2.5V	±0.5	**±3**	±3.6	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 2.5V	+20	**+40**	+46	+56	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 2.5V			–250	–250	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 2.5V	±5	**±25**	±30	±40	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 2.5V			±112	±200	nA°C	max	B
INPUT								
Least Positive Input Voltage		1.5	1.6	1.7	1.8	V	max	B
Most Positive Input Voltage		3.5	3.4	3.3	3.2	V	min	B
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4.0	**3.8**	3.7	3.5	V	min	A
	R_L = 100Ω	3.9	**3.7**	3.6	3.4	V	min	A
Least Positive Output Voltage	No Load	1.0	**1.2**	1.3	1.5	V	max	A
	R_L = 100Ω	1.1	**1.3**	1.4	1.6	V	max	A
Current Output, Sourcing		+160	**+120**	+100	+80	mA	min	A
Sinking		–160	**–120**	–100	–80	mA	min	A
Short-Circuit Current	V_O = V_S/2	±250				mA	typ	C
Output Impedance	G = +2, f = 100kHz	0.12				Ω	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications. (2) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: V_S = +5V (Cont.)

Boldface limits are tested at **+25°C.**

G = +2 (–IN grounded though 0.1µF) and R_L = 100Ω to V_S/2 (see Figure 2 for AC performance only), unless otherwise noted.

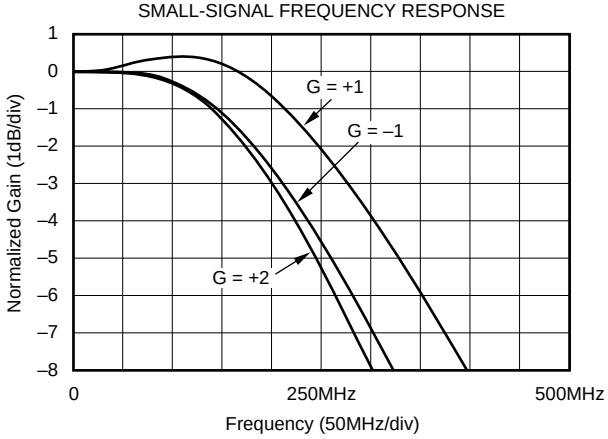
PARAMETER	CONDITIONS	OPA692ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C(1)	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL(2)
DISABLE/POWER DOWN ($\overline{DIS}$ Pin)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–150	–300	–350	–400	µA	typ	C
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±50				mV	typ	B
Turn-Off Glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±20				mV	typ	B
Enable Voltage		3.3	3.5	3.6	3.7	V	min	B
Disable Voltage		1.8	1.7	1.6	1.5	V	max	B
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	75	130	150	160	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			**12**	12	12	V	max	A
Maximum Quiescent Current	V_S = +5V	4.5	**4.8**	5.0	5.2	mA	max	A
Minimum Quiescent Current	V_S = +5V	4.5	**4.1**	3.8	3.7	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	55				dB	typ	C
TEMPERATURE RANGE								
Specification: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications. (2) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

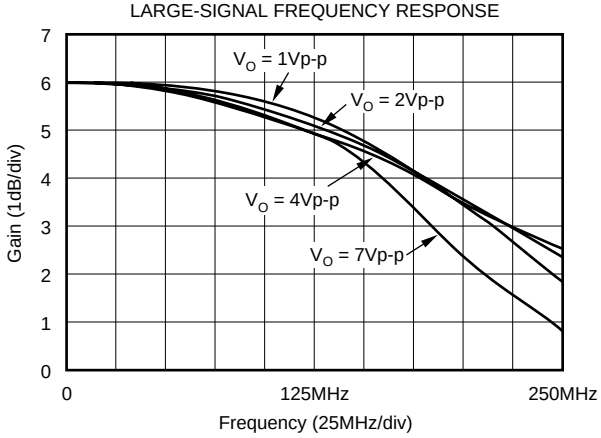
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = +25°C, G = +2, and R_L = 100Ω (see Figure 1 for DC performance only), unless otherwise noted.

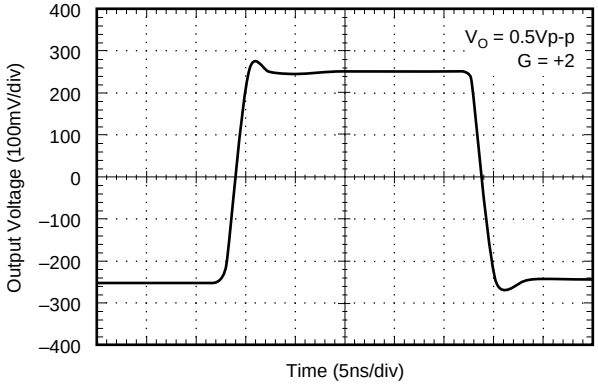
SMALL-SIGNAL FREQUENCY RESPONSE



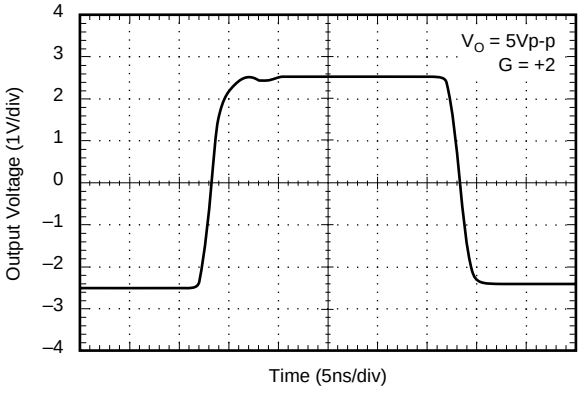
LARGE-SIGNAL FREQUENCY RESPONSE



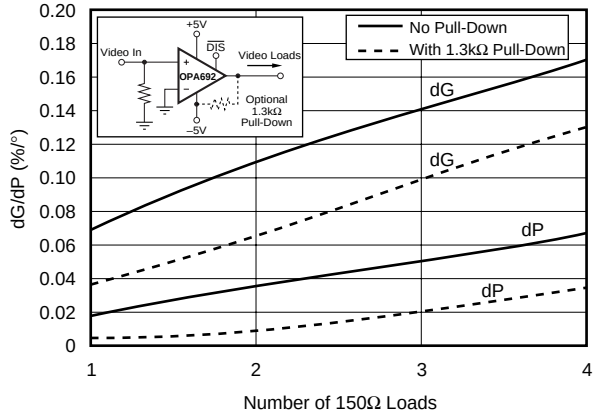
SMALL-SIGNAL PULSE RESPONSE



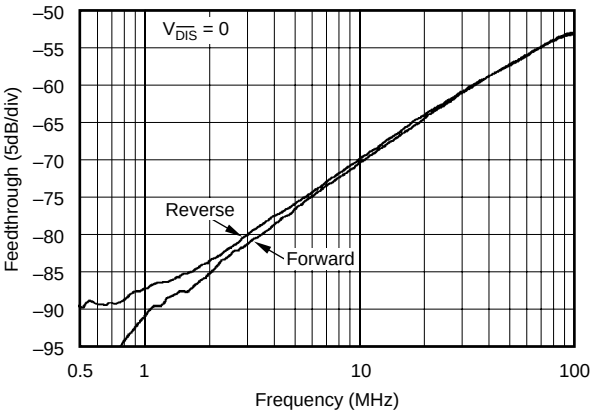
LARGE-SIGNAL PULSE RESPONSE



COMPOSITE VIDEO dG/dP



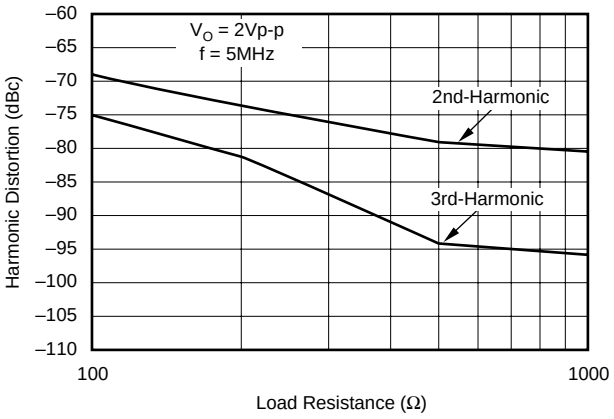
DISABLED FEEDTHROUGH vs FREQUENCY



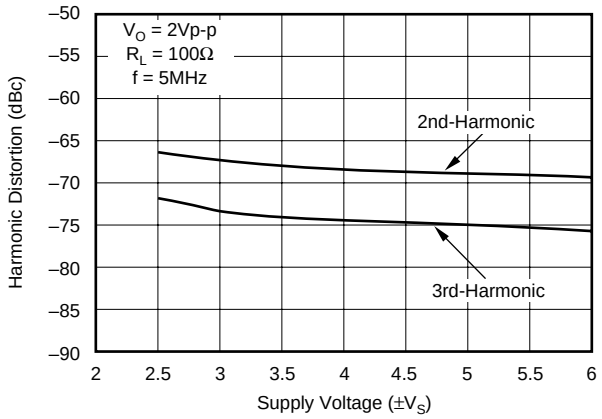
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, and R_L = 100Ω (see Figure 1 for DC performance only), unless otherwise noted.

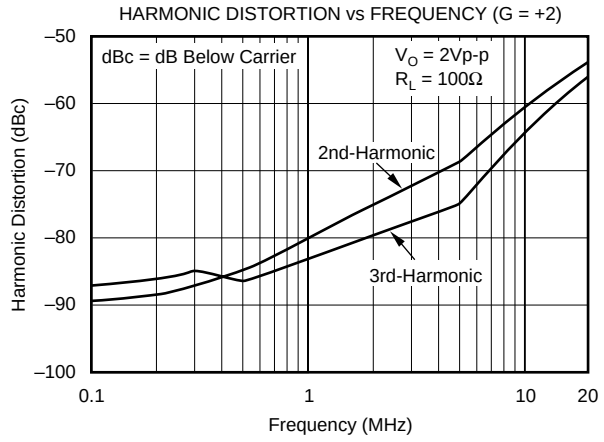
HARMONIC DISTORTION vs LOAD RESISTANCE



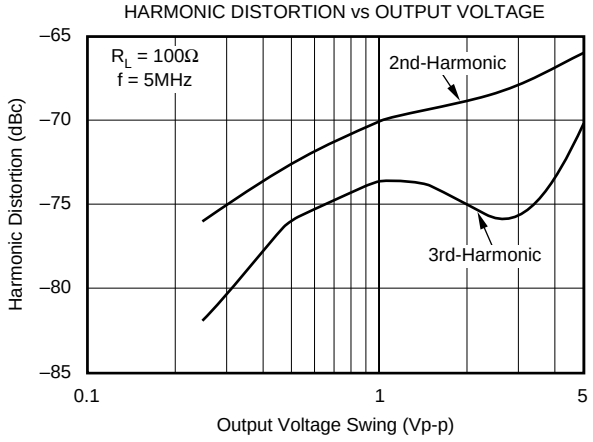
5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



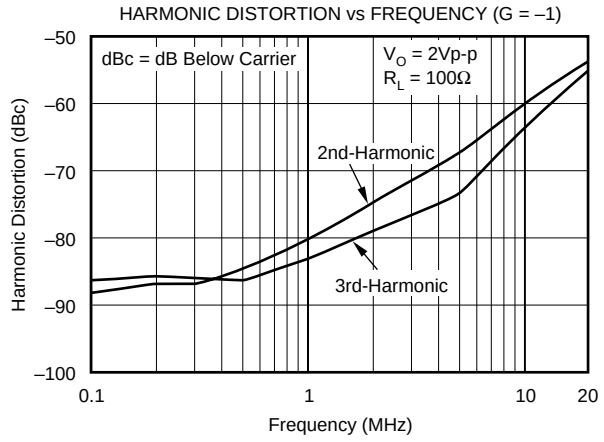
HARMONIC DISTORTION vs FREQUENCY (G = +2)



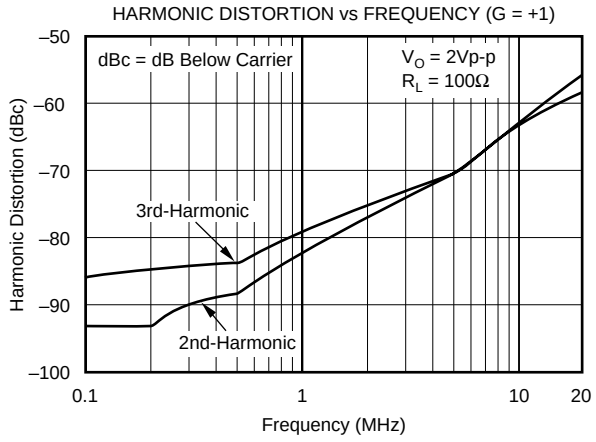
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs FREQUENCY (G = –1)



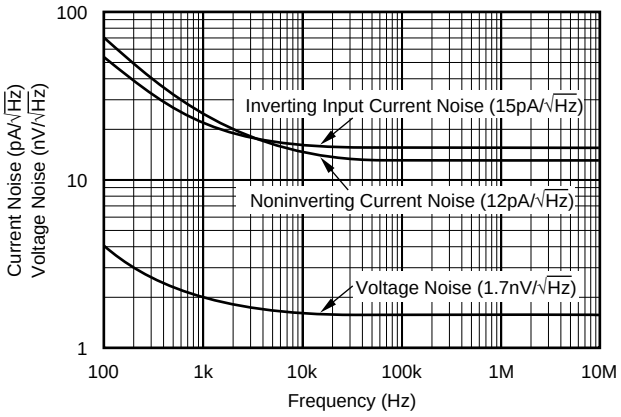
HARMONIC DISTORTION vs FREQUENCY (G = +1)



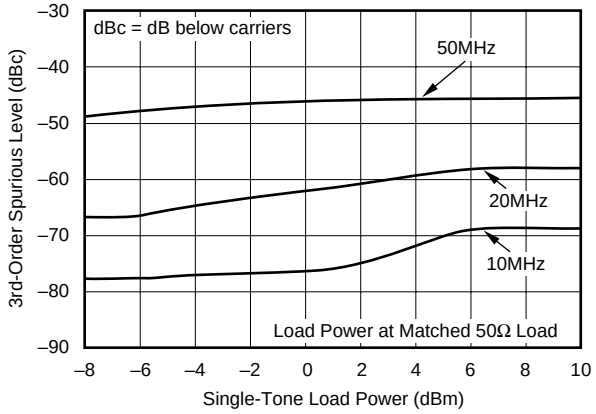
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, and R_L = 100Ω (see Figure 1 for DC performance only), unless otherwise noted.

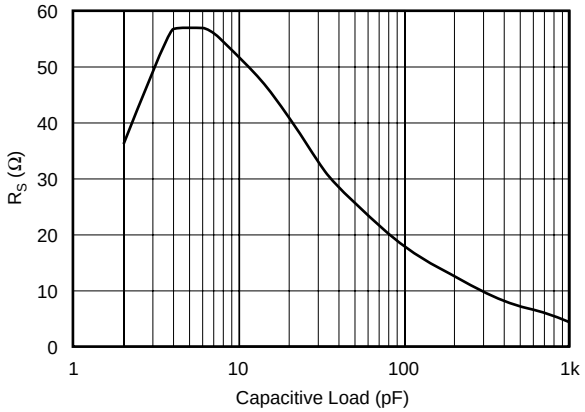
INPUT VOLTAGE AND CURRENT NOISE DENSITY



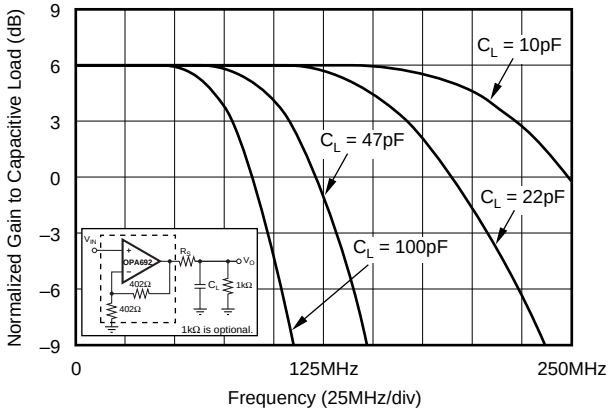
2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



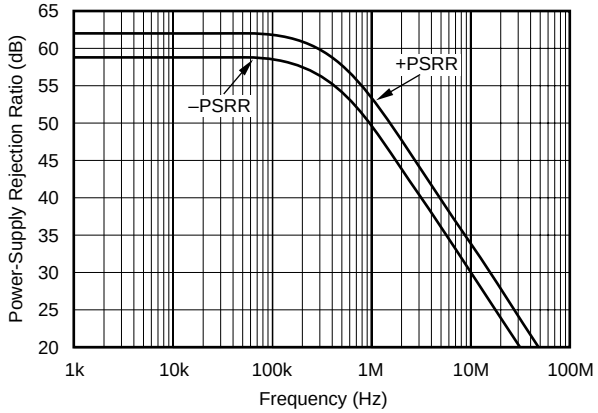
RECOMMENDED R_S vs CAPACITIVE LOAD



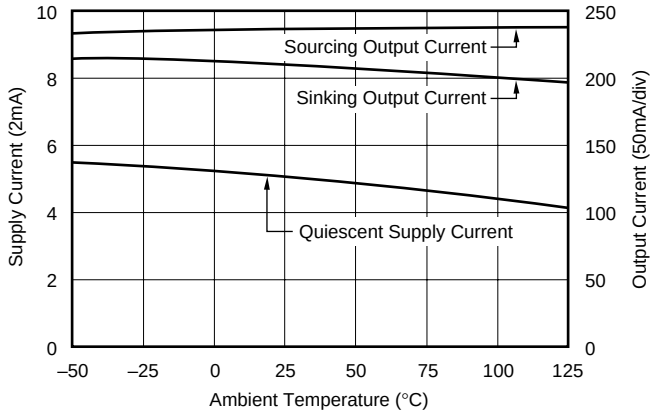
FREQUENCY RESPONSE vs CAPACITIVE LOAD



PSRR vs FREQUENCY



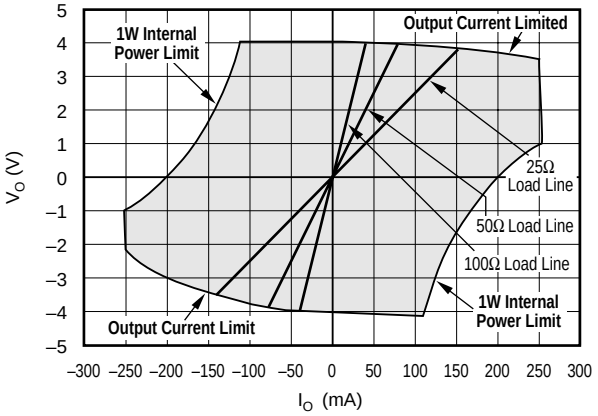
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



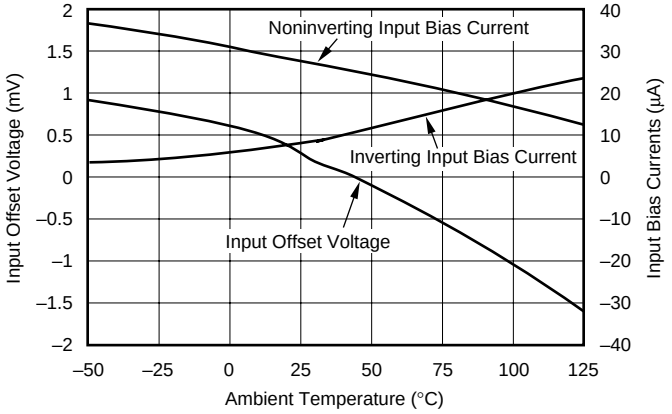
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2, and R_L = 100Ω (see Figure 1 for DC performance only), unless otherwise noted.

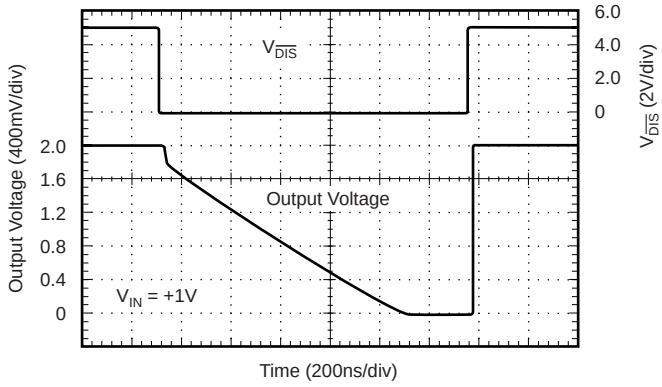
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



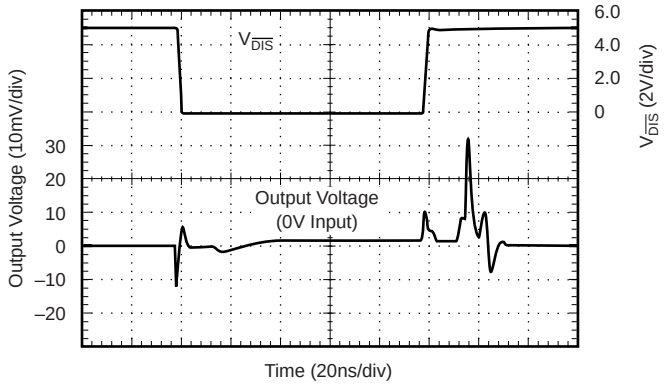
TYPICAL DC DRIFT OVER TEMPERATURE



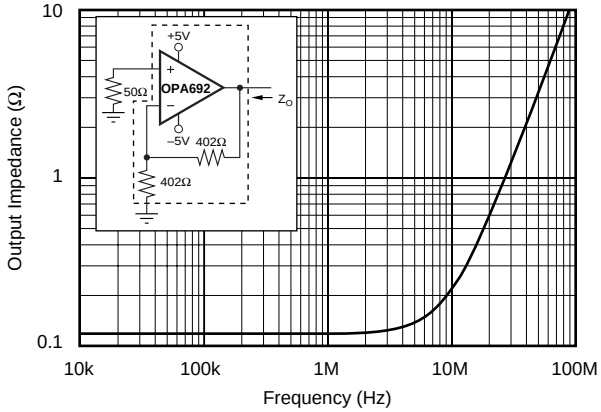
LARGE-SIGNAL DISABLE/ENABLE RESPONSE



DISABLE/ENABLE GLITCH



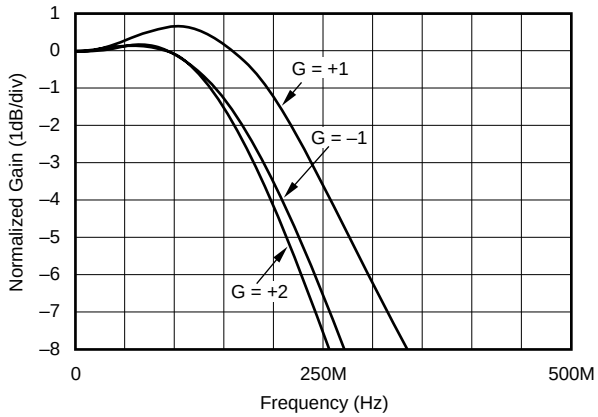
CLOSED-LOOP OUTPUT IMPEDANCE



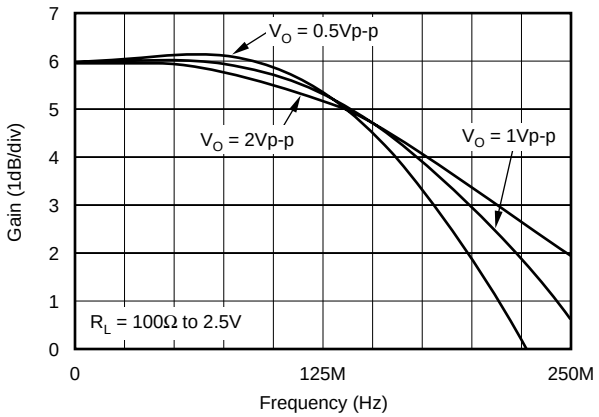
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = +25°C, G = +2, and R_L = 100Ω (see Figure 2 for AC performance only), unless otherwise noted.

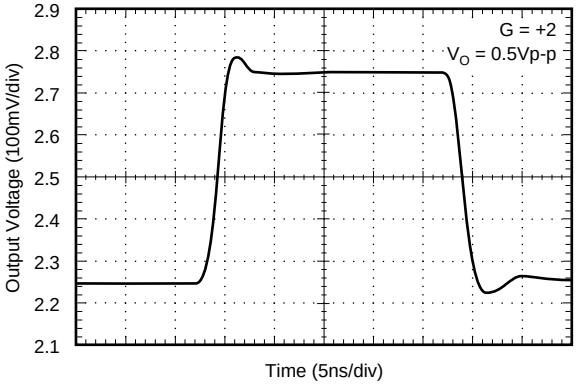
SMALL-SIGNAL FREQUENCY RESPONSE



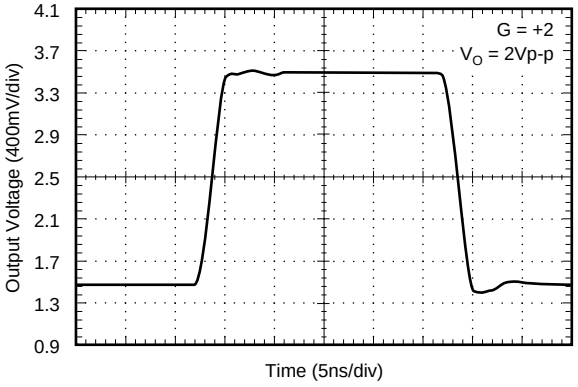
LARGE-SIGNAL FREQUENCY RESPONSE



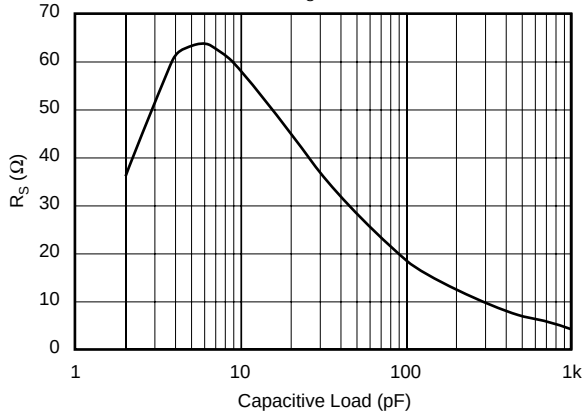
SMALL-SIGNAL PULSE RESPONSE



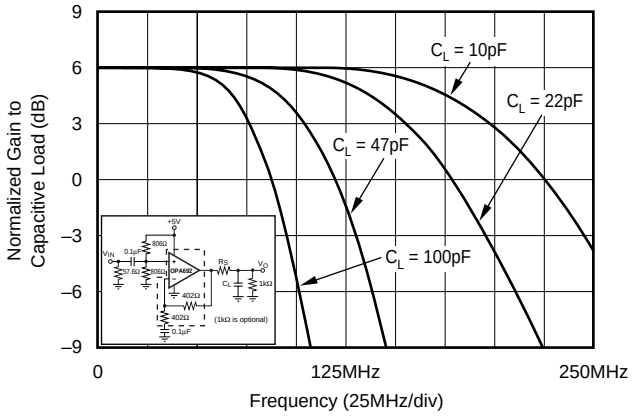
LARGE-SIGNAL PULSE RESPONSE



RECOMMENDED R_S vs CAPACITIVE LOAD



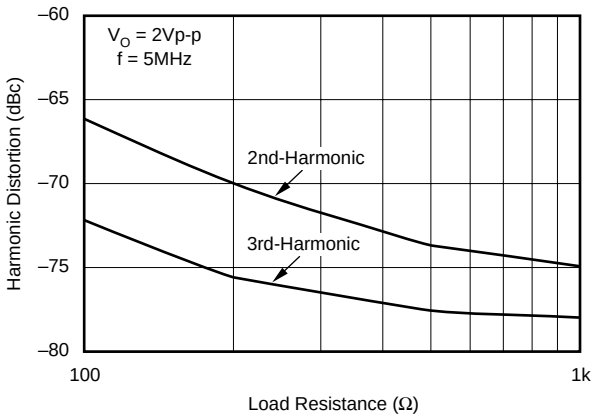
FREQUENCY RESPONSE vs CAPACITIVE LOAD



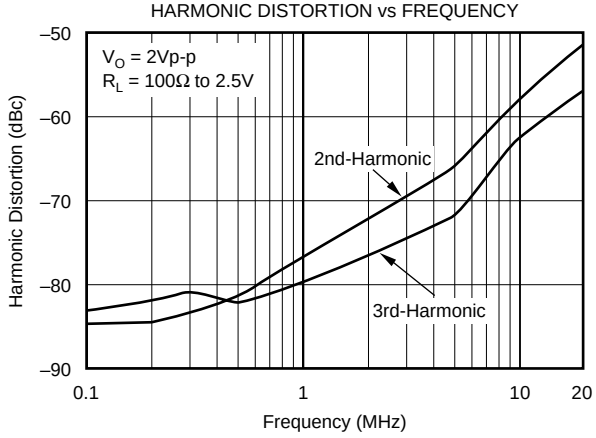
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

T_A = +25°C, G = +2, and R_L = 100Ω (see Figure 2 for AC performance only), unless otherwise noted.

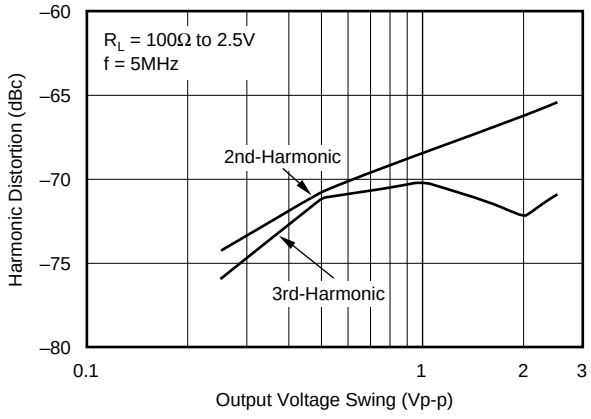
HARMONIC DISTORTION vs LOAD RESISTANCE



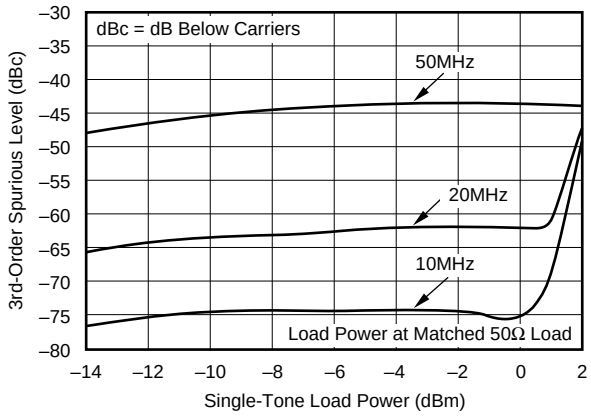
HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs OUTPUT VOLTAGE



2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



APPLICATIONS INFORMATION

WIDEBAND BUFFER OPERATION

The OPA692 gives the exceptional AC performance of a wideband current-feedback op amp with a highly linear, high-power output stage. It features internal R_F and R_G resistors that make it easy to select a gain of +2, +1, or –1 without any external resistors. Requiring only 5.1mA quiescent current, the OPA692 will swing to within 1V of either supply rail and deliver in excess of 160mA at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA692 will deliver greater than 200MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers have typically suffered from very poor crossover distortion as the output current goes through zero. The OPA692 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 804Ω = 89Ω. The disable control line ($\overline{DIS}$) is typically left open to ensure normal amplifier operation. In addition to the usual power-supply decoupling capacitors to ground, a 0.1µF capacitor can be included between the two power-supply pins. This optional added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

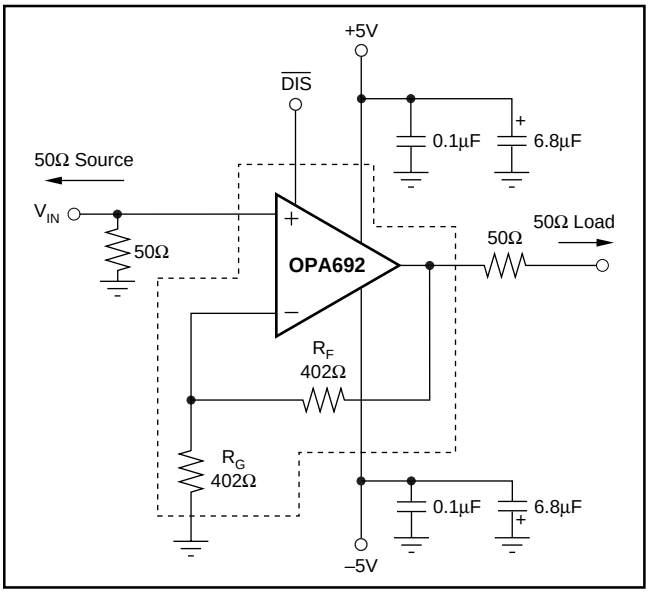


FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

Figure 2 shows the AC-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a *rail-to-rail* design, the OPA692 requires minimal input and output voltage headroom compared to other very wideband current-feedback op amps. It will deliver a $3V_{PP}$ output swing on a single +5V supply with greater than 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 2 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a $2V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1—which puts the input DC bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 120mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA692 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, 3rd-harmonic distortion typical characteristics.

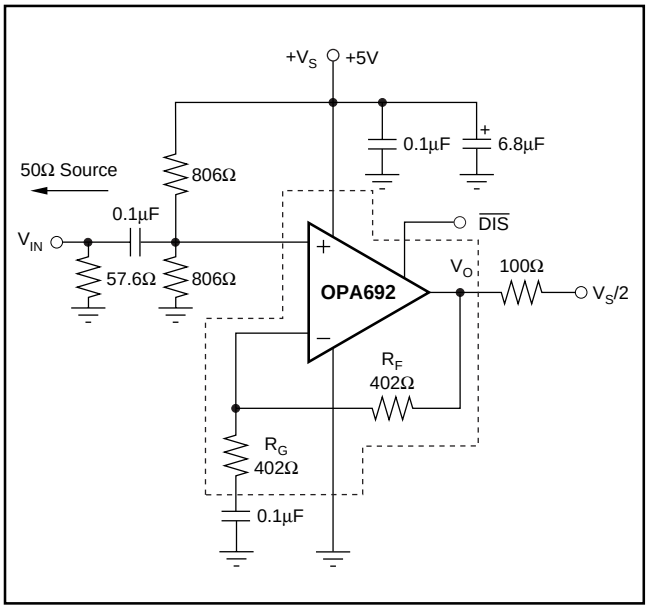


FIGURE 2. AC-Coupled, G = +2, Single-Supply Specification and Test Circuit.

SINGLE-SUPPLY ADC INTERFACE

Most modern, high-performance ADCs (such as the Texas Instruments ADS8xx and ADS9xx series) operate on a single +5V (or lower) power supply. It has been a considerable challenge for single-supply op amps to deliver a low-distortion input signal at the ADC input for signal frequencies

exceeding 5MHz. The high slew rate, exceptional output swing, and high linearity of the OPA692 make it an ideal single-supply ADC driver. Figure 3 shows an example input interface to a very high performance 10-bit, 60MSPS CMOS converter.

The OPA692 in the circuit of Figure 3 provides 190MHz bandwidth operating at a signal gain of +2 with a $2V_{PP}$ output swing. The noninverting input bias voltage is referenced to the midpoint of the ADC signal range by dividing off the top and bottom of the internal ADC reference ladder. With the gain resistor (R_G) AC-coupled, this bias voltage has a gain of +1 to the output, centering the output voltage swing as well. Tested performance at a 20MHz analog input frequency and a 60MSPS clock rate on the converter gives > 58dBc SFDR.

WIDEBAND VIDEO MULTIPLEXING

One common application for video speed amplifiers that include a disable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple wired-OR video multiplexer can be easily implemented using the OPA692, as shown in Figure 4.

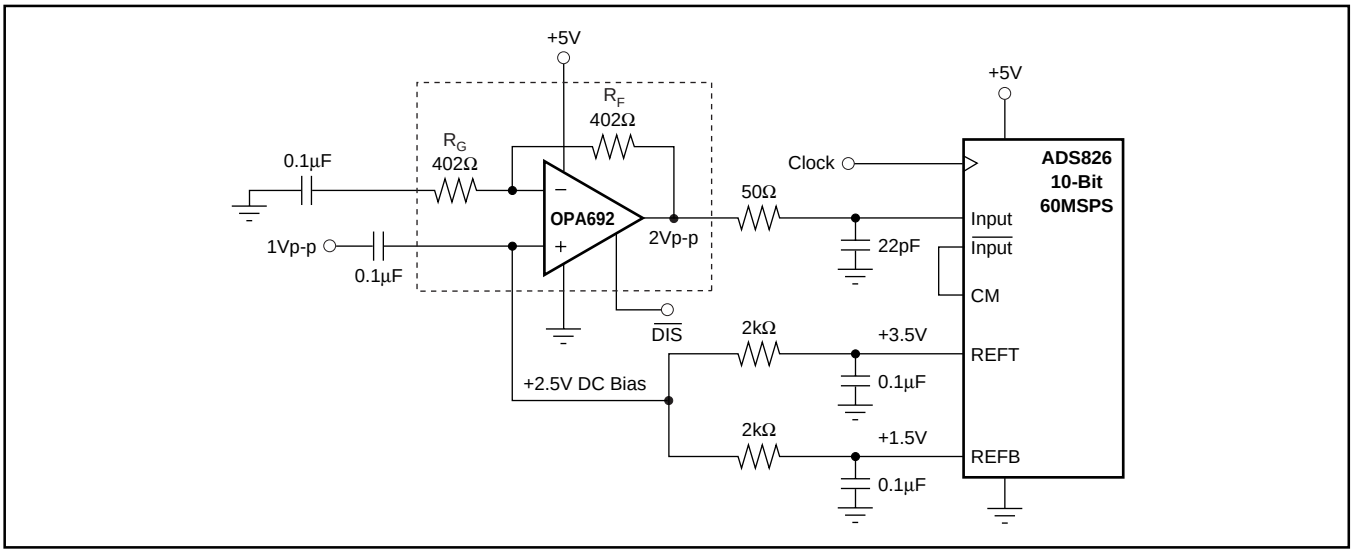


FIGURE 3. Wideband, AC-Coupled, Single-Supply ADC Driver.

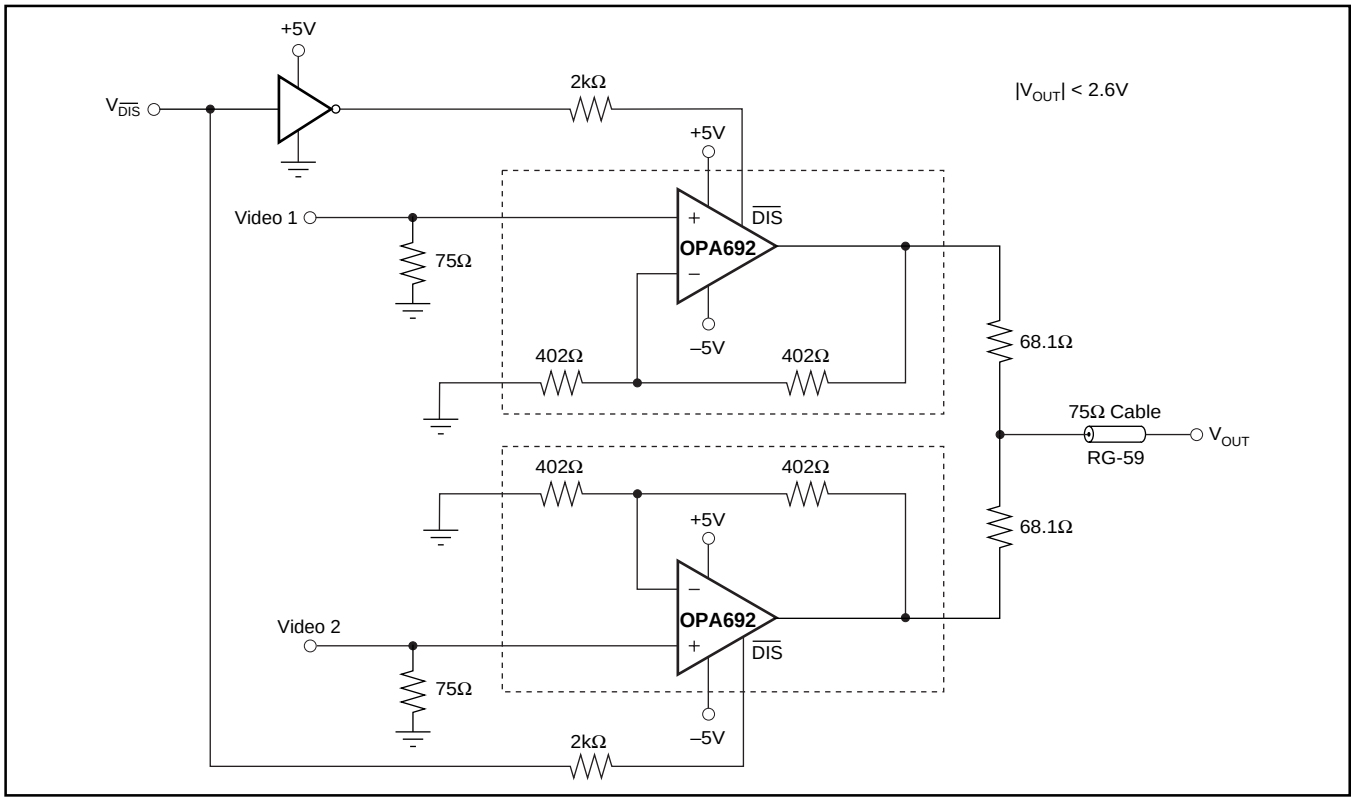


FIGURE 4. 2-Channel Video Multiplexer.

Typically, channel switching is performed either on sync or retrace time in the video signal. The two inputs are approximately equal at this time. The *make-before-break* disable characteristic of the OPA692 ensures that there is always one amplifier controlling the line when using a wired-OR circuit (see Figure 4). Since both inputs may be on for a short period during the transition between channels, the outputs are combined through the output impedance matching resistors (68.1Ω in this case). When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal in getting out onto the cable. The matching resistors have been set to get a signal gain of +1 at the load while providing > 20dB return loss at the load.

The video multiplexer connection (see Figure 4) also insures that the maximum differential voltage across the inputs of the unselected channel do not exceed the rated ±1.2V maximum for standard video signal levels. In any case, V_{OUT} *must* be < $\pm 2.6V_{PP}$ in order to not exceed the absolute maximum differential input voltage (±1.2V) on the disabled channel.

The Disable Operation section shows the turn-on and turn-off switching glitches using a grounded input for a single channel is typically less than ±50mV. Where two outputs are switched (see Figure 4), the output line is always under the control of one amplifier or the other due to the make-before-break disable timing. In this case, the switching glitches for two 0V inputs drops to < 20mV.

4-CHANNEL FREQUENCY CHANNELIZER

The circuit of Figure 5 is a 4-channel multiplexer. In this circuit the OPA691 provides the drive for all four channels. Each channel includes a bandpass filter and each bandpass filter is set for a different frequency band. This allows the channelizing part of this circuit. The role of the OPA692 is to provide impedance isolation. This is done through the use of four matching resistances (59Ω in this case). These matching resistors ensure that the signals will combine during the transition between channels. They have been used to get a gain of +1 at the load.

This circuit may be used with a different number of channels. Its limitation comes from the drive requirement for each channel, as well as the minimum acceptable return loss.

The output resistor value (R_O) to keep a gain of +1 at the load, depends on the number of channels. For the OPA692, Equation 1 gives:

(1)

$$R_O = \frac{\left[75\Omega \bullet (n-2) + 804\Omega\right]}{2} \bullet \left(\sqrt{1 + \frac{241200\Omega}{\left[75\Omega \bullet (n-2) + 804\Omega\right]^2}} - 1 \right)$$

Where n = number of devices in multiplexer.

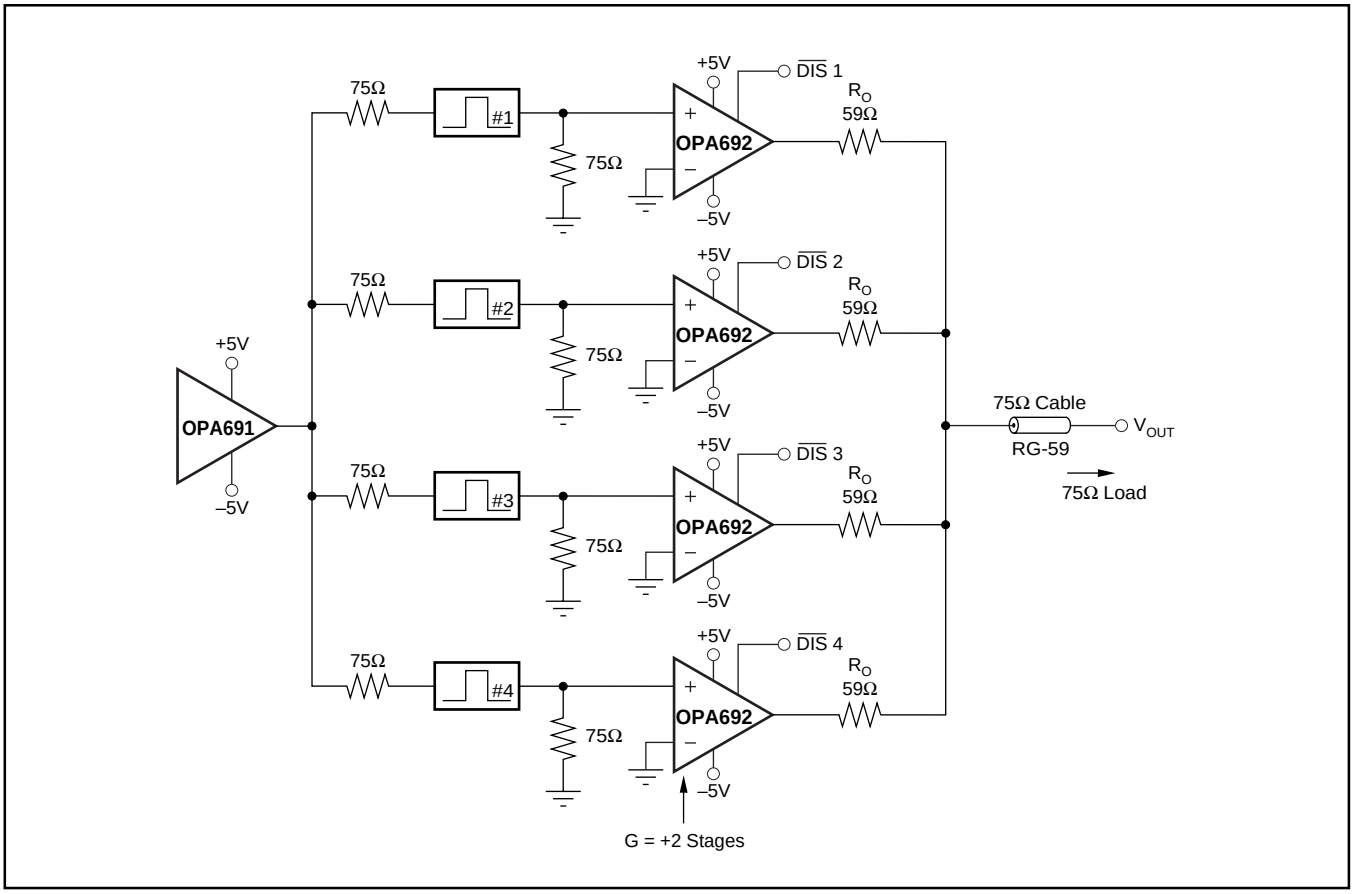


FIGURE 5. 4-Channel Frequency Channelizer.

DELAY-EQUALIZED LOW-PASS FILTER

The circuit in Figure 6 realizes a 5th-order Butterworth low-pass filter with a –3dB bandwidth of 20MHz and group delay equalization. This filter is based on the KRC active filter topology using amplifiers with a fixed positive gain ≥ 1.

The OPA692 makes a good amplifier for this type of filter. The first stage is the group delay equalizer, which is based on a gain of –1. The second stage has a high-Q pole, uses a gain of +2 for minimum component sensitivity, and also produces a real pole. The last stage has a low-Q pole, and uses a gain of +1 for minimum component sensitivity.

The component values have been predistorted to compensate for the op amps parasitic effects. The low-Q pole section was placed last to minimize noise peaking in the passband, while maintaining good dynamic range performance.

PRECISION VOLTAGE BUFFER

The precision buffer in Figure 7 combines the DC precision and low 1/f noise of the OPA227 with the high-speed performance of the OPA692. The 80.6kΩ resistor makes the high-frequency and low-frequency nominal gains equal. The OPA692 takes over from the OPA227 at approximately 32kHz.

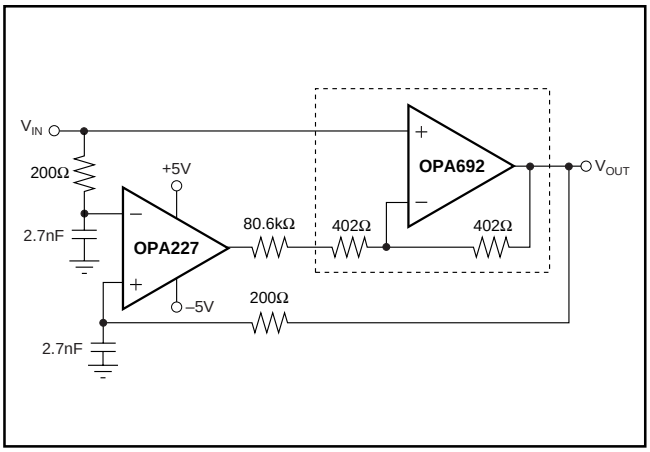


FIGURE 7. Precision Wideband, Unity-Gain Buffer.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA692 in its two package options. Both of these are offered free of

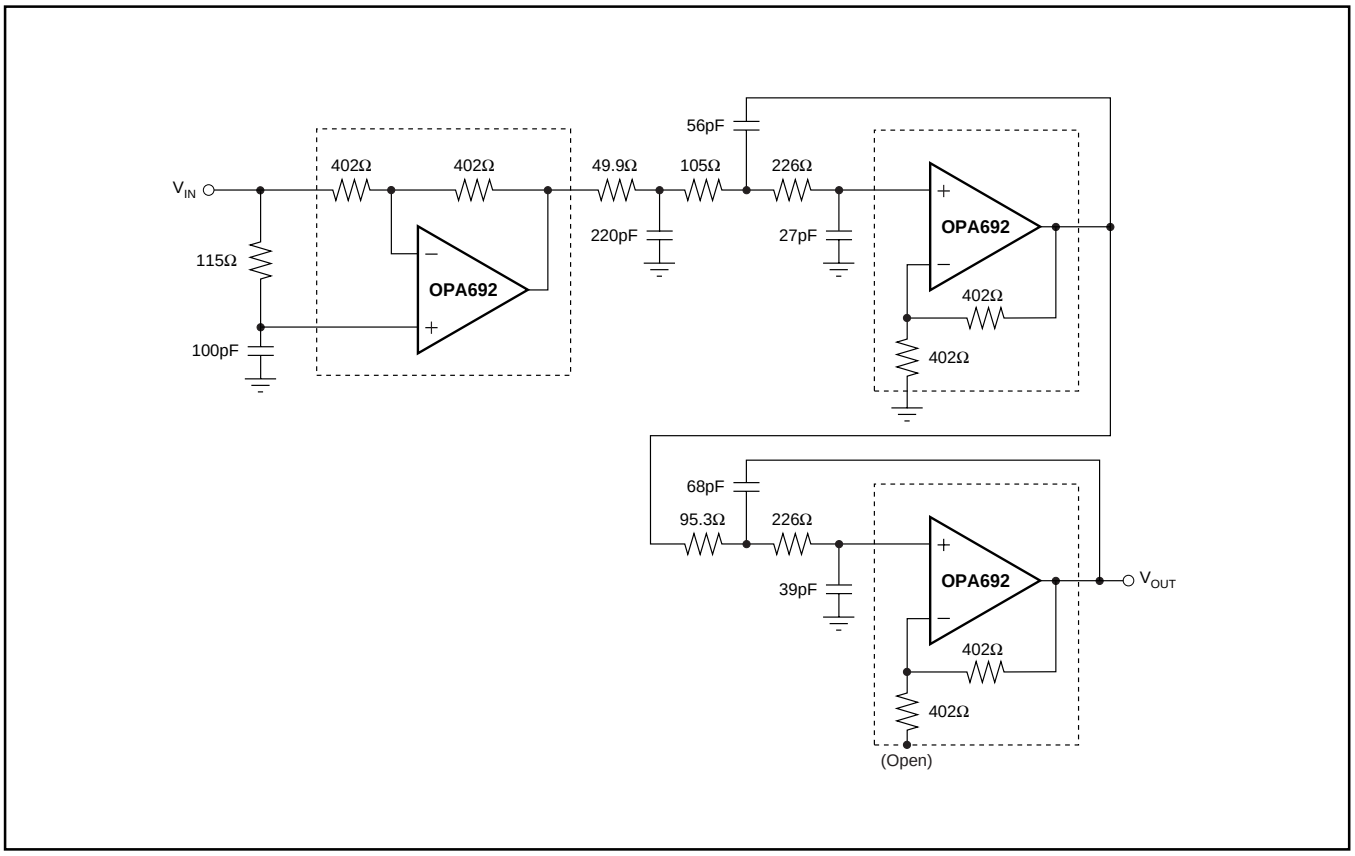


FIGURE 6. Butterworth LP Filter with Delay Equalization.

charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in the table below.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA692ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA692IDBV	SOT23-6	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA692 product folder.

OPERATING SUGGESTIONS

GAIN SETTING

Setting the gain with the OPA692 is very easy. For a gain of +2, ground the –IN pin and drive the +IN pin with the signal. For a gain of +1, leave the –IN pin open and drive the +IN pin with the signal. For a gain of –1, ground the +IN pin and drive the –IN pin with the signal. As the internal resistor values (not their ratio) change over temperature and process, external resistors should not be used to modify the gain.

OUTPUT CURRENT AND VOLTAGE

The OPA692 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1V to either supply rail; the tested swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is specified to deliver more than ±160mA.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current, or V-I product, which is more relevant to circuit operation. Refer to the “Output Voltage and Current Limitations” plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA692 output drive capabilities, noting that the graph is bounded by a safe operating area of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA692 can drive ±2.5V into 25Ω, or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability (see the Electrical Characteristics).

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristics. As the output transistors deliver power, their junction temperatures increase, decreasing their V_{BE}s (increasing the available output voltage swing), and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over-temperature specifications because the output stage junction temperatures are higher than the minimum specified operating ambient.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed amplifier like the OPA692 can be very susceptible to decreased stability and frequency response peaking when a capacitive load is placed directly on the output pin. When the amplifier’s open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended “R_S vs Capacitive Load” and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA692. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA692 output pin (see the Board Layout Guidelines section).

DISTORTION PERFORMANCE

The OPA692 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high-frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration, it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2x rate while the 3rd-harmonic increases at a much lower rate than the expected 3x. Where the test power doubles, the difference between it and the 2nd-harmonic decreases less than the

expected 6dB, while the difference between it and the 3rd decreases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (i.e., $2V_{PP}$ for each tone at the load, which requires $8V_{PP}$ for the overall 2-tone envelope at the output pin), the Typical Characteristics show 58dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

The OPA692 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (15pA/$\sqrt{\text{Hz}}$) is significantly lower than earlier solutions while the input voltage noise (1.7nV$\sqrt{\text{Hz}}$) is lower than most unity-gain stable, wideband, voltage-feedback op amps. This low input voltage noise was achieved at the price of higher noninverting input current noise (12pA/$\sqrt{\text{Hz}}$). As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise for the gain settings, available using the OPA692. Figure 8 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{\text{Hz}}$ or pA/$\sqrt{\text{Hz}}$.

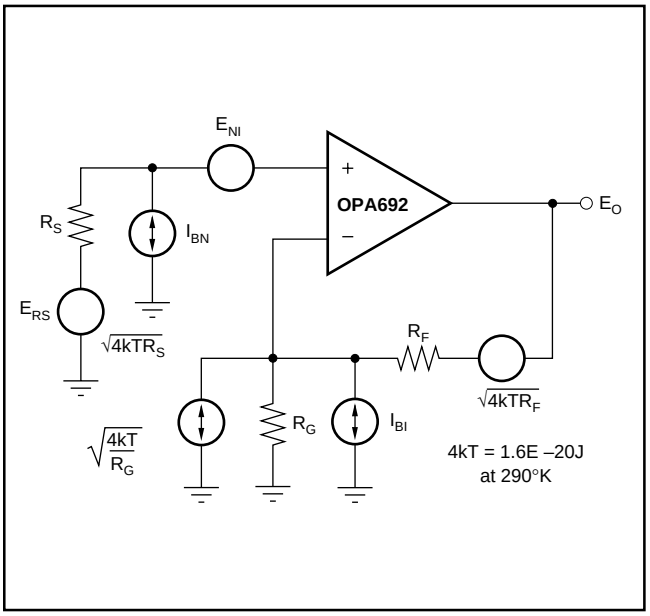


FIGURE 8. Noise Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 2 shows the general form for the output noise voltage using the terms shown in Figure 8.

(2)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 3.

(3)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA692 circuit and component values (see Figure 1) will give a total output spot noise voltage of 8.2nV/$\sqrt{\text{Hz}}$ and a total equivalent input spot noise voltage of 4.1nV/$\sqrt{\text{Hz}}$. This total input-referred spot noise voltage is higher than the 1.7nV/$\sqrt{\text{Hz}}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor.

DC ACCURACY

The OPA692 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Bias current cancellation techniques will not reduce the output DC offset for OPA692. As the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$\pm(NG \bullet V_{OS}(max)) + (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$$

where NG = noninverting signal gain

$$= \pm(2 \bullet 2.5mV) + (35\mu A \bullet 25\Omega \bullet 2) \pm (402\Omega \bullet 25\mu A)$$

$$= \pm 5mV + 1.75mV \pm 10.05mV$$

$$= -13.3mV \rightarrow +16.80mV$$

Minimizing the resistance seen by the noninverting input will give the best DC offset performance.

For significantly improved DC accuracy, consider the precision buffer circuit (see Figure 7).

DISABLE OPERATION

The OPA692 provides an optional disable feature that may be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{\text{DIS}}$ control pin is left

unconnected, the OPA692 will operate normally. To disable, the control pin must be asserted LOW. Figure 9 shows a simplified internal circuit for the disable control feature.

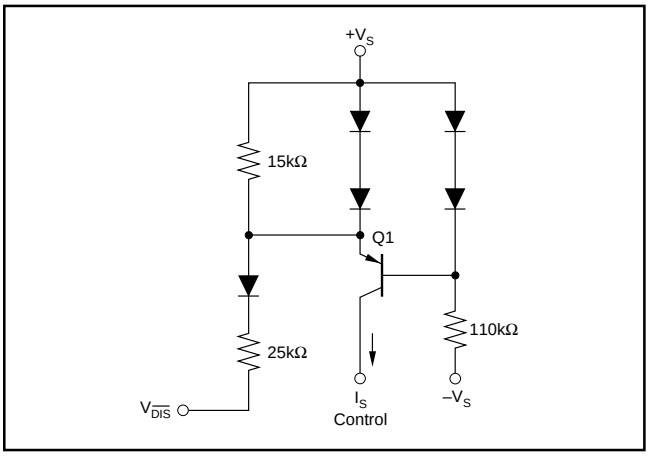


FIGURE 9. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 15kΩ resistor eventually turning on these two diodes (≈ 75μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode is only that required to operate the circuit of Figure 8. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high-impedance state. If the OPA692 is operating in a gain of +1, this will show a very high impedance (4pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain of +2, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured at a gain of –1, the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode. The Typical Characteristics show these glitches for the circuit of Figure 1 with the input signal set to 0V. The glitch waveform at the output pin is plotted along with the $\overline{DIS}$ pin voltage.

The transition edge rate (dV/dt) of the $\overline{DIS}$ control line will influence this glitch. Slowing this edge can be achieved by adding a simple RC filter into the $V_{\overline{DIS}}$ pin from a higher speed logic line. If extremely fast transition logic is used, a 2kΩ series resistor between the logic gate and the $\overline{DIS}$ input pin will provide adequate bandlimiting using just the parasitic input capacitance on the $\overline{DIS}$ pin while still ensuring an adequate logic level swing.

THERMAL ANALYSIS

Due to the high output power capability of the OPA692, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA692IDBV (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 20Ω load to $+2.5V_{DC}$:

$$P_D = 10V \bullet 5.8mA + 5^2/(4 \bullet (20\Omega \parallel 800\Omega)) = 378mW$$

$$\text{Maximum } T_J = +85°C + (0.39W \bullet 150°C/W) = 142°C$$

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower junction temperatures. Remember, this is a worst-case internal power dissipation—use your actual signal and load to compute P_{DL}. The highest possible internal dissipation occurs if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The "Output Voltage and Current Limitations" plot shown in the Typical Characteristics include a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA692 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output pin can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat further from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA692. Any external resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC-board trace length as short as possible. Never use wirewound type resistors in a high-frequency application. All external components should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended "R_S vs Capacitive Load." Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA692 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the "Distortion vs Load" plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA692 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA692 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of "R_S vs Capacitive Load." This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA692 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA692 onto the board.

INPUT AND ESD PROTECTION

The OPA692 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in

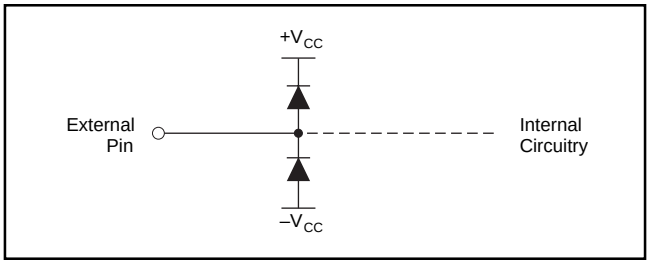


FIGURE 10. Internal ESD Protection.

Figure 10.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA692), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
12/08	E	2	Absolute Maximum Ratings	Changed minimum Storage Temperature Range from –40°C to –65°C.
3/06	D	16-17	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA692ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 692	Samples
OPA692IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAGI	Samples
OPA692IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAGI	Samples
OPA692IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAGI	Samples
OPA692IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 692	Samples
OPA692IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 692	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

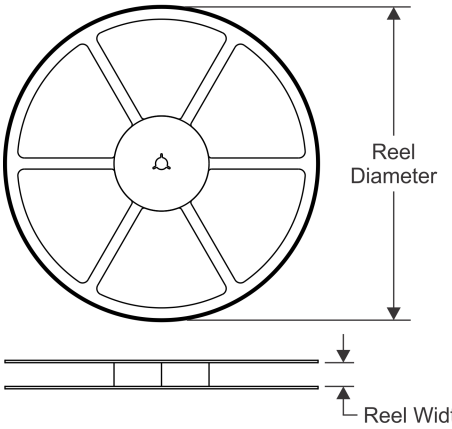
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

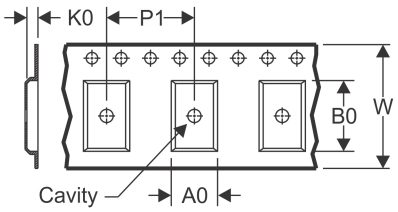
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

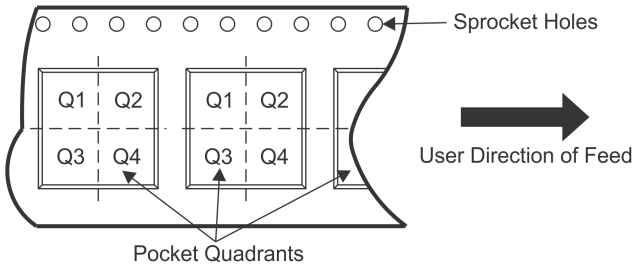


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

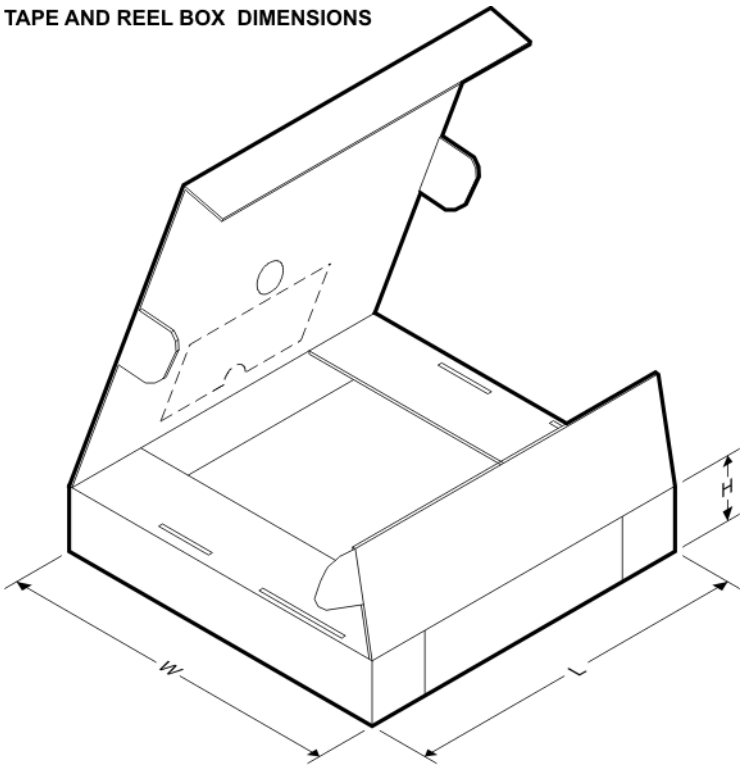
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA692IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

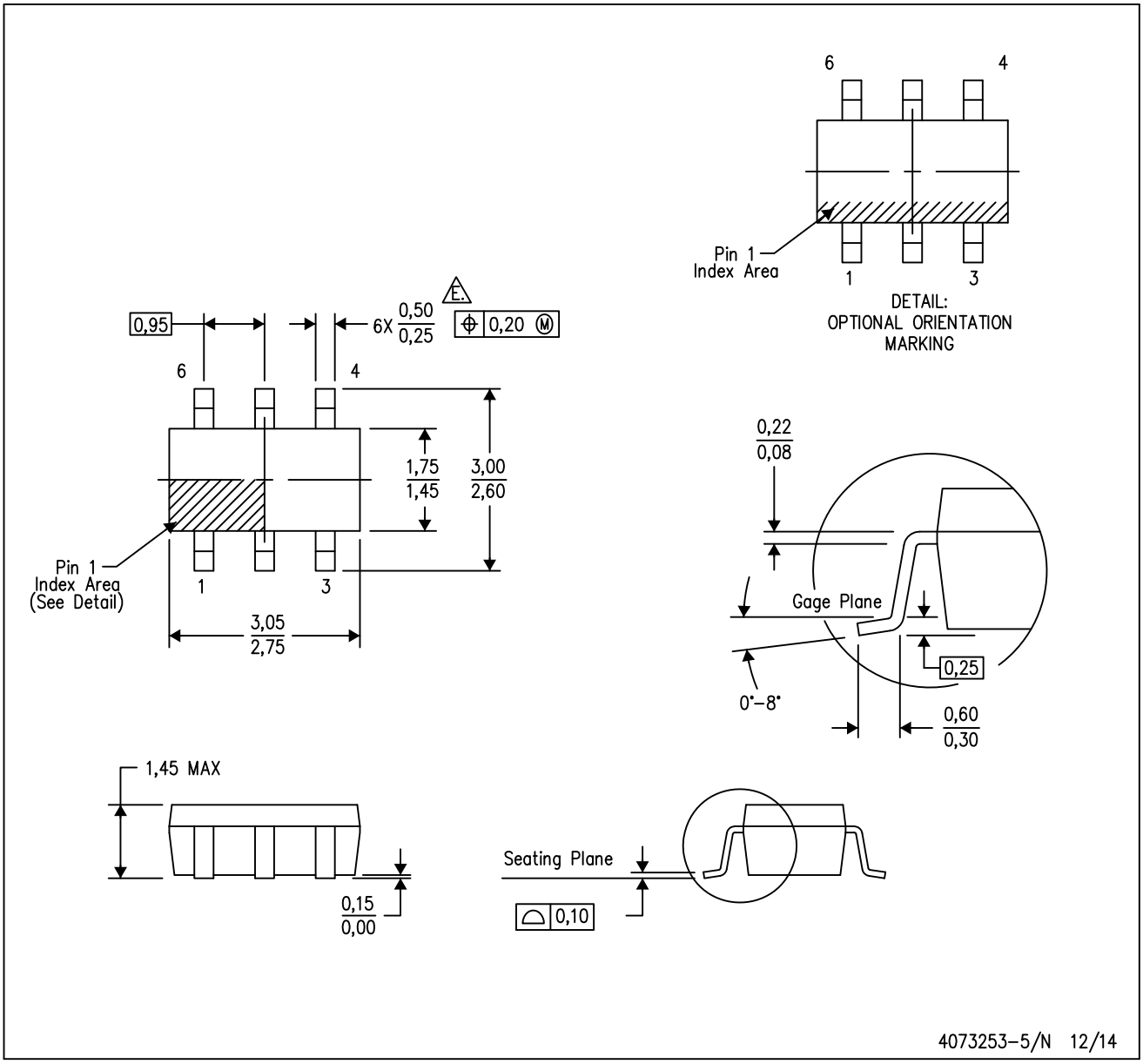
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

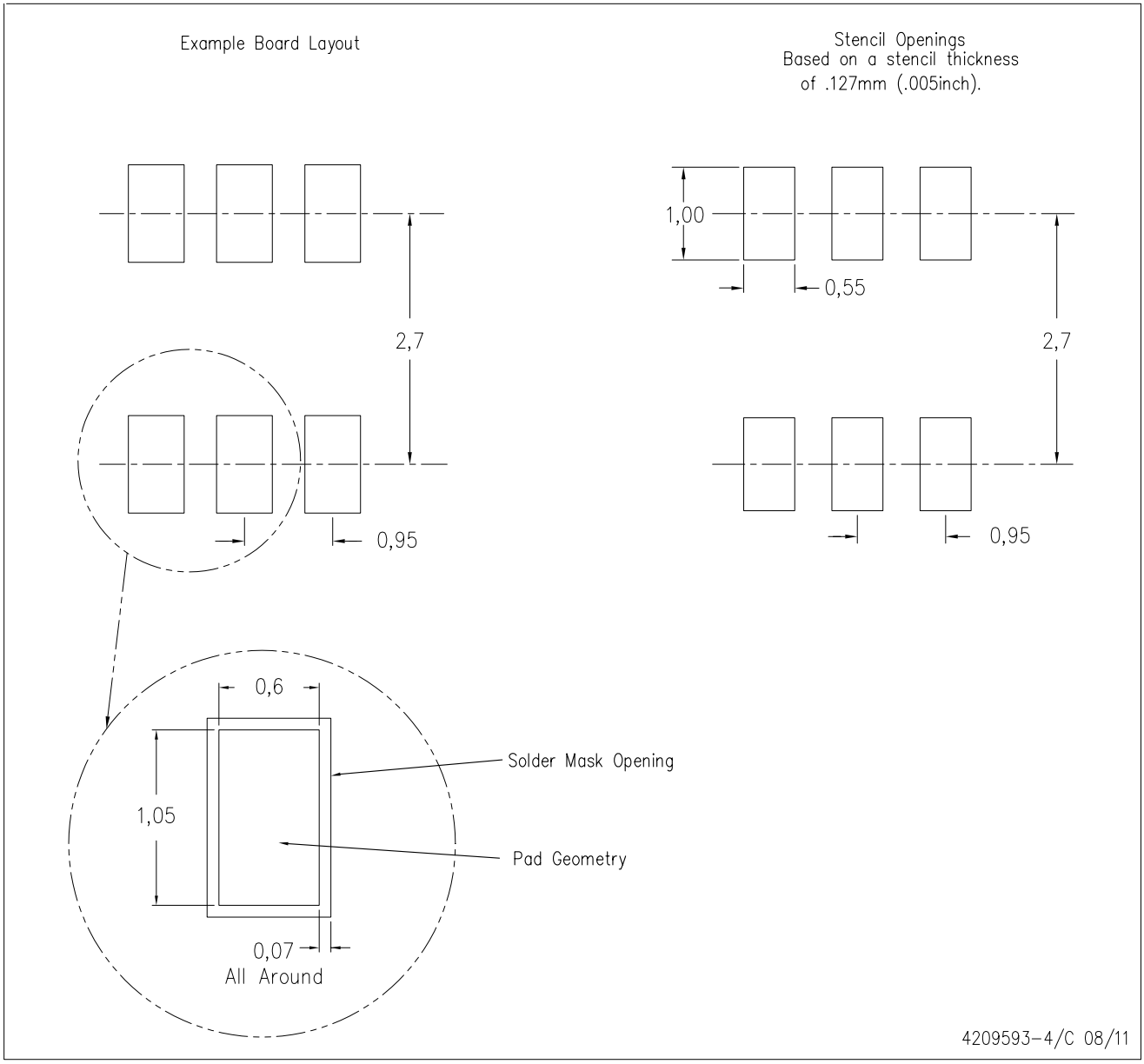
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA692IDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



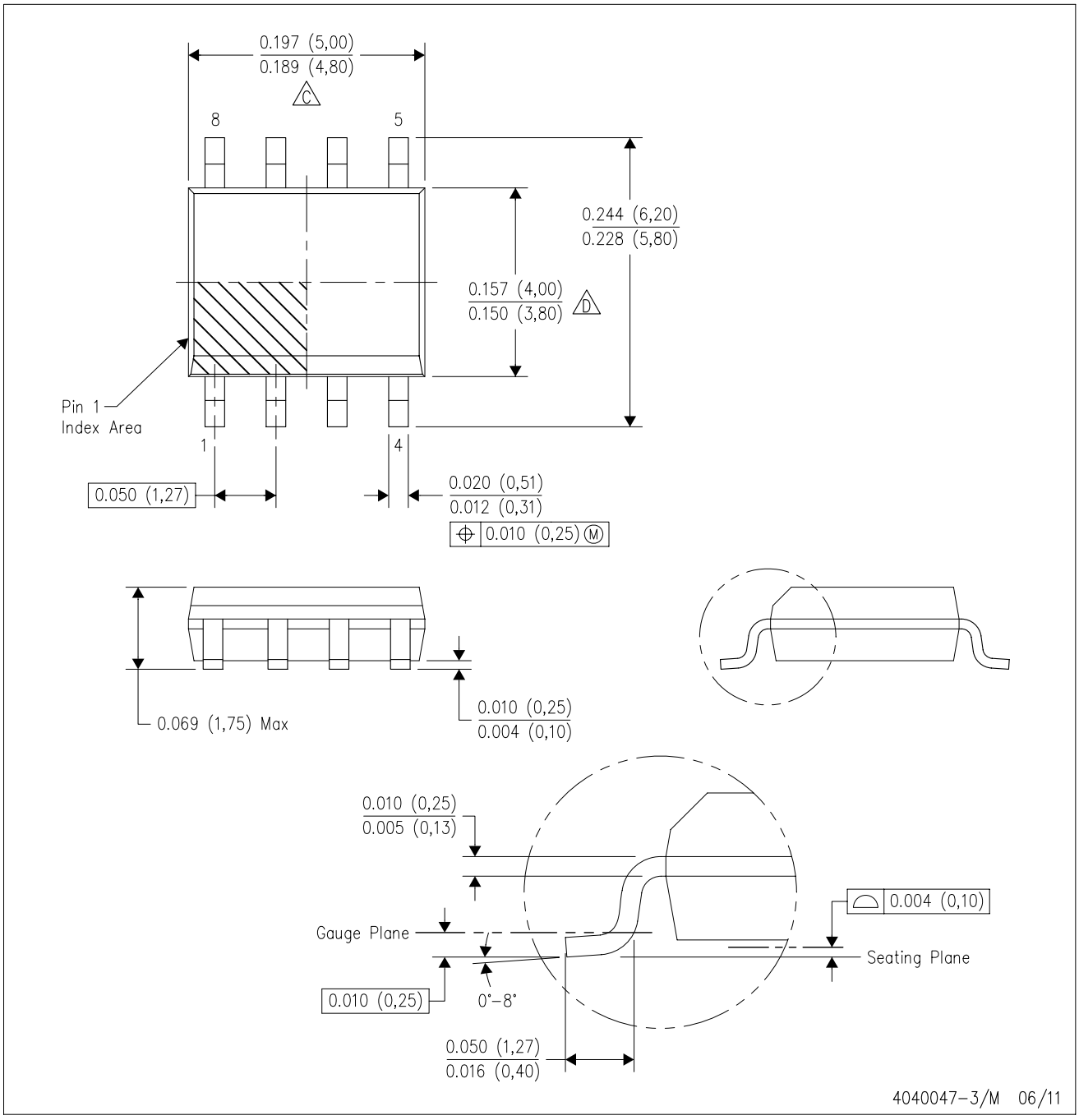
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



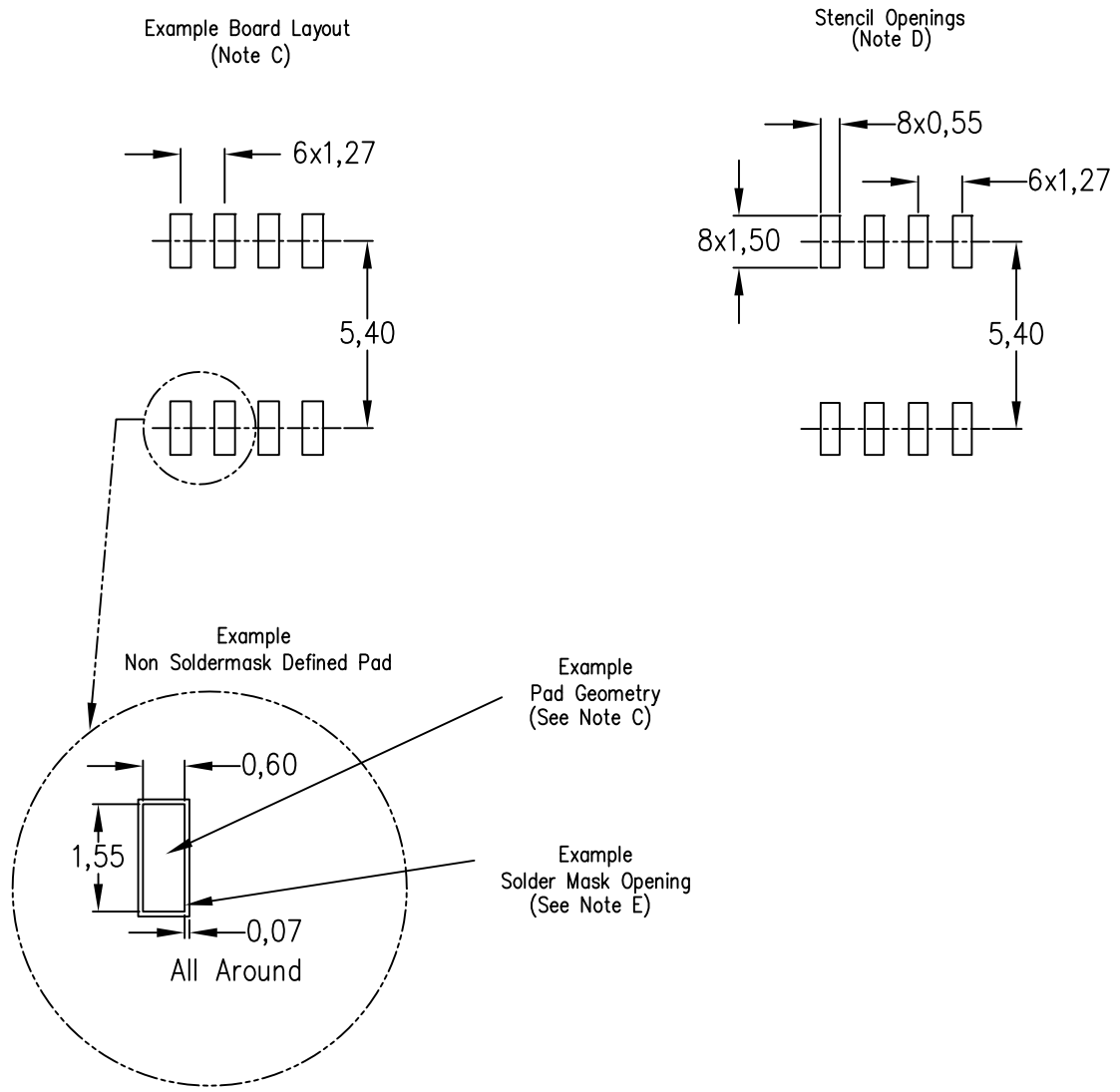
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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