



## 6 Mbps, Extended Common-Mode RS-485 Transceiver

Check for Samples: [SN65HVD21A](#)

### FEATURES

- **Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA-485 Requirement**
- **Reduced Unit-Load for up to 256 Nodes**
- **Bus I/O Protection to Over 16-kV HBM**
- **Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions**
- **Low Standby Supply Current 1- $\mu$ A Max**
- **More Than 100 mV Receiver Hysteresis**

### APPLICATIONS

- **Long Cable Solutions**
  - **Factory Automation**
  - **Security Networks**
  - **Building HVAC**
- **Severe Electrical Environments**
  - **Electrical Power Inverters**
  - **Industrial Drives**
  - **Avionics**

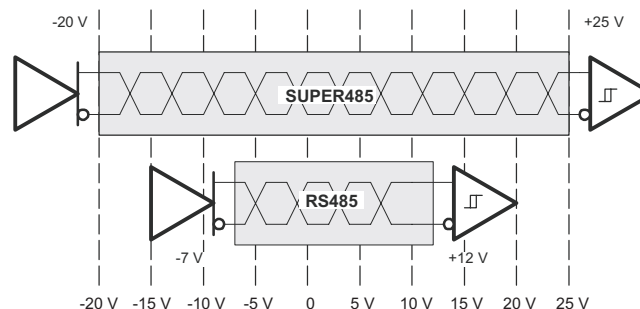
### DESCRIPTION

The SN65HVD21A offers performance far exceeding typical RS-485 devices. In addition to meeting all requirements of the TIA/EIA-485-A standard, the device operates over an extended range of common-mode voltage, and has features such as high ESD protection, wide receiver hysteresis, and failsafe operation. This device is ideally suited for long-cable networks, and other applications where the environment is too harsh for ordinary transceivers.

The device is designed for bidirectional data transmission on multipoint twisted-pair cables. Example applications are digital motor controllers, remote sensors and terminals, industrial process control, security stations, and environmental control systems.

The device combines a 3-state differential driver and a differential receiver, which operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a differential bus port that offers minimum loading to the bus. This port features an extended common-mode voltage range making the device suitable for multipoint applications over long cable runs.

### Device Operates Over a Wider Common-Mode Voltage Range



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

The SN65HVD21A allows up to 256 connected nodes at moderate data rates (up to 6 Mbps). The driver output slew rate is controlled to provide reliable switching with shaped transitions which reduce high-frequency noise emissions.

The receivers also include a failsafe circuit that provides a high-level output within 250 microseconds after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or the absence of any active transmitters on the bus. This feature prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling.

The SN65HVD21A is characterized for operation over the temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## PRODUCT SELECTION GUIDE

PART NUMBERS	CABLE LENGTH AND SIGNALING RATE <sup>(1)</sup>	NODES	MARKING
SN65HVD21A	Up to 150 m at 5 Mbps (with slew rate limit)	Up to 256	D: VP21A

(1) Distance and signaling rate predictions based upon Belden 3105A cable and 15% eye pattern jitter.

### AVAILABLE OPTIONS

<b>PLASTIC SMALL-OUTLINE<sup>(1)</sup></b> <b>D-PACKAGE</b> <b>(JEDEC MS-012)</b> SN65HVD21AD
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(1) Add R suffix for taped and reeled carriers.

**Table 1. DRIVER FUNCTION TABLE**

INPUT D	ENABLE	OUTPUTS	
	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	H	L

H = high level, L = low level, X = don't care, Z = high impedance (off), ? = indeterminate

**Table 2. RECEIVER FUNCTION TABLE**

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE RE	OUTPUT R
$0.2\text{ V} \leq V_{ID}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	H (see Note <sup>(1)</sup> )
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
X	OPEN	Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

H = high level, L = low level, Z = high impedance (off)

(1) If the differential input  $V_{ID}$  remains within the transition range for more than 250  $\mu\text{s}$ , the integrated failsafe circuitry detects a bus fault, and set the receiver output to a high state. See [Figure 15](#).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			<b>SN65HVD2X</b>
Supply voltage <sup>(2)</sup> , $V_{CC}$			–0.5 V to 7 V
Voltage at any bus I/O terminal			–27 V to 27 V
Voltage input, transient pulse, A and B, (through 100 $\Omega$ , see Figure 16)			–60 V to 60 V
Voltage input at any D, DE or $\overline{RE}$ terminal			–0.5 V to $V_{CC} + 0.5$ V
Receiver output current, $I_O$			–10 mA to 10 mA
Electrostatic discharge	Human Body Model <sup>(3)</sup>	A, B, GND	16 kV
		All pins	5 kV
	Charged-Device Model <sup>(4)</sup>	All pins	1.5 kV
		Machine Model <sup>(5)</sup>	All pins
Continuous total power dissipation			See Thermal Table
Junction temperature, $T_J$			150°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.
- (5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

## RECOMMENDED OPERATING CONDITIONS

		<b>MIN</b>	<b>NOM</b>	<b>MAX</b>	<b>UNIT</b>
Supply voltage, $V_{CC}$		4.5	5	5.5	V
Voltage at any bus I/O terminal	A, B	–20		25	V
High-level input voltage, $V_{IH}$	D, DE, $\overline{RE}$	2		$V_{CC}$	V
Low-level input voltage, $V_{IL}$		0		0.8	
Differential input voltage, $V_{ID}$	A with respect to B	–25		25	V
Output current	Driver	–110		110	mA
	Receiver	–8		8	
Operating free-air temperature, $T_A$ <sup>(1)</sup>		–40		85	°C
Junction temperature, $T_J$		–40		130	°C

- (1) Maximum free-air temperature operation is allowed as long as the device recommended junction temperature is not exceeded.

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## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18$ mA	-1.5	0.75		V
$V_O$	Open-circuit output voltage	A or B, No load	0		$V_{CC}$	V
$ V_{OD(SS)} $	Steady-state differential output voltage	No load (open circuit)	3.3	4.2	$V_{CC}$	V
		$R_L = 54 \Omega$ , See <a href="#">Figure 1</a>	1.8	2.5		
		With common-mode loading, See <a href="#">Figure 2</a>	1.8			
$\Delta V_{OD(SS)} $	Change in steady-state differential output voltage between logic states	See <a href="#">Figure 1</a> and <a href="#">Figure 3</a>	-0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See <a href="#">Figure 1</a>	2.1	2.5	2.9	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage, $V_{OC(H)} - V_{OC(L)}$	See <a href="#">Figure 1</a> and <a href="#">Figure 4</a>	-0.1		0.1	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage, $V_{OC(MAX)} - V_{OC(MIN)}$	$R_L = 54 \Omega$ , $C_L = 50$ pF, See <a href="#">Figure 1</a> and <a href="#">Figure 4</a>	0.35			V
$V_{OD(RING)}$	Differential output voltage over and under shoot	$R_L = 54 \Omega$ , $C_L = 50$ pF, See <a href="#">Figure 5</a>			10%	
$I_I$	Input current	D, DE	-100		100	$\mu$ A
$I_O$	Output current with power off. High impedance state output current.	$V_O < -7$ V to 12 V, Other input = 0 V	-100		125	$\mu$ A
		$V_O < -20$ V to 25 V, Other input = 0 V	-200		250	
$I_{OS}$	Short-circuit output current	$V_O = -20$ V to 25 V, See <a href="#">Figure 9</a>	-250		250	mA
$C_{OD}$	Differential output capacitance				20	pF

(1) All typical values are at  $V_{CC} = 5$  V and 25°C.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Differential output propagation delay, low-to-high	$R_L = 54 \Omega$ , $C_L = 50$ pF, See <a href="#">Figure 3</a>	20	32	60	ns
$t_{PHL}$	Differential output propagation delay, high-to-low					
$t_r$	Differential output rise time	$R_L = 54 \Omega$ , $C_L = 50$ pF, See <a href="#">Figure 3</a>	20	40	50	ns
$t_f$	Differential output fall time					
$t_{pZH}$	Propagation delay time, high-impedance-to-high-level output	$\overline{RE}$ at 0 V, See <a href="#">Figure 6</a>			100	ns
$t_{pHZ}$	Propagation delay time, high-level output-to-high-impedance					
$t_{pZL}$	Propagation delay time, high-impedance-to-high-level output	$\overline{RE}$ at 0 V, See <a href="#">Figure 7</a>			100	ns
$t_{pLZ}$	Propagation delay time, high-level output-to-high-impedance					
$t_{d(standby)}$	Time from an active differential output to standby	$\overline{RE}$ at $V_{CC}$ , See <a href="#">Figure 8</a>			2	$\mu$ s
$t_{d(wake)}$	Wake-up time from standby to an active differential output				8	$\mu$ s
$t_{sk(p)}$	Pulse skew $ t_{PLH} - t_{PHL} $				6	ns

(1) All typical values are at  $V_{CC} = 5$  V and 25°C

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IT(+)}$	Positive-going differential input voltage threshold	See Figure 10 $V_O = 2.4\text{ V}$ , $I_O = -8\text{ mA}$		60	200	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		$V_O = 0.4\text{ V}$ , $I_O = 8\text{ mA}$	-200	-60	
$V_{HYS}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )		100	130		mV
$V_{IT(F+)}$	Positive-going differential input failsafe voltage threshold	See Figure 15 VCM = -7 V to 12 V VCM = -20 V to 25 V	40	120	200	mV
$V_{IT(F-)}$	Negative-going differential input failsafe voltage threshold		VCM = -7 V to 12 V VCM = -20 V to 25 V	-200	-120	
$V_{IK}$	Input clamp voltage	$I_I = -18\text{ mA}$	-1.5			V
$V_{OH}$	High-level output voltage	$V_{ID} = 200\text{ mV}$ , $I_{OH} = -8\text{ mA}$ , See Figure 11	4			V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200\text{ mV}$ , $I_{OL} = 8\text{ mA}$ , See Figure 11			0.4	V
$I_{I(BUS)}$	Bus input current (power on or power off)	$V_I = -7\text{ to }12\text{ V}$ , Other input = 0 V	-100		125	$\mu\text{A}$
		$V_I = -20\text{ to }25\text{ V}$ , Other input = 0 V	-200		250	
$I_I$	Input current	RE	-100		100	$\mu\text{A}$
$R_I$	Input resistance		96			k $\Omega$
$C_{ID}$	Differential input capacitance	$V_{ID} = 0.5 + 0.4\text{ sine}(2\pi \times 1.5 \times 10^6 t)$		20		pF

(1) All typical values are at 25°C.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high level output	See Figure 11		25	50	ns
$t_{PHL}$	Propagation delay time high-to low level output					
$t_r$	Receiver output rise time	See Figure 11		2	4	ns
$t_f$	Receiver output fall time					
$t_{PZH}$	Receiver output enable time to high level	See Figure 12		90	120	ns
$t_{PHZ}$	Receiver output disable time from high level			16	35	
$t_{PZL}$	Receiver output enable time to low level	See Figure 13		90	120	ns
$t_{PLZ}$	Receiver output disable time from low level			16	35	
$t_{r(\text{standby})}$	Time from an active receiver output to standby	See Figure 14, DE at 0 V		2		$\mu\text{s}$
$t_{r(\text{wake})}$	Wake-up time from standby to an active receiver output			8		
$t_{sk(p)}$	Pulse skew [ $t_{PLH} - t_{PHL}$ ]				5	
$t_{p(\text{set})}$	Delay time, bus fail to failsafe set	See Figure 15, pulse rate = 1 kHz		250	350	$\mu\text{s}$
$t_{p(\text{reset})}$	Delay time, bus recovery to failsafe reset			50		

## SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

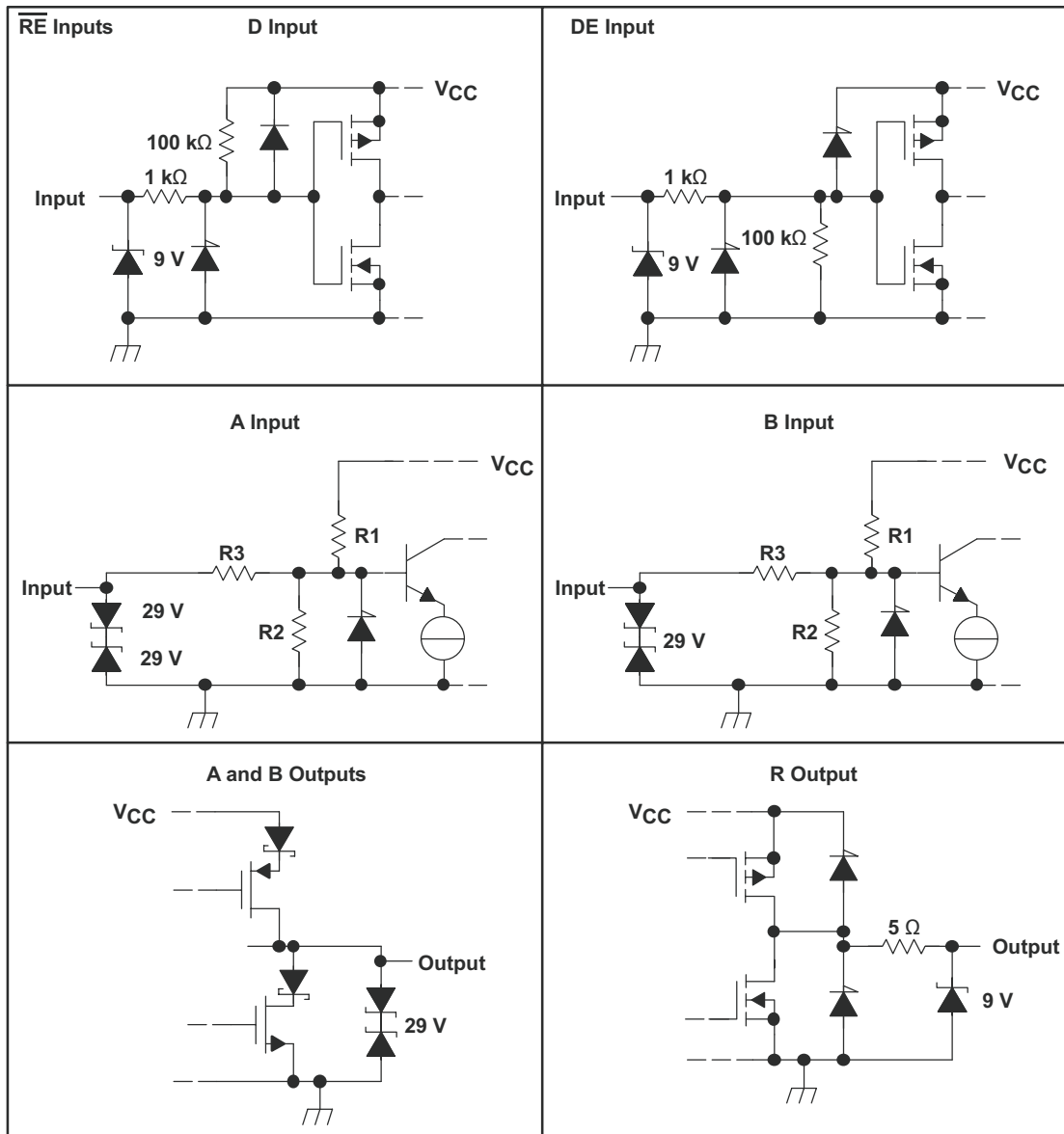
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}$	Supply current	Driver enabled (DE at $V_{CC}$ ), Receiver enabled (RE at 0 V), No load, $V_I = 0\text{ V}$ or $V_{CC}$		8	12	mA
		Driver enabled (DE at $V_{CC}$ ), Receiver disabled (RE at $V_{CC}$ ), No load, $V_I = 0\text{ V}$ or $V_{CC}$		7	11	mA
		Driver disabled (DE at 0 V), Receiver enabled (RE at 0 V), No load		5	8	mA
		Driver disabled (DE at 0 V), Receiver disabled (RE at $V_{CC}$ ) D open			1	$\mu\text{A}$

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## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



R1/R2	R3
36 kΩ	180 kΩ

PARAMETER MEASUREMENT INFORMATION

**NOTE:** Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle,  $Z_o = 50 \Omega$  (unless otherwise specified).

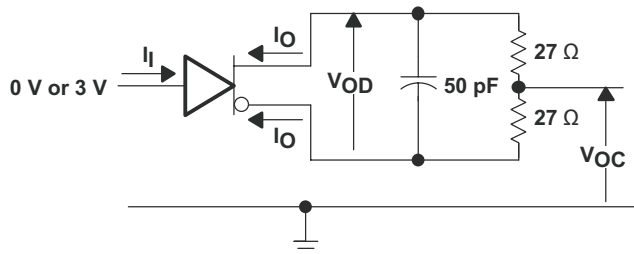


Figure 1. Driver Test Circuit,  $V_{OD}$  and  $V_{OC}$  Without Common-Mode Loading

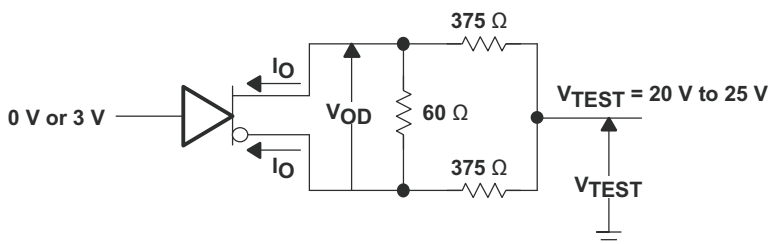


Figure 2. Driver Test Circuit,  $V_{OD}$  With Common-Mode Loading

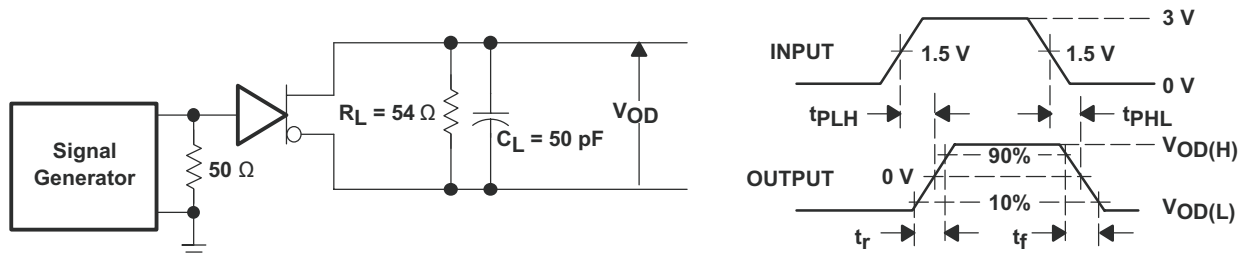


Figure 3. Driver Switching Test Circuit and Waveforms

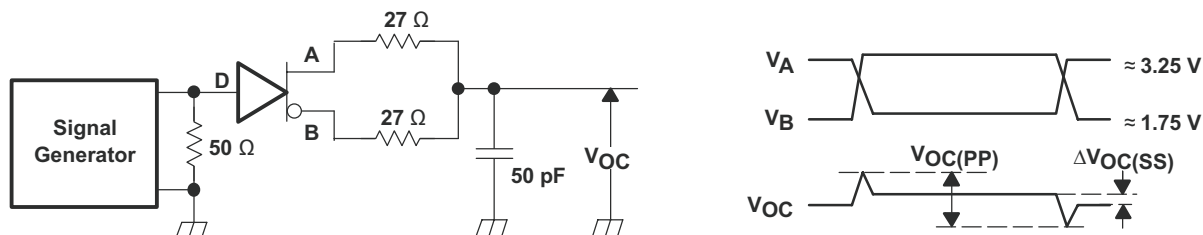
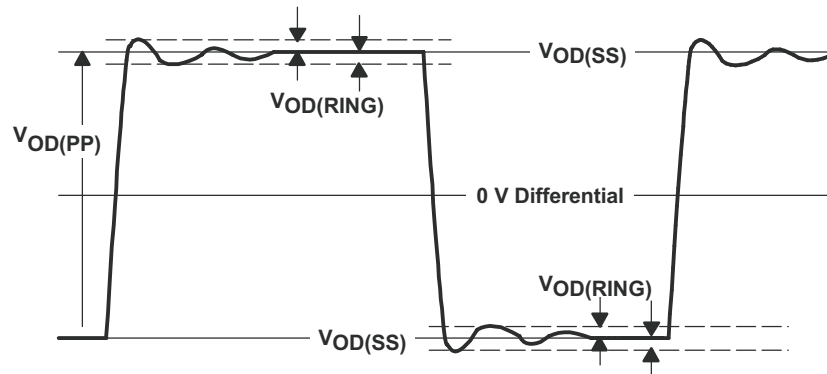


Figure 4. Driver  $V_{OC}$  Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE:  $V_{OD(RING)}$  is measured at four points on the output waveform, corresponding to overshoot and undershoot from the  $V_{OD(H)}$  and  $V_{OD(L)}$  steady state values.

Figure 5.  $V_{OD(RING)}$  Waveform and Definitions

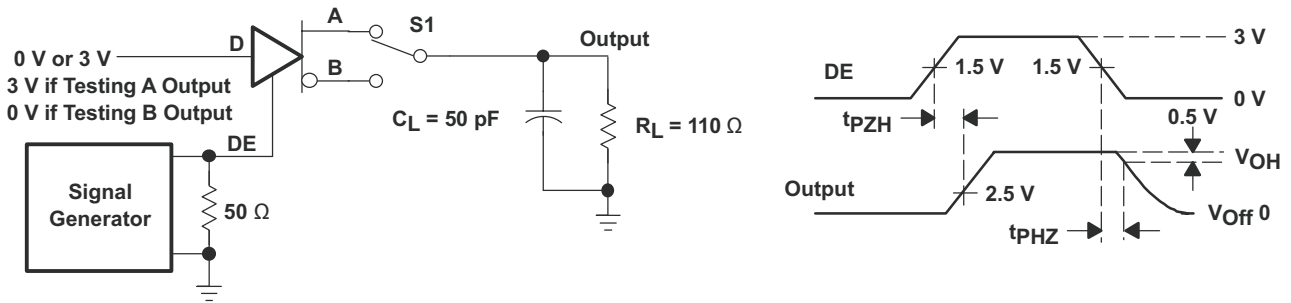


Figure 6. Driver Enable/Disable Test, High Output

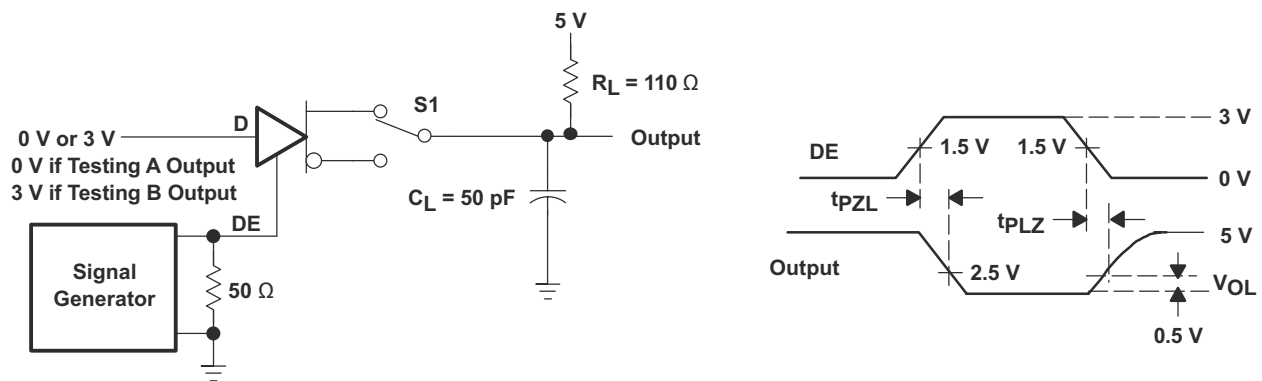


Figure 7. Driver Enable/Disable Test, Low Output



PARAMETER MEASUREMENT INFORMATION (continued)

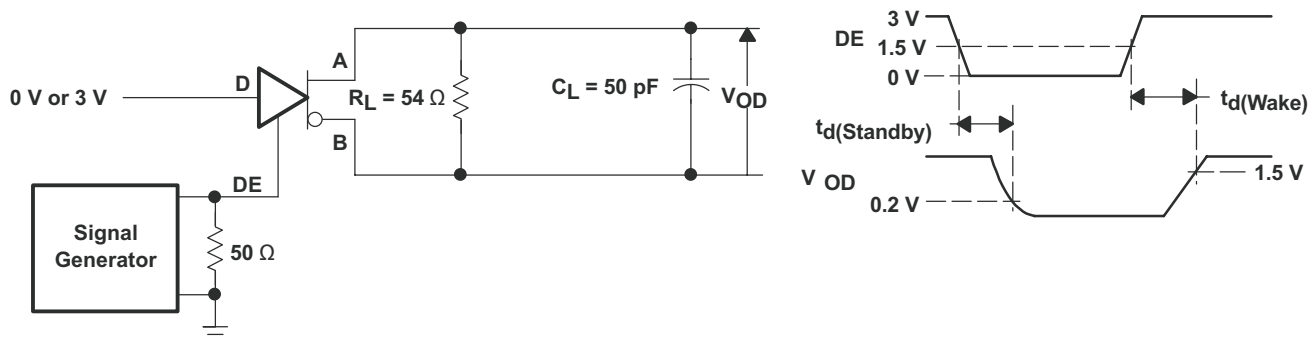


Figure 8. Driver Standby/Wake Test Circuit and Waveforms

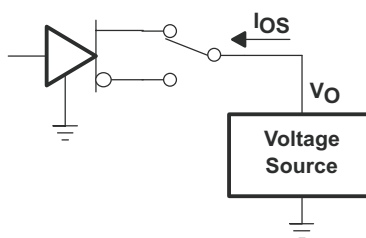


Figure 9. Driver Short-Circuit Test

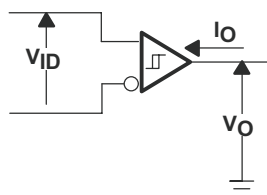


Figure 10. Receiver DC Parameter Definitions

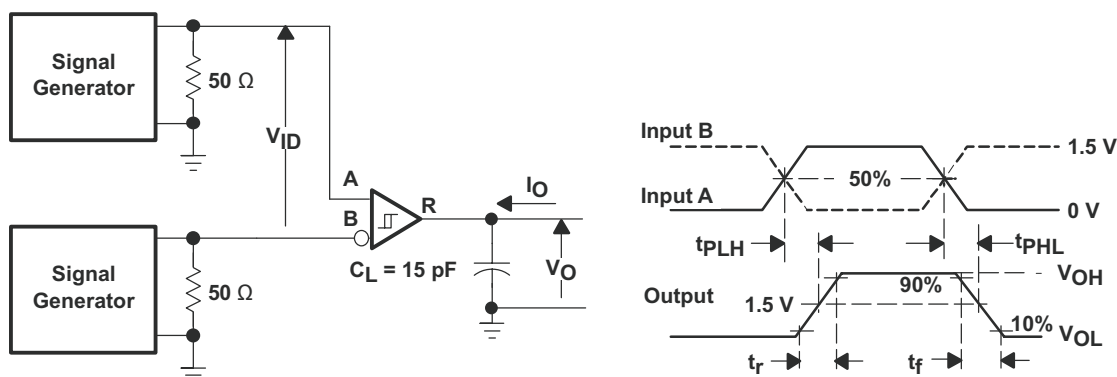
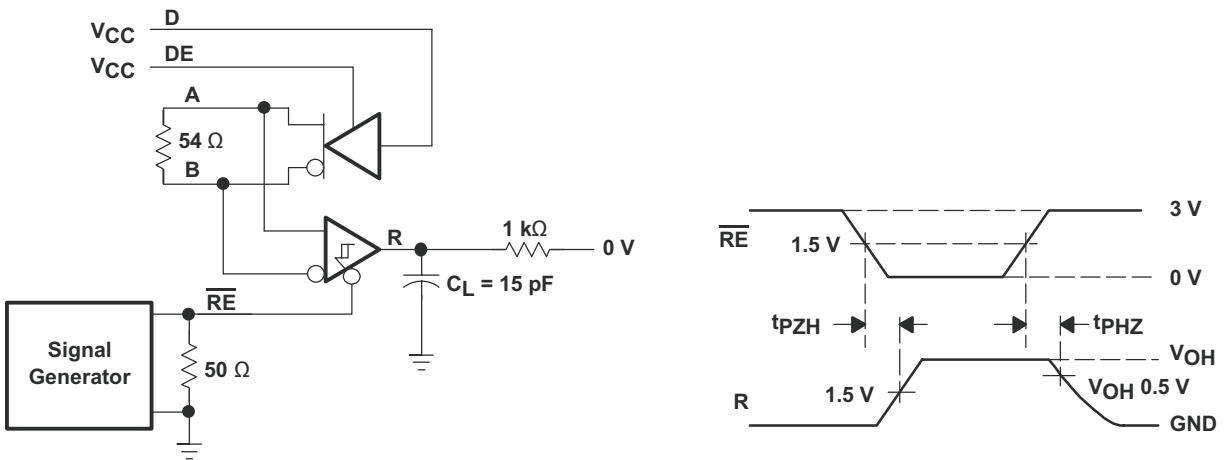
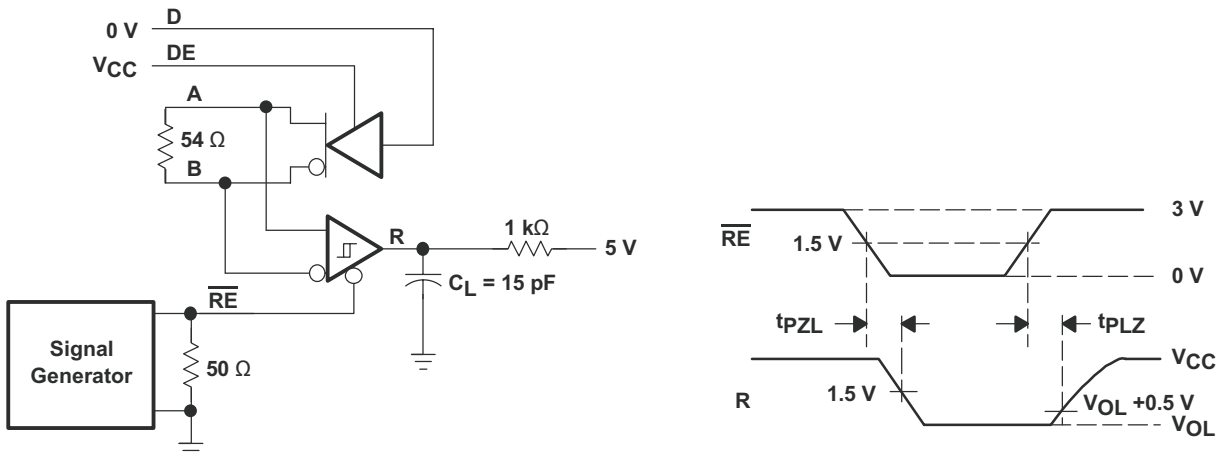
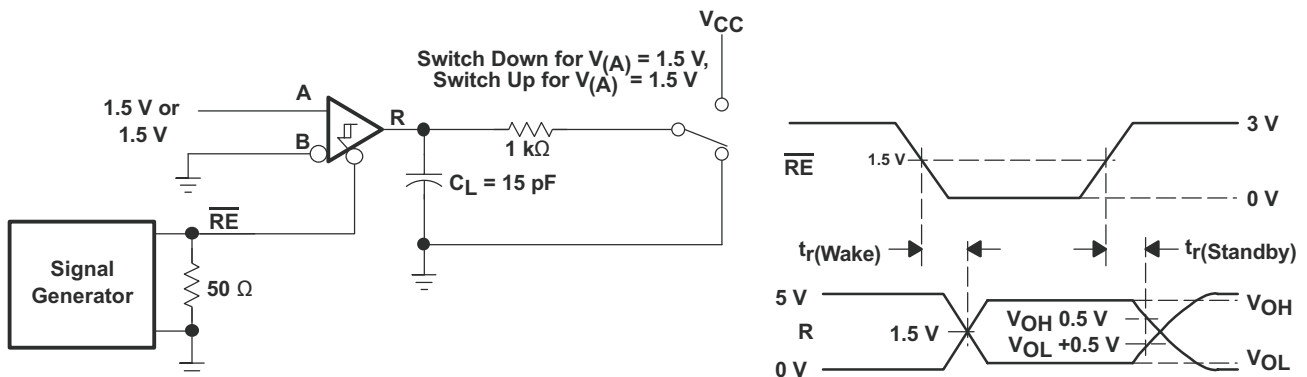


Figure 11. Receiver Switching Test Circuit and Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)**

**Figure 12. Receiver Enable Test Circuit and Waveforms, Data Output High**

**Figure 13. Receiver Enable Test Circuit and Waveforms, Data Output Low**

**Figure 14. Receiver Standby and Wake Test Circuit and Waveforms**

PARAMETER MEASUREMENT INFORMATION (continued)

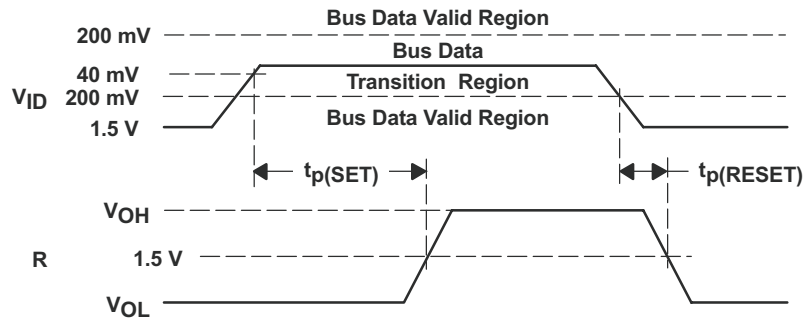


Figure 15. Receiver Active Failsafe Definitions and Waveforms

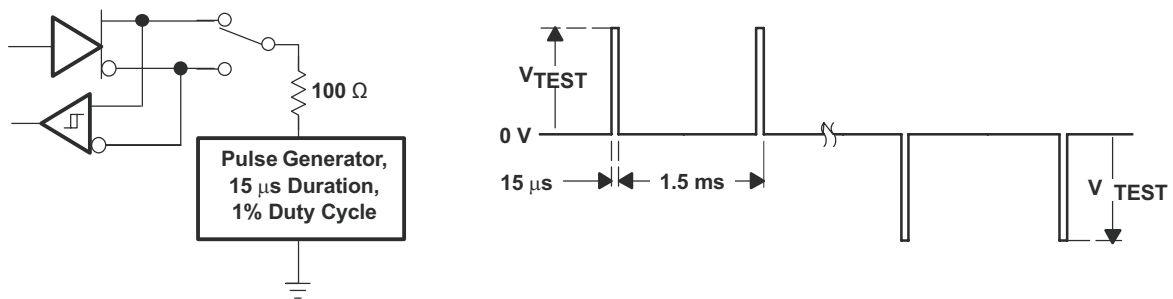
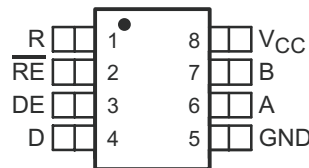
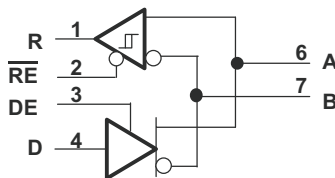


Figure 16. Test Circuit and Waveforms, Transient Overvoltage Test

D PACKAGE (TOP VIEW)



LOGIC DIAGRAM



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## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		SN65HVD21A	UNITS
		SOIC (D)	
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	78.1	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance	56.5	
$\theta_{JB}$	Junction-to-board thermal resistance	50.44	
$\psi_{JT}$	Junction-to-top characterization parameter	4.1	
$\psi_{JB}$	Junction-to-board characterization parameter	32.6	
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## POWER DISSIPATION

PARAMETERS		TEST CONDITIONS		VALUE	UNIT
Device Power dissipation, $P_D$	Typical	$V_{CC} = 5\text{ V}$ , $T_J = 25^\circ\text{C}$ , $R_L = 54\ \Omega$ , $C_L = 50\ \text{pF}$ (driver), $C_L = 15\ \text{pF}$ (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	5 Mbps	260	mW
	Worst case	$V_{CC} = 5.5\ \text{V}$ , $T_J = 125^\circ\text{C}$ , $R_L = 54\ \Omega$ , $C_L = 50\ \text{pF}$ , $C_L = 15\ \text{pF}$ (receiver), 50% Duty cycle square-wave signal, Driver and receiver enabled	5 Mbps	342	mW
Thermal shut down junction temperature, $T_{SD}$				170	°C

TYPICAL CHARACTERISTICS

BUS PIN CURRENT  
vs  
BUS PIN VOLTAGE

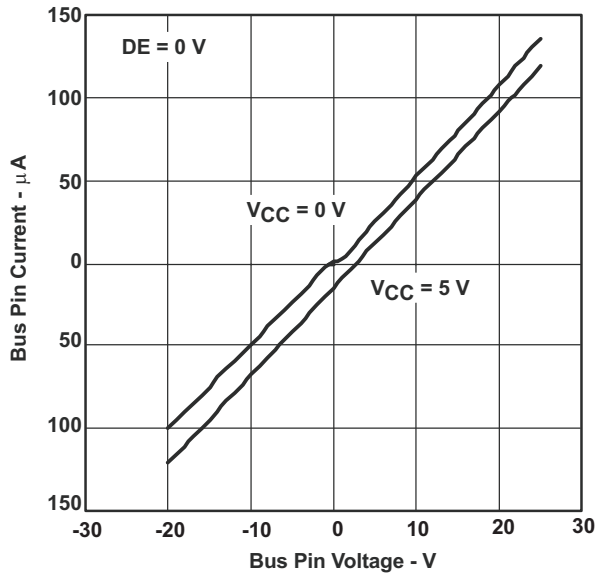


Figure 17.

SUPPLY CURRENT  
vs  
SIGNALLING RATE

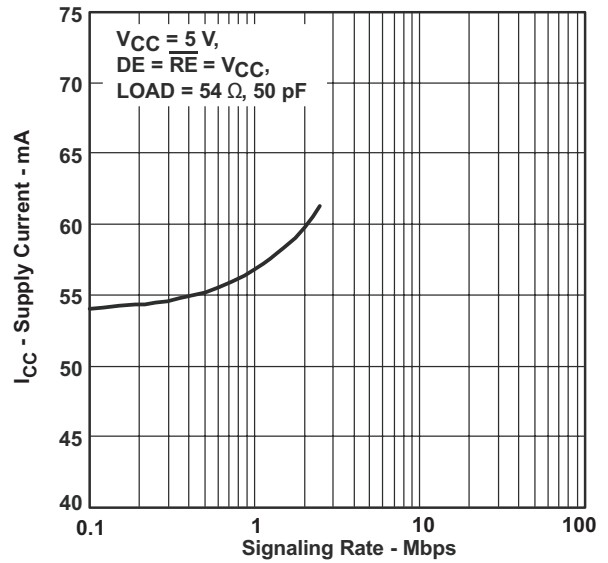


Figure 18.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE  
vs  
DRIVER LOAD CURRENT

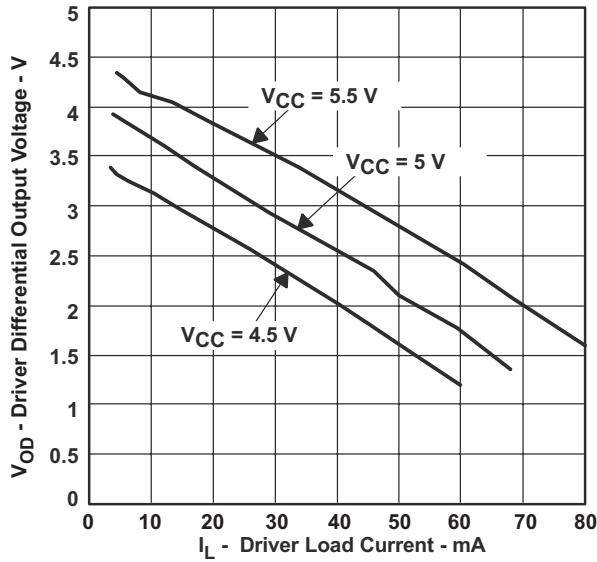


Figure 19.

RECEIVER OUTPUT VOLTAGE  
vs  
DIFFERENTIAL INPUT VOLTAGE

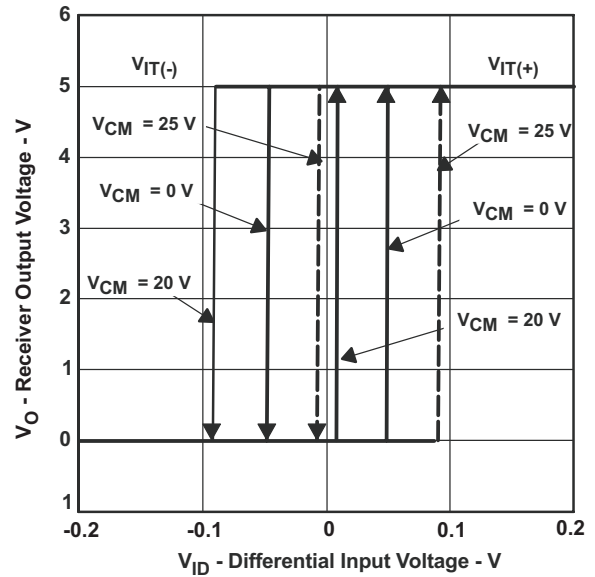


Figure 20.

TYPICAL CHARACTERISTICS (continued)

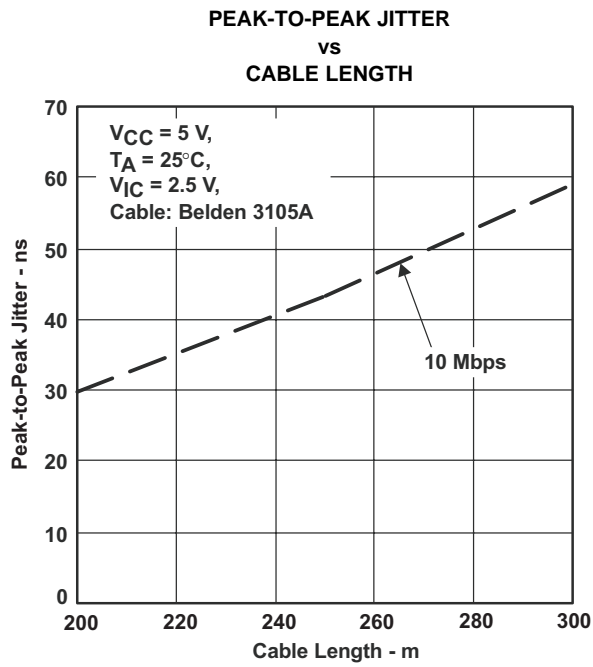


Figure 21.

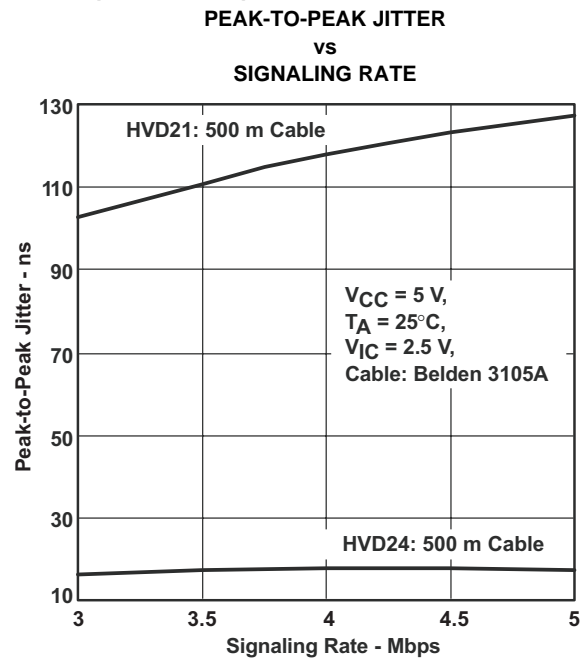


Figure 22.

## APPLICATION INFORMATION

### THEORY OF OPERATION

The SN65HVD21A integrates a differential receiver and differential driver with additional features for improved performance in electrically-noisy, long-cable, or other fault-intolerant applications.

The receiver hysteresis (typically 130 mV) is much larger than found in typical RS-485 transceivers. This helps reject spurious noise signals which would otherwise cause false changes in the receiver output state.

Slew rate limiting on the driver outputs reduces the high-frequency content of signal edges. This decreases reflections from bus discontinuities, and allows longer stub lengths between nodes and the main bus line. Designers should consider the maximum signaling rate and cable length required for a specific application, and choose the transceiver best matching those requirements.

When DE is low, the differential driver is disabled, and the A and B outputs are in high-impedance states. When DE is high, the differential driver is enabled, and drives the A and B outputs according to the state of the D inputs.

When  $\overline{RE}$  is high, the differential receiver output buffer is disabled, and the R output is in a high-impedance state. When  $\overline{RE}$  is low, the differential receiver is enabled, and the R output reflects the state of the differential bus inputs on the A and B pins.

If both the driver and receiver are disabled, (DE low and  $\overline{RE}$  high) then all nonessential circuitry, including auxiliary functions such as failsafe and receiver equalization is placed in a low-power standby state. This reduces power consumption to less than 5µW. When either enable input is asserted, the circuitry again becomes active.

In addition to the primary differential receiver, these devices incorporate a set of comparators and logic to implement an active receiver failsafe feature. These components determine whether the differential bus signal is valid. Whenever the differential signal is close to zero volts (neither high nor low), a timer initiates. If the differential input remains within the transition range for more than 250 microseconds, the timer expires and set the receiver output to the high state. If a valid bus input (high or low) is received at any time, the receiver output reflects the valid bus state, and the timer is reset.

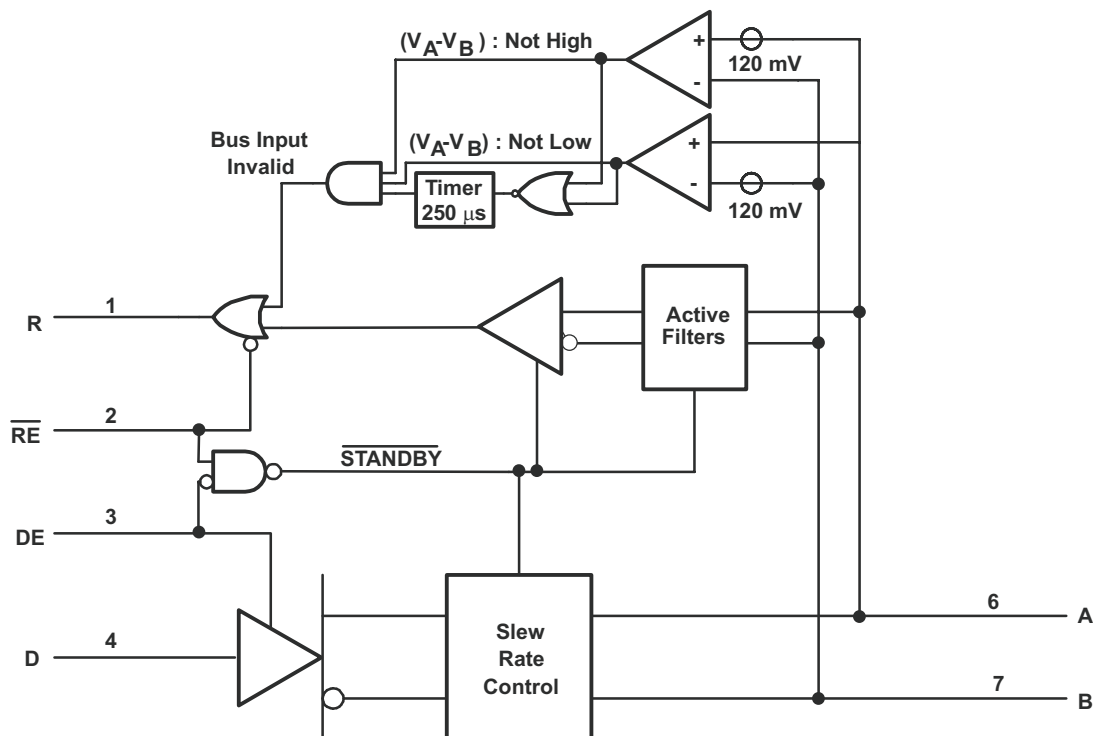


Figure 23. Function Block Diagram

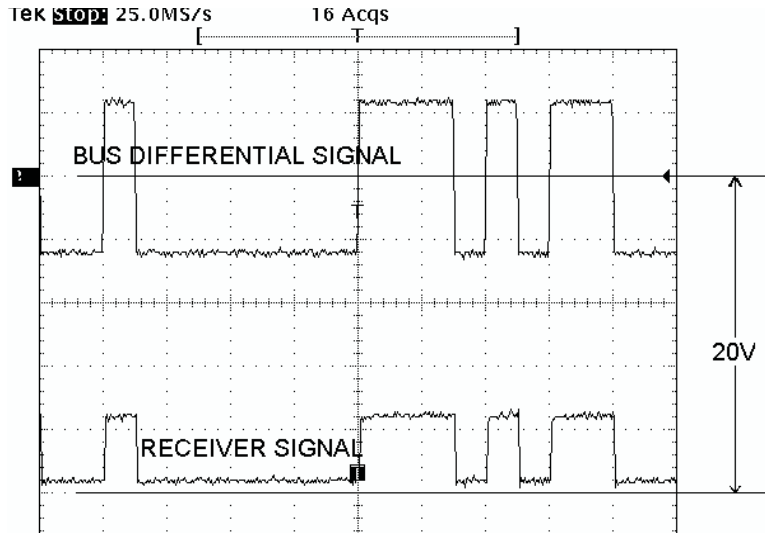


Figure 24. Receiver Operation With 20-V Offset on Input Signal

$$H(s) = k_0 \left[ (1-k_1) + \frac{k_1 p_1}{(s + p_1)} \right] \left[ (1-k_2) + \frac{k_2 p_2}{(s + p_2)} \right] \left[ (1-k_3) + \frac{k_3 p_3}{(s + p_3)} \right]$$

	k0 (DC loss)	p1 (MHz)	k1	p2 (MHz)	k2	p3 (MHz)	k3
Similar to 160m of Belden 3105A	0.95	0.25	0.3	3.5	0.5	15	1
Similar to 250m of Belden 3105A	0.9	0.25	0.4	3.5	0.7	12	1
Similar to 500m of Belden 3105A	0.8	0.25	0.6	2.2	1	8	1
Similar to 1000m of Belden 3105A	0.6	0.3	1	3	1	6	1

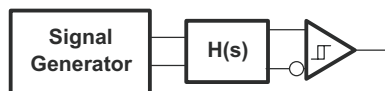


Figure 25. Cable Attenuation Model for Jitter Measurements



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVD21AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP21A	<a href="#">Samples</a>
SN65HVD21ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP21A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD21ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

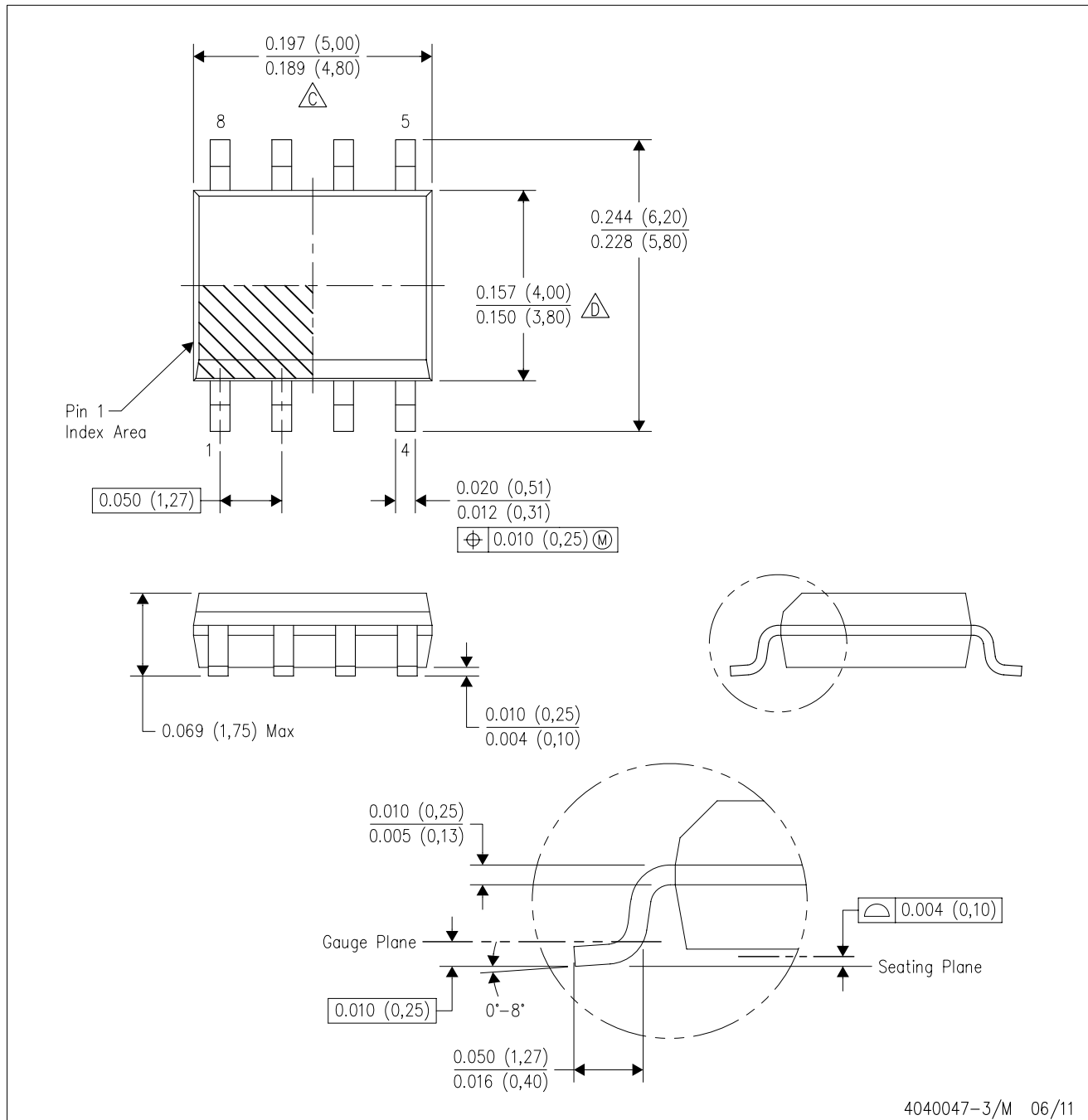


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD21ADR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.

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