DATA SHEET
HSCDTD008A

☐Electronic Compass function

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OVERVIEW

HSCDTD series is three axis terrestrial magnetism sensor of the digital output.
A high sensitivity magnetic sensor that detects the terrestrial magnetism element is mounted.
It provides with the drive circuit, the signal processing circuit, and the serial interface.
The electronic compass function is achieved by combining with our software.

FEATURES

- 3-Axis magnetic sensor with 0.15μT/LSB resolution
- Output, x, y, z axis magnetic field strength.
- Serial interface
  I2C slave interface (SS、FS、FS+、HS) PhilipsI2C revision .2.1 and
  NXP UM10204 I2C-bus specification and user manual Rev.03-19 June 2007 is supported.
-8 pin, FLGA package
- Package size : 1.6mm x 1.6mm x t0.7mm
- Low current consumption
- Lead free, RoHS instruction, Halogen free conforming

- Function
  - Initialization Function (Power on reset)
  - Functional Mode: Stand-by Mode; Active Mode
  - Measurement: Force State; Normal State (Data Rate 0.5,10,20,100Hz Selectable)
  - Temperature Compensation Function
  - Offset Calibration Function
  - Data Ready Function
  - Offset Drift Function
  - Self Test Function
  - FIFO Function (8 depth)

- Supply Voltage
  - Analog 1.7 to 3.6 V
  - Digital 1.65V to AVDD

- Operating Temperature -40 to +85℃

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Analog Supply Voltage	AVDD	-0.3	-	+5.0	V
Digital Supply Voltage	DVDD	-0.3	-	+5.0	V
Input Voltage	VIN	-0.3	-	+5.0	V
Strage Temperature	Tstg	-40	-	+125	℃

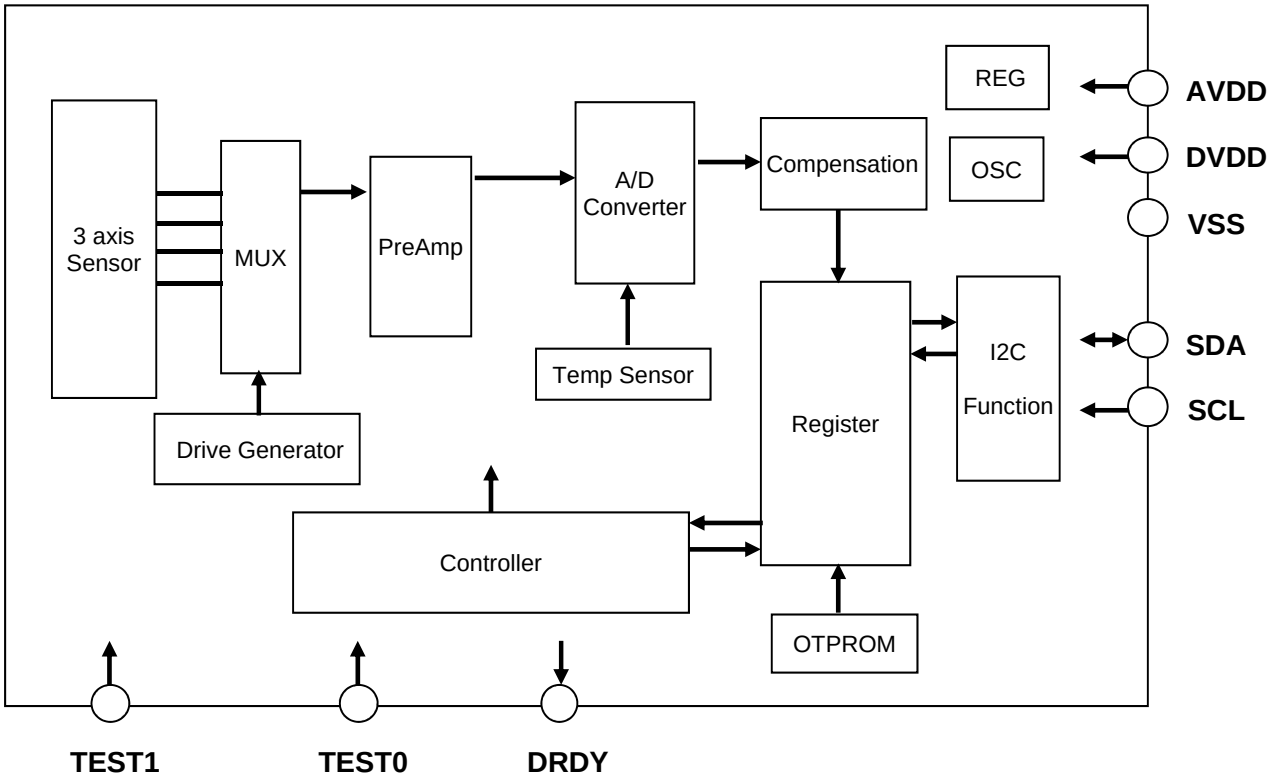
ELECTRICAL / MAGNETIC CHARACTERISTICS

Unless otherwise specified: AVDD = 2.5V, DVDD_IO = 1.8V, Ta = 25℃

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Analog Supply Voltage	AVDD	1.7	2.5	3.6	V
Digital Supply Voltage	DVDD	1.65	1.8	AVDD	V
Supply Current Consumption (Total)					
Stand-by Mode	IDD	-	3	10	μA
Active Mode, Average (ODR = 10Hz)	IDD	-	60	85	μA
Active Mode, Maximum	IDD	-	2.5	3	mA
Operating Temperature	Ta	-40	-	+85	℃
Measurement Range (*1)		-7.2	-	+7.2	mT
Measurement Nonlinearity (±1.2mT)		-2	-	+2	%FS
Measurement Sensitivity		-	0.150	-	μT/LSB
Input Voltage High	VIH	0.8 x DVDD	-	DVDD	V
Low	VIL	0	-	0.2 x DVDD	V
Output Voltage High	VOH	0.9 x DVDD	-	DVDD	V
Low	VOL	0	-	0.1 x DVDD	V
Output Data Rate (Normal State)	ODR	0.5	-	100	Hz
Output Resolution		-	-	15	bit
Measurement Time		-	-	5	msec
Control Timing					
Turn On Time (Off to Stand-by Mode)		-	-	3	msec
Turn On Time (Stand-by to Active Mode)		-	-	5	μsec
Turn Off Time (Active to Stand-by Mode)		-	-	5	μsec

*1. "Measurement range : ±7.2" is total value of 3-Axis measurement. One axis is ±2.4mT.

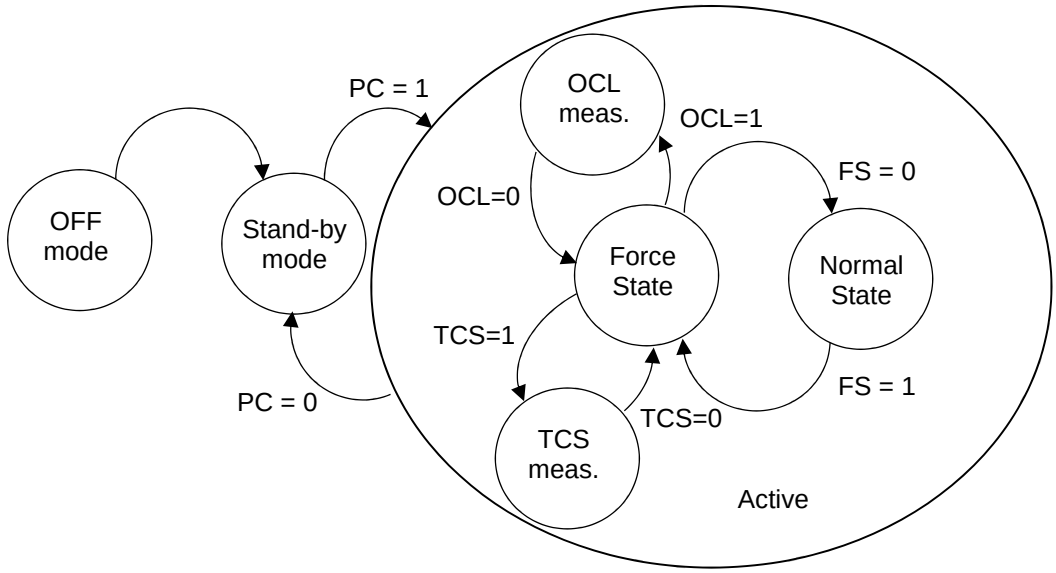
BLOCK DIAGRAM



FUNCTIONAL SPECIFICATIONS

Function List

Name	Description
Initialization	Power on reset is performed by turning on the power. All circuits and registers are set to default and mode is set to stand-by mode automatically by POR. Software reset is performed by writing to control register. All register is reloaded form OTP and internal compensation table is reloaded.
Self Test	Self test confirm the operation on sensor by register command
Functional Modes	This sensor has stand-by mode and active mode for power control. There are two states in active mode.
Off mode	The sensor is not active when AVDD and/or DVDD_IO are disable.
Stand-by Mode	Low power waiting state. Stand-by mode can access to register. Reading/Writing register is enable on stand-by mode.
Active Mode	Change from stand-by to active mode by register command to control register.
Force State	Start to measure and output data by register command. Force state is default.
Normal State	Perform to measure and output data by using the internal timer trigger.
Data Ready Function	Informs when new measured results are updated. It is possible that data ready inform the signal to the DRDY pin when updated output data.
Offset Calibration Function	Sensor offset can be canceled by using internal DAC circuit and digital compensation function when the register command is set.
Offset Drift Function	When magnetic field strength have offset drift, output data values can be compensated by writing in the offset value registers.
Temperature Measurement Function	Retrieve temperature data from internal temperature sensor. Temperature data is used for internal compensation for output data.
Temperature Compensation Function	Compensate gain in digital circuit by temperature measurement results.
FIFO Function	This products have 8 depth FIFO memory



State Machine

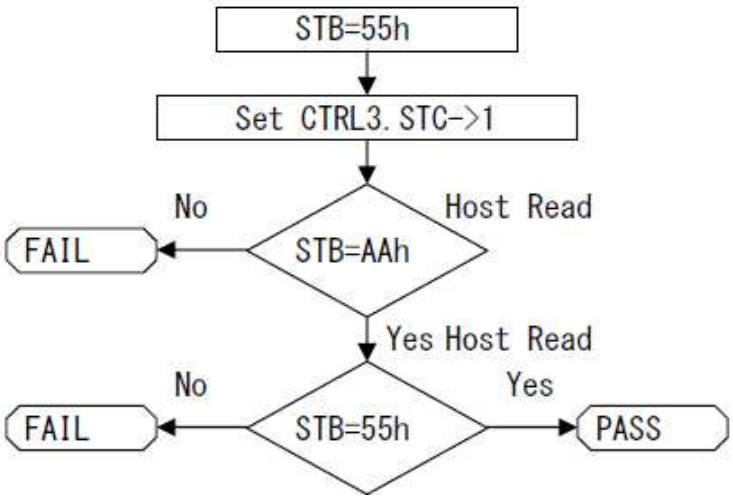
FUNCTIONAL SPECIFICATIONS (Continued)

Initialization

- All internal circuits and all register values are initialized with POR (Power On Reset) after power-on.
- After initialization, the functional mode move to standby mode automatically.
- The software reset set by the register command SRST=1 makes all register value to defaults and reload the compensation values for internal sensor calculation.

Selftest

-Selftest confirm with the inner I/F and the digital logic.
-Selftest is performed with reading the STB register and setting the register command CTRL3 STC bit to Hi.
-The following chart show the procedure of selftest .
-The value of response register STB is back to 55h after reading it.



The flow chart of selftest

FUNCTIONAL SPECIFICATIONS (Continued)

Modes

OFF mode

-The sensor is not active when AVDD and/or DVDD_IO are disable.

-The following table show the each status of off mode.

AVDD	DVDD	Operation State
0V	0V	Sensor is not active, There are no inference on the interface bus.
0V	1.65V to 3.6V	Sensor is not active, There are no inference on the interface bus.
1.7V to 3.6V	0V	Sensor is not active, There are no inference on the interface bus.

Stand-by mode

-After loading the POR (Power On Reset), internal state is moved to the standby mode automatically.

-Read and Write access function is limitative as follows at the stand-by mode.

-Write: (CTRL3) FORCE, TCS and STC are disable

-Read: All resister can be read.

-Register is cahnged form the Active mode to the Stand-by mode by set PC=0(CNTL1) as follows.

Active mode

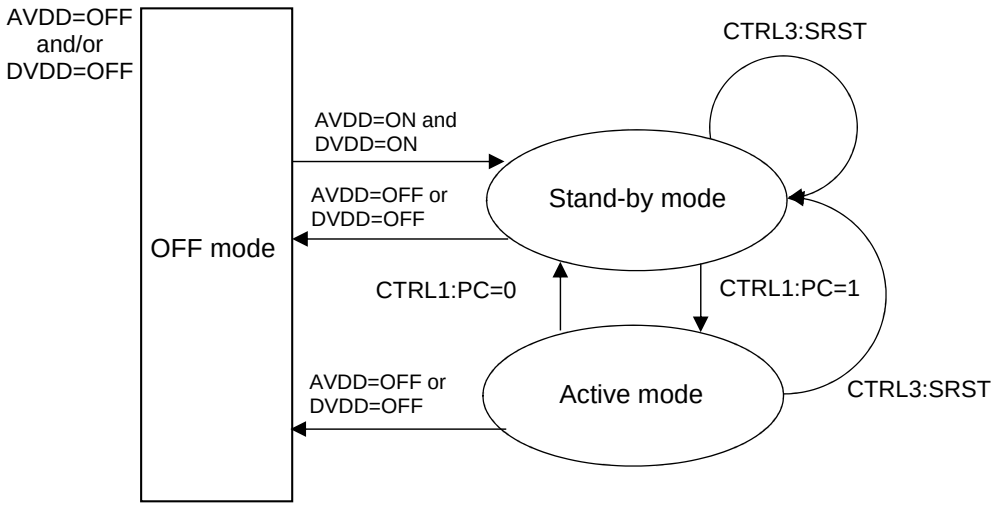
-At active mode, each function can be performed by setting control register 3(CTRL3).

-To transfer to active mode, it sets the PC=1(CTRL1).

-There are two types of measurement state. One is periodical measurement "Normal state " controlled by inner timer. and the other is "Force state" controlled by register command form outside.

-The measurement state is selectable with FS bit on control register 1(CTRL1)

-The default of measurement state is the force state (FS=1) after POR or reset running.



The diagram on mode transfer

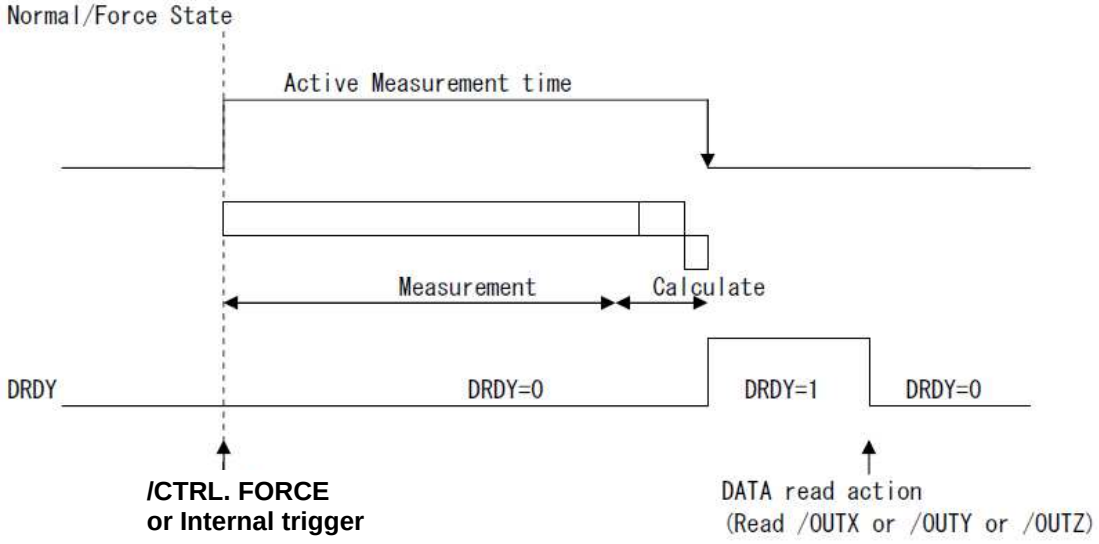
FUNCTIONAL SPECIFICATIONS (Continued)

Contorol function for Data Ready terminal with CTRL2 register

CNRL2 bit	Bit Name	Default	Condition
4	DEN	0	Output control on DRDY PIN 0 = Disable 1 = Enable
3	DRP	1	The polarity setting on DRDY PIN 0 = Active Low 1 = Active High

Data ready function

-This function is used for notice that output data was updated.
-Data ready output is enable on the outside terminal (DRDY PIN), when the data was updated.
- Information of dada ready can be red with the status register (STAT).
-DRDY is changed to LOW after reading data on the output register.
- Conditions of data ready function can be set on the control register (CTRL2).



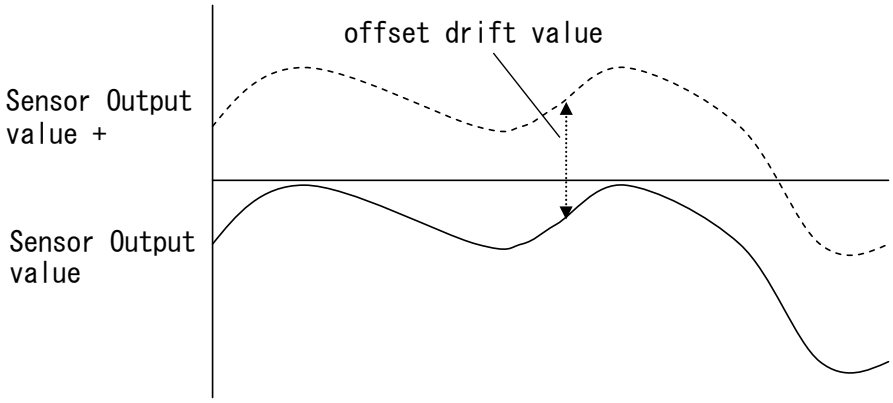
FUNCTIONAL SPECIFICATIONS (Continued)

Offset calibration function

-This function is enable when the control register (CNTL3:OCL) was set to Hi during the Force State.
-The offset value for inner ADC output is calculated with the measured sensor offset, and then set compensation values for the amplitude offset and also the digital offset automatically.
-The OCL bit is changed to be low after updating the compensation offset value, and then the status is back to before measurement.

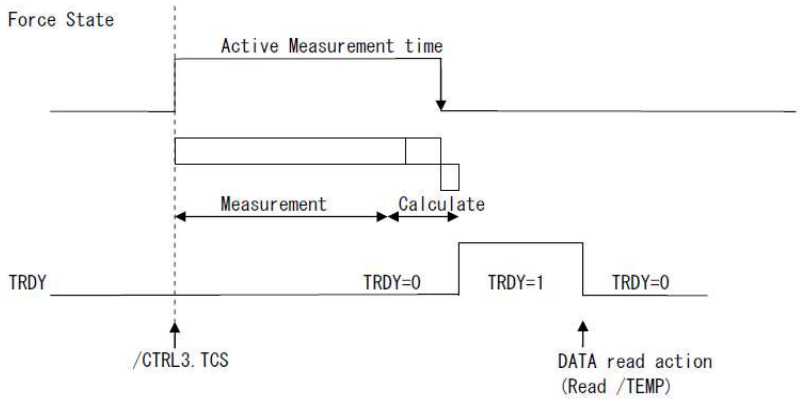
Offset drift function

-This function can make the digital compensation output that is add with values wrote by the host CPU on the offset drift register (OFFX,OFFY,OFFZ).
-Offset drift values can be set with 15bit signed value.



Temperature Measurement and Compensation Function

- The temperature measurement function will be executed when the register command TCS is set "1" during the Force State. After measurement, TCS bit change to "0" and back to before measurement.
-The measurement result is wet on the temperature value register (TEMP).
-Sensor output values are compensated with the temperature value register(TEMP)
-After temperature measurement, the status register TRDY (STAT1) change to"1". This register is cleared by reading the TEMP register. And the status of temperature measurement Active/inactive can be output on the external DRDY Pin with setting the bit DRTS at the control register CTRL2.



FUNCTIONAL SPECIFICATIONS (Continued)

FIFO Function

- This products have 8 depth FIFO memory.
- This mode is performed when the control register /CTRL2.FF(1Ch) is set to Hi.
- Data is stored in FIFO and FIFO pointer is shown in /FFPT.FP(19h).
- /STAT.FFU(18h) is performed when /FFPT.FP = 8.
- /STAT.DOR(18h) is performed when new data is stored and oldest data is cleared during FP=8.
- In case of FP=1,2,3,4,5,6,7,8 , DRDY =1(/CNTL2.DEN=1).

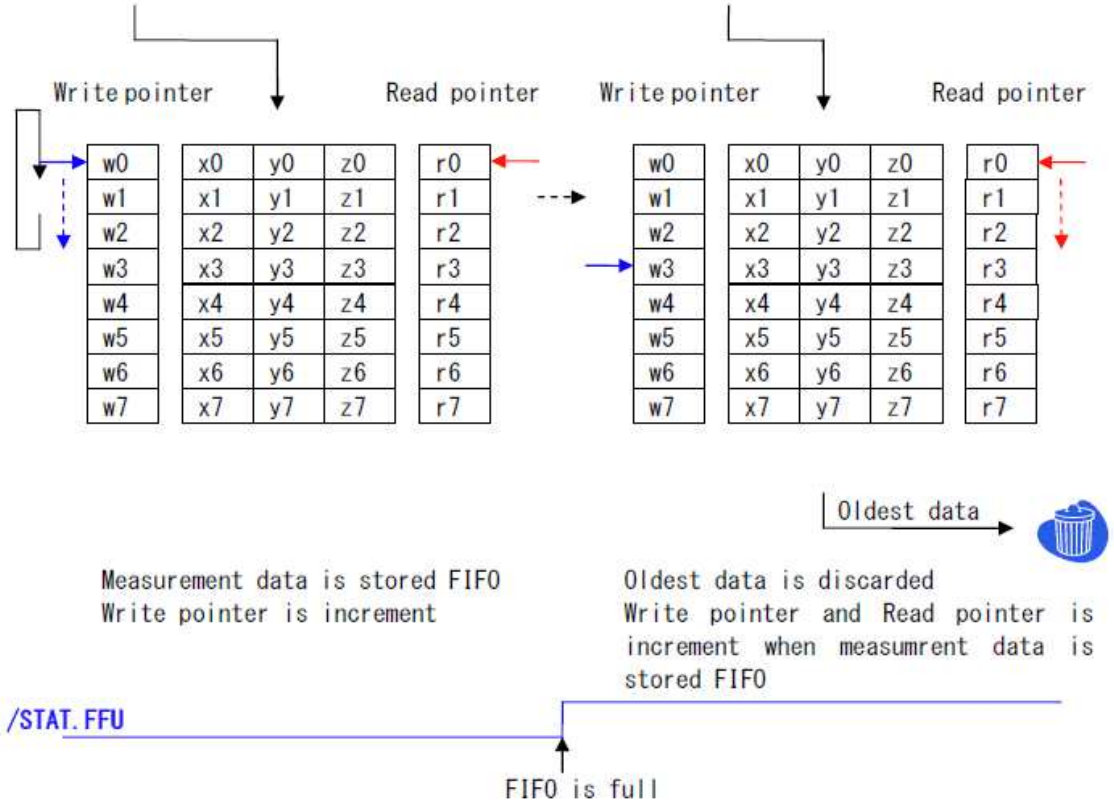


Figure. FIFO Structure

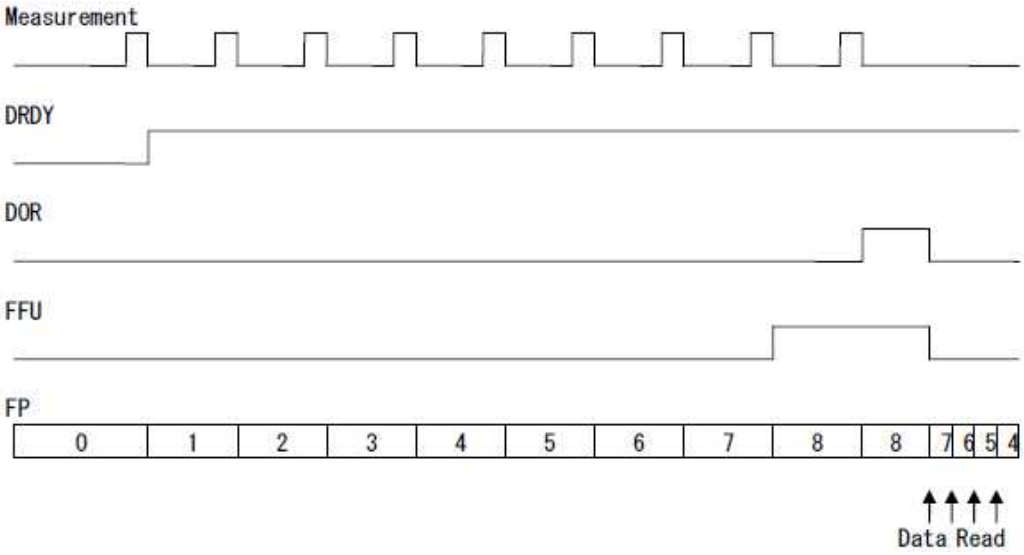


Figure. FIFO Event (DRDY , DOR , FFU)

FUNCTIONAL SPECIFICATIONS (Continued)

FIFO Function

- When CTRL2.FCO is set to "1", Data is stored in the following manner.
- The data is set to FIFO only if the distance of maesurement data against the all data in FIFO is over the "ITHR(26h-27h)" distance.
- When CNTL2.FCO is set to "1" and CNTL2.AOR is set to "0", if there is one axis over the distance, the data is set to FIFO. ("OR" condition)
- When CNTL2.FCO is set to "1" and CNTL2.AOR is set to "1", only if all axes over the distance, the data is set to FIFO. ("AND" condition)

DF(axis) = ABS(/MEAS(axis) - /FIFO(axis))

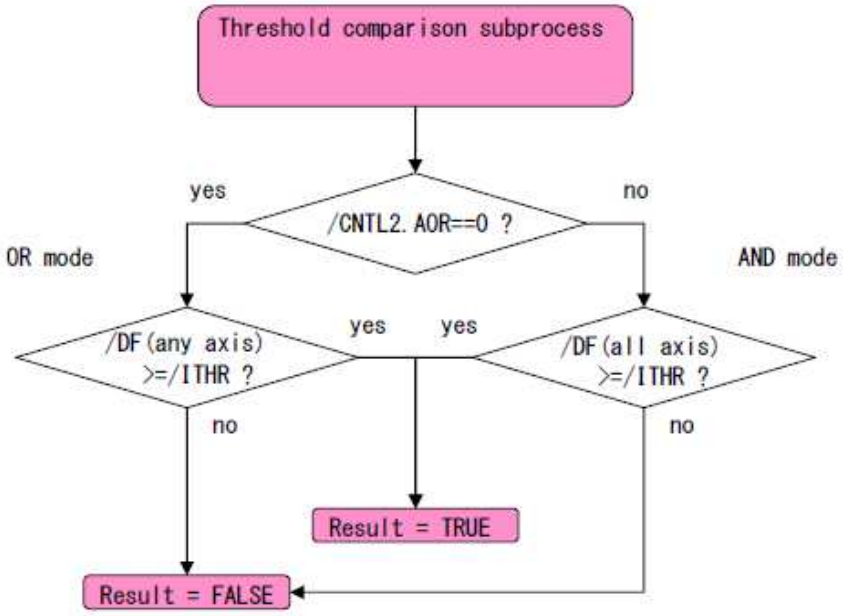
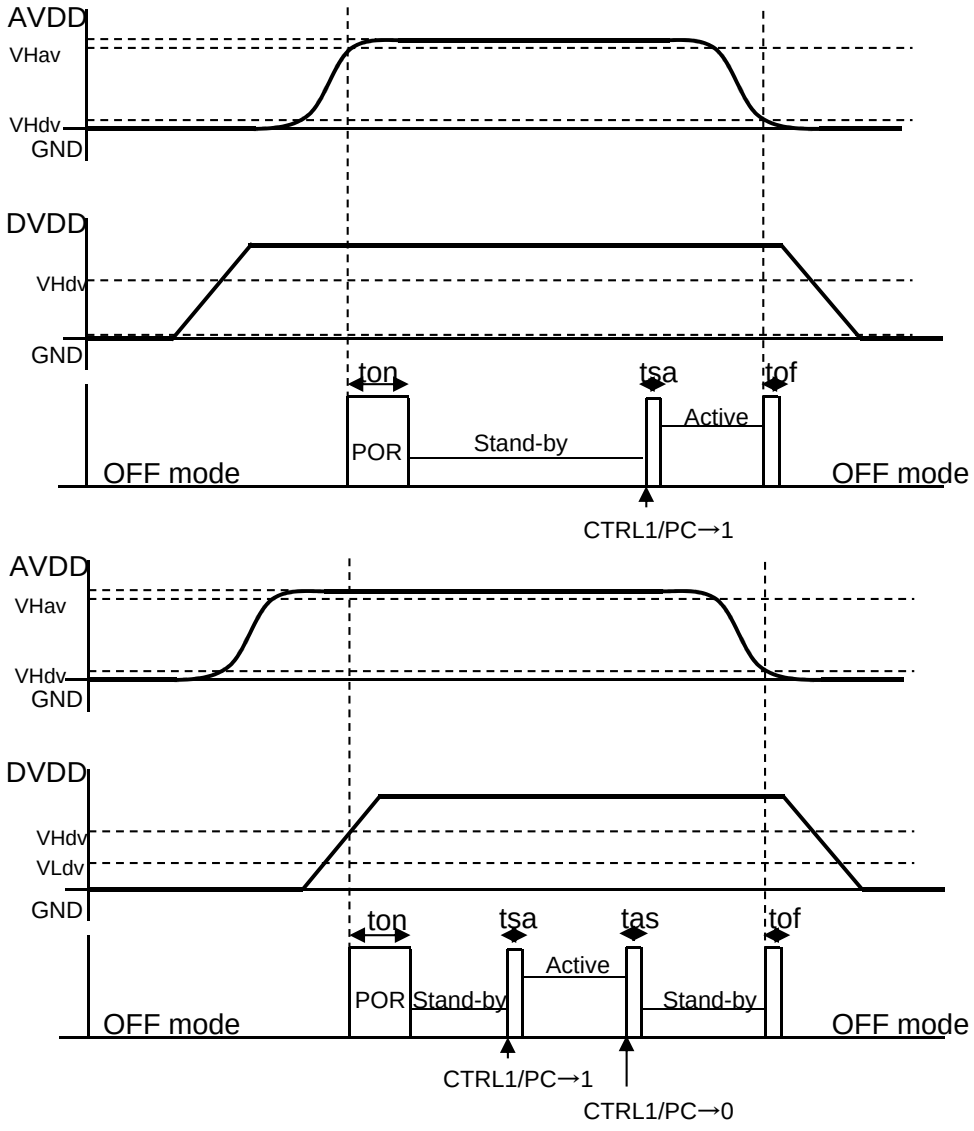


Figure. Multiple comparison task subprocess

CONTROL TIMING SPECIFICATIONS

POWER SUPPLY SEQUENCE



Parameters on Supply voltage sequence (All Condition)

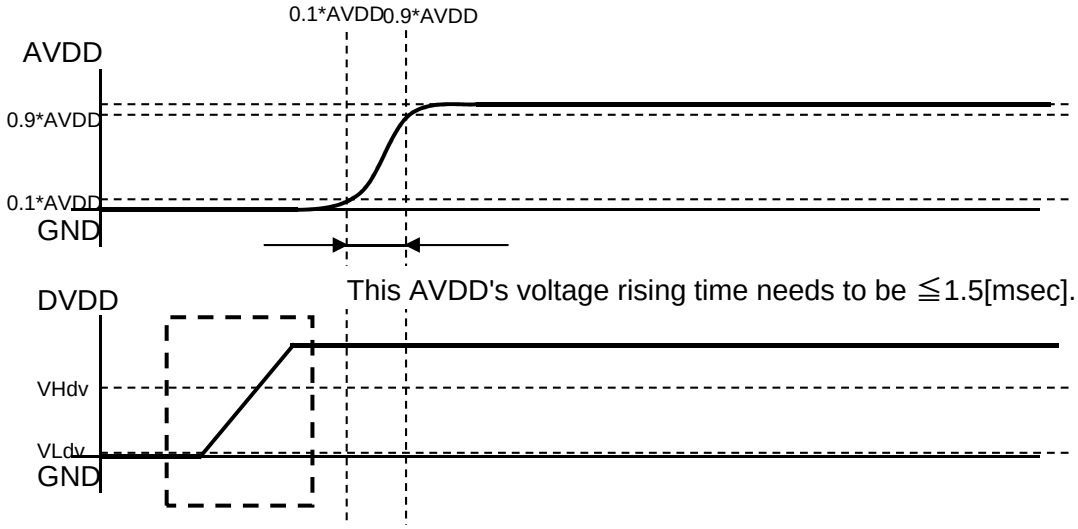
Transition	Symbol	Typ.	Max.	Unit
OFF→Stand-by	ton	-	3	ms
Stand-by→Active	tsa	-	5	μs
Active→Stand-by	tas	-	5	μs
Active or Stand-by→OFF	tof	-	10	ms

Parameters on Supply voltage sequence (All Condition)

Characteristics	Symbol	Min.	Max.	Unit
AVDD ON	VHav	1.53	-	V
AVDD OFF	VLav	-	0.17	V
DVDD ON	VHdv	1.53	-	V
DVDD OFF	VLdv	-	0.17	V

CONTROL TIMING SPECIFICATIONS (Continued)

Note No limitation in the turn on timing of the AVDD and the DVDD_IO voltage.
Case 1:
When the DVDD_IO voltage turns on initially,
After the DVDD_IO voltage has risen (reached VHdv)
the AVDD's voltage rising slope must rise (reach 0.9*AVDD) within 1.5 [msec].

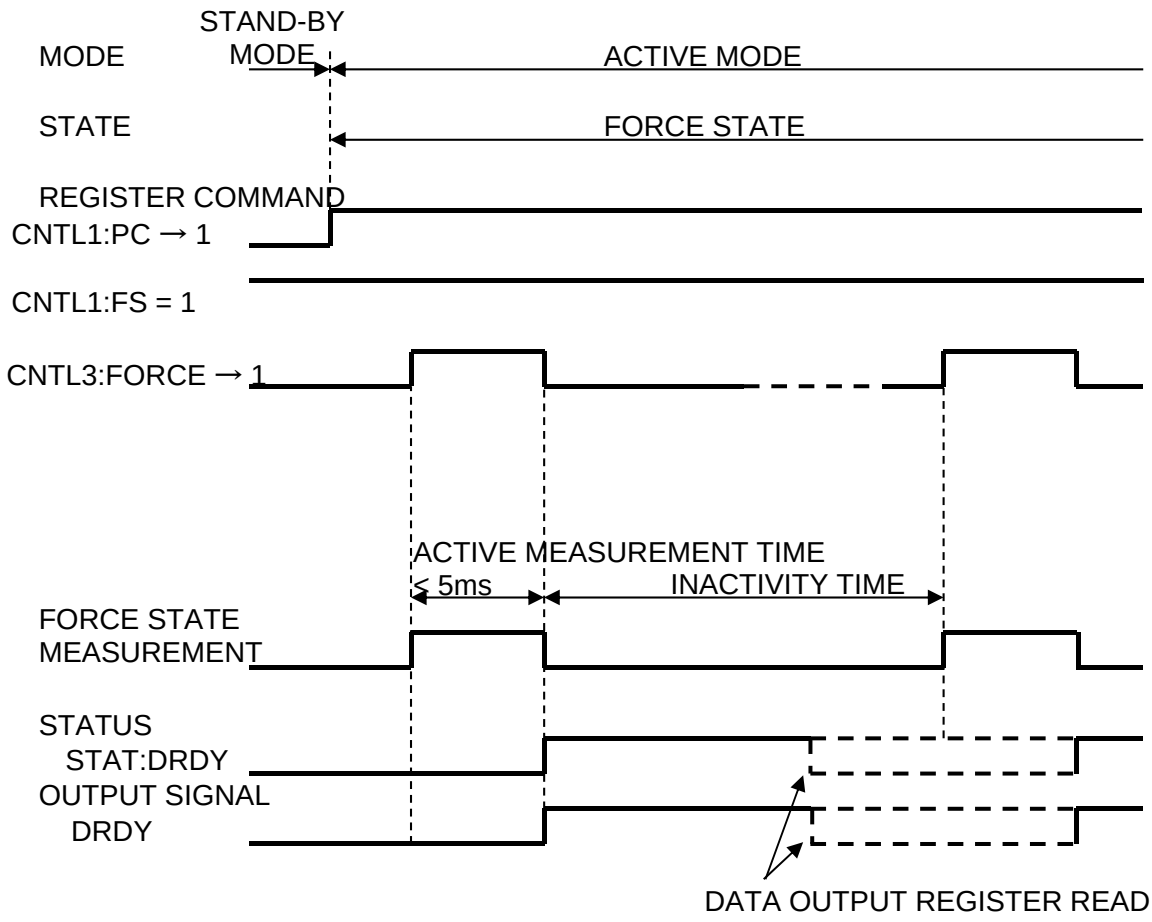


When the DVDD_IO voltage turns on initially

CONTROL TIMINGS (Continued)

Force state

- Force state is used for synchronous measurement (selected from register CTRL3, bit FRC), and measurement starts after forced register command to register via bus.
- Functional mode changes from Stand-by mode to Active mode by setting register (Control1: bit PC) to "1".
- Force state is set by control register (CNTL1: bit FS) "1".
- Acquired data stored to output register (OUTX, OUTY, OUTZ), and status register (STAT: bit DRDY) is set to "1" and output signal (DRDY PIN) are set to active.
- Output on external DRAY PIN is set by control register (CNTL2)
- During reading data, out put register is not updating. After reading is complete, reading data is updated.
- Change of state from Normal to Force is valid after measurement if control register is set during the Active measuring in Normal state.

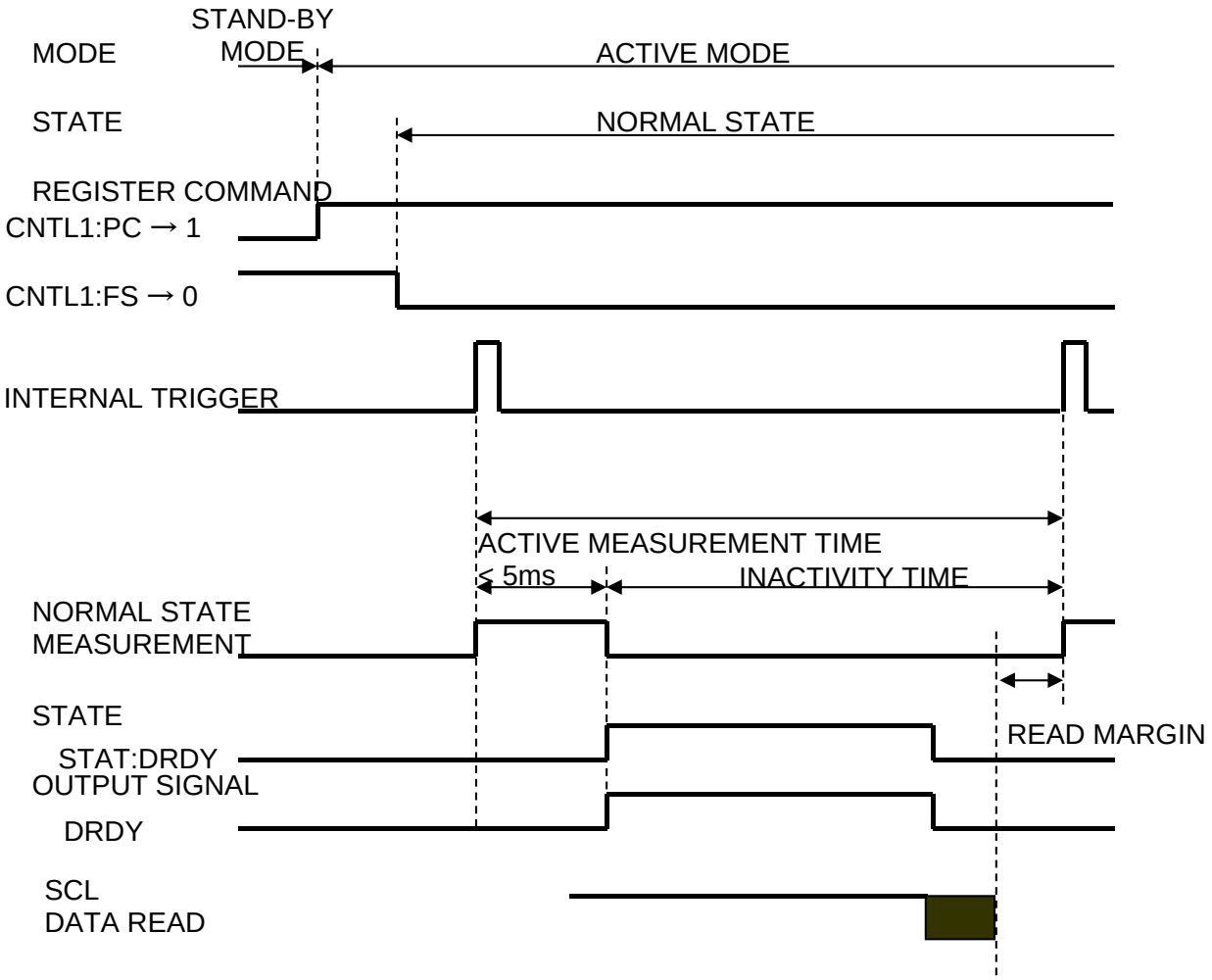


Measurement control timing (Force state)

CONTROL TIMINGS (Continued)

Normal state

- Normal state is continuous measurement state, and when Normal state is set by setting “0” to control register (CNTL1: bit FS), channels measurement is started.
- Measurement time and interval are managed with internal clock.
- Functional mode changes from Stand-by mode to Active mode by setting register (CNTL1: bit PC) to "1".
- Output data rate (ODR) is selectable with 0.5Hz or 100Hz by register (CNTL1: bit ODR).
- Acquired data are stored to register (OUTX, OUTY, OUTZ), status register (STAT: bit DRDY) is set to "1" and output PIN signal are control with (CNTL2:bit DEN).



Note: READ MARGIN is need more than "0msec" in normal state.

. DATA READ Time should be set less than 1msec including clock starch.
Minimum case is happen in ODR=11(100Hz) on measurement function.

Measurement control timing (Normal state)

CONTROL INTERFACE CONNECTIONS

Symbol	Pin Number	Detail
VSS	1	Analog and Digital Ground
AVDD	2	Terminal for analog supply voltage
DVDD	3	Terminal for digital supply voltage
DRDY	4	Output terminal for data ready signal The active level is selectable with LOW or HIGH. The output is selectable with enable or disable for external terminal The internal circuit is pull down after initializing.
TEST0	5	It is used for only test on product line. Connect this terminal to the GND or NC at using sensor.
TEST1	6	It is used for only test on product line. Do not connect it to any more at using sensor.
SCL	7	Clock bus line under using I2C interface
SDA	8	Data bus line under using I2C interface

INTERFACE SPECIFICATIONS

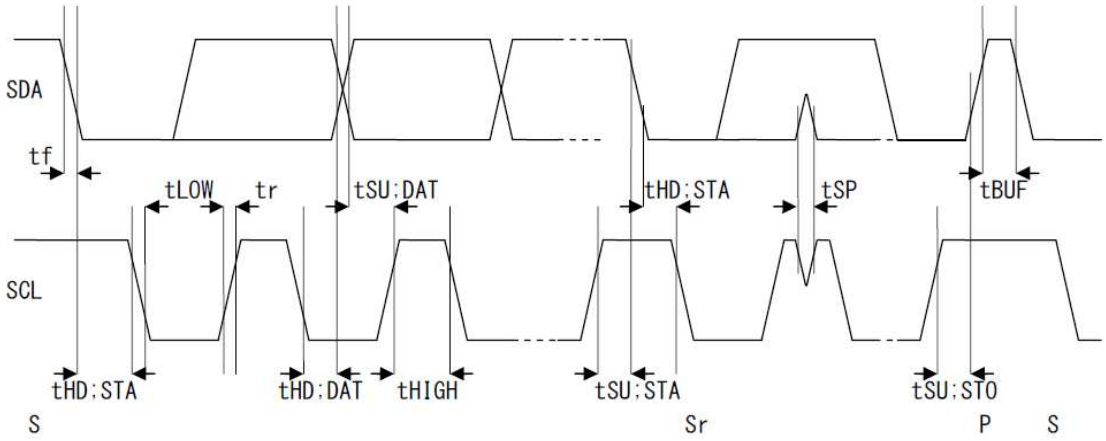
I2C SLAVE INTERFACE

- Conformable to Philips I2C-Bus Specification Version 2.1 and
  NXP UM10204 I2C-bus specification and user manual Rev.03-19 June 2007
- Slave address is fixed '0001100'. (7bit device adressing) *1
- Support Stabderd mode, Fast mode , Fast mode Plus and Hi speed mode.
- It is seemless change from Fast mode to Hi speed mode to use the master code (00001XXX)
- Support Multiple Read and Write mode.
- Clock stretch function is not available.

Note:*1 LSB 2bit adress can be chage on only the products process.

I2C bus interface timing diagram 1

Parameters	Symbol	Standard Mode		Fast mode		Fast mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Hold time (re)start condition	$t_{HD:STA}$	4.0	–	0.6	–	0.26	–	us
Low period of the SCL clock	t_{LOW}	4.7	–	1.3	–	0.5	–	us
High period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	0.26	–	us
Set-up time for (re)start condition	$t_{SU:STA}$	4.7	–	0.6	–	0.26	–	us
Data hold time	$t_{HD:DAT}$	0	–	0	–	0	–	us
Data set-up time	$t_{SU:DAT}$	250	–	100	–	50	–	ns
Rise time of SDA and SCL	t_r	–	1000	–	300	–	120	ns
Fall time of SDA and SCL	t_f	–	300	–	300	–	120	ns
Set-up time for stop condition	$t_{SU:STO}$	4.0	–	0.6	–	0.26	–	us
Bus free time between a stop and start condition	t_{BUF}	4.7	–	1.3	–	0.5	–	us
Capcacitive load for SDA/SCL	C_b	–	400	–	400	–	300	pF
Data valid time	$t_{VD:DAT}$	–	3.45	–	0.9	–	0.45	us
Data valid acknowledge time	$t_{VD:ACK}$	–	3.45	–	0.9	–	0.45	us
Noise margin at the low level	VnL	0.1* DVDD	–	0.1* DVDD	–	0.1* DVDD	–	V
Noise margin at the high level	VnH	0.2* DVDD	–	0.2* DVDD	–	0.2* DVDD	–	V



INTERFACE SPECIFICATIONS

I2C SLAVE INTERFACE

I2C bus interface timing diagram 2

Parameters	Symbol	Hs-mode C_b=100pF (max)		Hs-mode C_b=400pF		Unit
		Min.	Max.	Min.	Max.	
SCLH clock frequency	f_{SCLH}	0	3.4	0	1.7	MHz
Hold time (re)start condition	$t_{HD:STA}$	160	–	160	–	ns
Low period of the SCLHclock	t_{LOW}	160	–	320	–	ns
High period of the SCLH clock	t_{HIGH}	60	–	120	–	ns
Set-up time for (re)start condition	$t_{SU:STA}$	160	–	160	–	ns
Data hold time	$t_{HD:DAT}$	0	70	0	150	ns
Data set-up time	$t_{SU:DAT}$	10	–	10	–	ns
Rise time of SCLH	t_{rCL}	10	40	20	80	ns
Fall time of SCLH	t_{fCL}	10	40	20	80	ns
Rise time of SDAH	t_{rDA}	10	80	20	160	ns
Fall time of SDAH	t_{fDA}	10	80	20	160	ns
Set-up time for stop condition	$t_{SU:STO}$	160	–	160	–	ns
Capcacitive load for SDA/SCL	C_b	–	100	–	400	pF
Noise margin at the low level	V_{nL}	0.1* DVDD	–	0.1* DVDD	–	V
Noise margin at the high level	V_{nH}	0.2* DVDD	–	0.2* DVDD	–	V

INTERFACE SPECIFICATIONS (Continued)

- Data transfers follow the combined format with 7-bit addressing of I2C interface.
- Data is transferred with the most significant bit (MSB) first and little endian.
- Auto-increment of previous accessed register address is available when the internal register address is written during the first data byte. Data then can be transferred continuously.

Bus protocol definitions

S: Start condition
SAD+W: Slave Address + write bit
SAD+R: Slave Address + read bit
SAD+R/W: Slave Address + read or write bit
SAK: Slave Acknoledge
REG: Register Address (2nd byte)
Sr: Repeat Start condition
A: (Master) Acknowledge
/A: (Master) Non-Acknowledge
DATA: Data (load)
P: Stop condition
M-code: Master code (00001XXX)

Read Formats

One byte read flow

master	S	SAD+W		REG		SR	SAD+R			/A	P
slave			SAK		SAK			SAK	DATA		

Multiple byte reads flow

master	S	SAD+W		REG		SR	SAD+R			A		/A	P
slave			SAK		SAK			SAK	DATA		DATA		

Write Format

One byte wirte flow

master	S	SAD+W		REG		DATA		P
slave			SAK		SAK		SAK	

Multiple byte writes flow

master	S	SAD+W		REG		DATA		DATA		P
slave			SAK		SAK		SAK		SAK	

HS mode data trasfer

HS mode is enable after writeing Mcode.

speed	F/S-mode			Hs-mode						FS-
master	S	Mcode	/A	SR	SAD +R/W		DATA	/A	P	
slave						A	DATA	A		
									Hs- continue	
master									SR	SAD +R/W

REGISTER DEFINITIONS

- Register addresses and definitions are as follows.
- Sensor output values are signed integer (2's compliment) presentation and little Endian order.

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
00-0B	---	---	---	---	---	---	---	---	---	00
0C	SelfTest response	STB[7:0]								55
0D	"More Info version"	0	0	0	1	0	0	0	1	11
0E	"More Info ALPS"	0	0	0	1	0	1	0	1	15
0F	"Who I am"	0	1	0	0	1	0	0	1	49
10	Output X LSB	OUTX[7:0]								00
11	Output X MSB	OUTX[15:8]								00
12	Output Y LSB	OUTY[7:0]								00
13	Output Y MSB	OUTY[15:8]								00
14	Output Z LSB	OUTZ[7:0]								00
15	Output Z MSB	OUTZ[15:8]								00
16-17	---	---	---	---	---	---	---	---	---	00
18	Status	---	DRDY	DOR	---	---	FFU	TRDY	ORDY	00
19	FIFO Pointer Status	---	---	---	---	FP				00
1A	---	---	---	---	---	---	---	---	---	00
1B	Control1	PC	---	---	ODR[1:0]		---	FS	---	0A
1C	Control2	AVG	FCO	AOR	FF	DEN	DRP	DTS	DOS	04
1D	Control3	SRST	FORCE	---	STC	---	---	TCS	OCL	00
1E	Control4	MMD		---	RS	AS	---	---	---	80
1F	---	---	---	---	---	---	---	---	---	0
20	Offset X LSB	OFFX[7:0]								00
21	Offset X MSB	---	OFFX[14:8]							00
22	Offset Y LSB	OFFY[7:0]								00
23	Offset Y MSB	---	OFFY[14:8]							00
24	Offset Z LSB	OFFZ[7:0]								00
25	Offset Z MSB	---	OFFZ[14:8]							00
26	ITHR_L	ITHR_L								00
27	ITHR_H	---	---	ITHR_H						00
28-2F,30	---	---	---	---	---	---	---	---	---	00
31	Temperature value	TEMP[7:0]								19
32-5F	---	---	---	---	---	---	---	---	---	00

REGISTER DESCRIPTIONS

Self Test Response Register (STB)

Address : 0Ch, Self Test Response (Read Only)

Bit	Name	Description
7:0	STB 7:0	Self test starts by STC bit (CNTL3 register). AAh is stored when CNTL3: bit STC sets to 1. 55h is stored after STB register is read.

Information Registers

Address : 0Dh, "More Info version" (Read Only)

Bit	Name	Description
7:0	INFO1 7:0	Information Value1 (11h)

Address : 0Eh, "More Info ALPS" (Read Only)

Bit	Name	Description
7:0	INFO2 7:0	Information Value2 (15h)

Address : 0Fh, "Who Am I" Value (Read Only)

Bit	Name	Description
7:0	WIA 7:0	Identify byte (49h)

REGISTER DESCRIPTIONS (Continued)

Output Data Register (OUTX, OUTY, OUTZ)
- 14bit integer and 1FFFh (+8191d) ～ E000h (-8192d)
- 15bit integer and 3FFFh (+16383d) ～ C000h (-16384d)

Address : 10h, X-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTX 7:0	X-axis Output Data, Signed Integer.

Address : 11h, X-axis Output Data MSB (Read Only)

Bit	Name	Description
7:0	OUTX 15:8	X-axis Output Data, Signed Integer.

Address : 12h, Y-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTY 7:0	Y-axis Output Data, Signed Integer.

Address : 13h, Y-axis Output Data MSB (Read Only)

Bit	Name	Description
7:0	OUTY 15:8	Y-axis Output Data, Signed Integer.

Address : 14h, Z-axis Output Data LSB (Read Only)

Bit	Name	Description
7:0	OUTZ 7:0	Z-axis Output Data, Signed Integer.

Address : 15h, Z-axis Output Data MSB (Read Only)

Bit	Name	Description
7:0	OUTZ 15:8	Z-axis Output Data, Signed Integer.

Note:
MSB, bit7 (and MSB, bit6 used under 14bit output) is copied
signed value "0": Positive or "1":Nagative.

Status Register (STAT)

Address : 18h, Status (Read Only)

Bit	Name	Description
7	X	Not Used
6	DRDY	Data Ready Detection 0 = Not Detected, 1 = Detected
5	DOR	Data Overrun Detection 0 = Not Detected, 1 = Detected Note: if Read Output Data Register.
4:3	X	Not Used
2	FFU	FIFO full alarm 0 = not Full(Default), 1 = Full
1	TRDY	Must be use Default setting. 0 = (Default) ※
0	ORDY	Must be use Default setting. 0 = (Default) ※

※. The change of this bit is prohibited.

REGISTER DESCRIPTIONS (Continued)

FIFO Pointer Status Register (FFPT)

Address : 19h, FIFO Pointer Status (Read Only)

Bit	Name	Description
7:4	X	Not Used (Read Only)
3:0	FP	Number of data in FIFO : 0 - 8

Control 1 Register (CTRL1)

Address : 1Bh, Control 1 (Write/Read)

Bit	Name	Description
7	PC	Power Mode Control 0 = Stand-by Mode (Default), 1 = Active Mode
6:5	X	Not Used (Read Only)
4:3	ODR 1:0	Output Data Rate Control in Normal State 00 = 0.5 Hz 01 = 10Hz (Default) 10 = 20Hz 11 = 100Hz
2	X	Not Used (Read Only)
1	FS	State Control in Active Mode 0 = Normal State 1 = Force State (Default)
0	X	Not Used (Read Only)

Control 2 Register (CTRL2)

- When a CTRL2 register value was changed during the measurement, The contents of the change are reflected after measurement.

Address : 1Ch, Control 2 (Write/Read)

Bit	Name	Description
7	AVG	Must be use Default setting. 0 = (Default) ※
6	FCO	Data storage method at FIFO. 0 = Direct (Default) , 1 = Comparison Note: Enabled if FIFO
5	AOR	Choice of method of data Comparison at FIFO. 0 = OR(Default) , 1 = AND Note: Enabled if FIFO
4	FF	FIFO Enable 0 = Disable (Default) , 1 = Enable
3	DEN	Data Ready Function Control Enable 0 = Disabled (Default), 1 = Enabled
2	DRP	DRDY signal active level control 0 = ACTIVE LOW, 1 = ACTIVE HIGH (Default)
1	DTS	Must be use Default setting. 0 = (Default) ※
0	DOS	Must be use Default setting. 0 = (Default) ※

※. The change of this bit is prohibited.

REGISTER DESCRIPTIONS (Continued)

Control 3 Register (CTRL3)

- Bit control at the same time is prohibited.
- Priority of this register is MSB.

Address : 1Dh, Control 3 (Write/Read)

Bit	Name	Description
7	SRST	Soft Reset Control Enable 0 = No Action (Default), 1 = Soft Reset Note: return to zero after soft reset.
6	FRC	Start to Measure in Force State 0 = No Action (Default), 1 = Measurement Start Note: return to zero after measurement.
5	X	Not Used (Read Only)
4	STC	Self Test Control Enable 0 = No Action (Default) 1 = Set parameters to Self Test Response (STB) register. Note: return to zero immediately.
3:2	X	Not Used (Read Only)
1	TCS	Start to Measure Temperature in Active Mode 0 = No Action (Default), 1 = Measurement Start
0	OCL	Start to Calibrate Offset in Active Mode 0 = No Action (Default), 1 = Action

Control 4 Register (CTRL4)

- When a CTRL4 register value was changed during the measurement,
  The contents of the change are reflected after measurement.

Address : 1Eh, Control 4 (Write/Read)

Bit	Name	Description
7:6	MMD	Must be use Default setting. 10 = (Default) ※
5	X	Not Used (Read Only)
4	RS	Set Dynamic range of output data. 0 = 14 bit signed value (-8192 to +8191) (Default) 1 = 15 bit signed value (-16384 to +16383)
3	AS	Must be use Default setting. 0 = (Default) ※
2:0	X	Not Used (Read Only)

※. The change of this bit is prohibited.

REGISTER DESCRIPTIONS (Continued)

Offset Drift Value Register (OFFX, OFFY, OFFZ)

- Data is 14bit integer and 1FFFh (8191d) ～ E000h (-8192d)

Address : 20h, 14 bits X-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFX 7:0	X-axis Offset Drift Value, Signed Integer.

Address : 21h, 14 bits X-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7	X	Not Used (Read Only)
6:0	OFFX 14:8	X-axis Offset Drift Value, Signed Integer.

Address : 22h, 14 bits Y-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFY 7:0	Y-axis Offset Drift Value, Signed Integer.

Address : 23h, 14 bits Y-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7	X	Not Used (Read Only)
6:0	OFFY 14:8	Y-axis Offset Drift Value, Signed Integer.

Address : 24h, 14 bits Z-axis Offset Drift Value LSB (Write/Read)

Bit	Name	Description
7:0	OFFZ 7:0	Z-axis Offset Drift Value, Signed Integer.

Address : 25h, 14 bits Z-axis Offset Drift Value MSB (Write/Read)

Bit	Name	Description
7	X	Not Used (Read Only)
6:0	OFFZ 14:8	Z-axis Offset Drift Value, Signed Integer.

Address : 26h-27h, ITHR : Interrupt Threshold (Write/Read)

Bit	Name	Description
15:14	X	Not Used (Read Only)
13:0	ITHR	Comparison value Note: Enabled if CTRL2.FCO

Temperature Data Register (TEMP)

- Temperature measurement is performed by setting register command (CNTL3 : bit TCS) when in the active mode
- Result is stored to temperature register (TEMP）
-Sensor output value are compensated with the temperature value stored TEMP register.

Address : 31h, Temperature Data (Read Only)

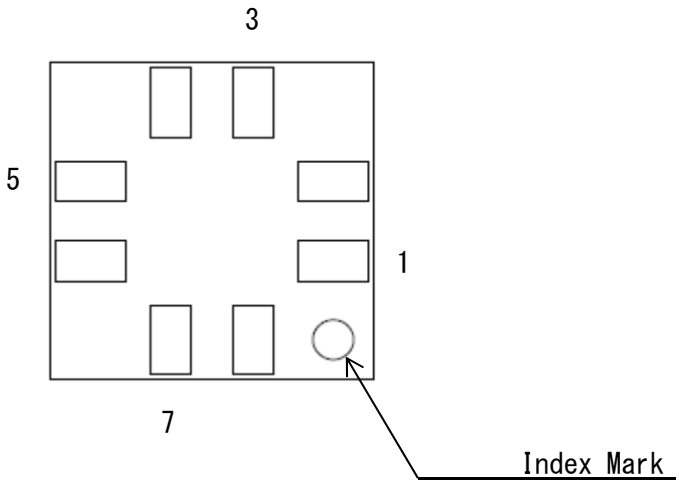
Bit	Name	Description
7:0	TEMP7:0	Temperature Data, Signed Integer. LSB = 1℃ 1000 0000 = -128℃ 0000 0000 = 0℃ 0111 1111 = 127℃

PIN CONFIGURATION

Pin	Symbol	Type	Description	Connect Pin
1	VSS	Power	Ground pin.	GND
2	AVDD	Power	Analog power supply pin.	AVDD
3	DVDD	Power	Digital power supply pin.	DVDD
4	DRDY	Output, CMOS	Data Ready output pin.	DRDY / NC
5	TEST0	Intput, CMOS	Test pin	NC / GND
6	TEST1	Intput, CMOS	Test pin	NC *1
7	SCL	Input, CMOS	Control data clock	SCL
8	SDA	Input / Output CMOS / Open drain	Control data input/output pin.	SDA

Notes - Test pin uses only the Manufacturing test.

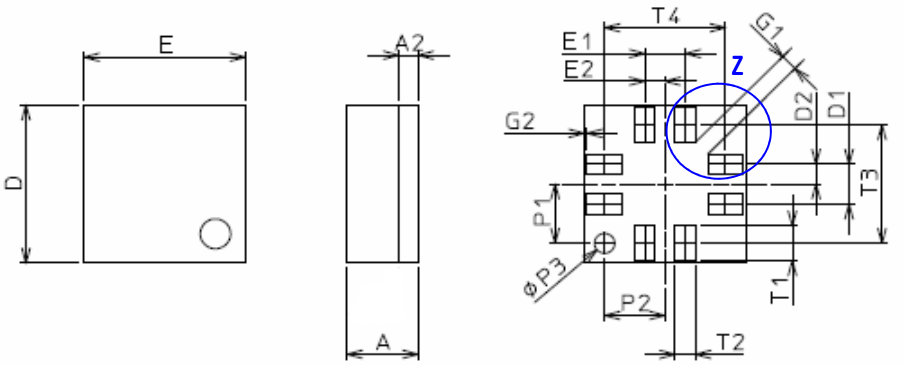
Top view



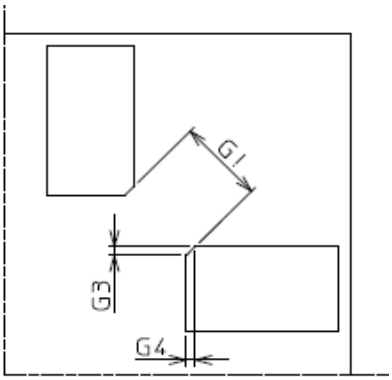
PACKAGE DIMENSIONS

Dimension in millimeters				Dimension in millimeters			
Ref	Min.	Nom.	Max.	Ref	Min.	Nom.	Max.
D	1.5	1.6	1.7	T1	---	0.35	---
E	1.5	1.6	1.7	T2	---	0.20	---
D1	0.37	0.40	0.43	T3	---	1.19	---
D2	0.17	0.20	0.23	T4	---	1.19	---
E1	0.37	0.40	0.43	P1	0.57	0.60	0.63
E2	0.17	0.20	0.23	P2	0.57	0.60	0.63
A	0.60	0.65	0.70	P3	0.07	0.10	0.13
A2	0.14	0.19	0.24	G1	0.2	---	---
				G2	0	---	0.1
				G3	---	0.067	---
				G4	---	0.067	---

Top view Side view Bottom view

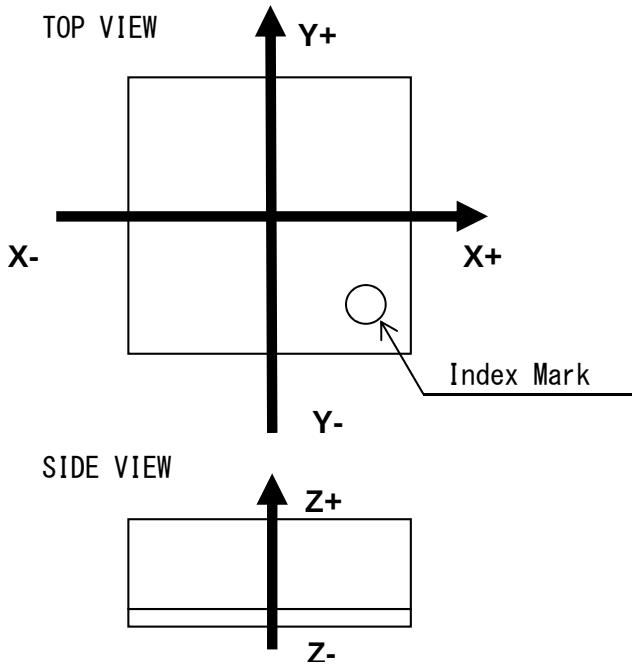


Z part enlarged picture

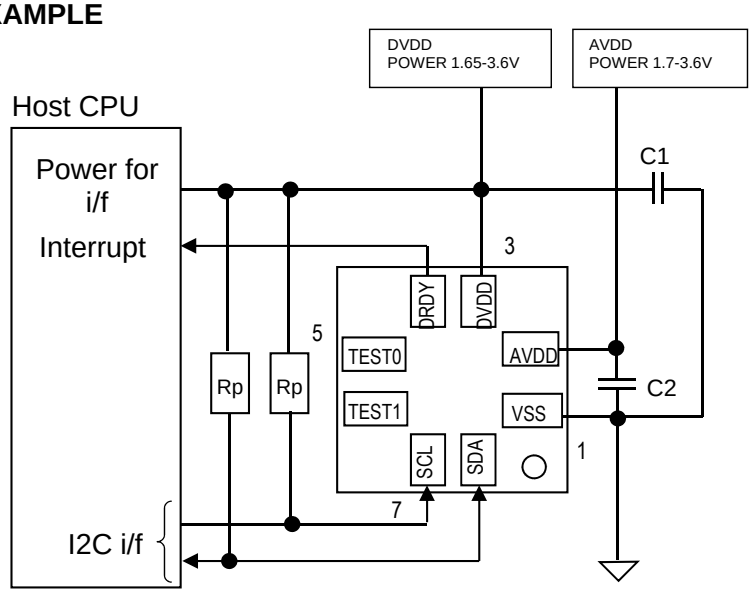


PACKAGE DIRECTIONS

- X, Y, Z presents measurement directions of 3 axis sensor.
- Output value of each axis is positive when turned toward magnetic north.



CONNECTION EXAMPLE

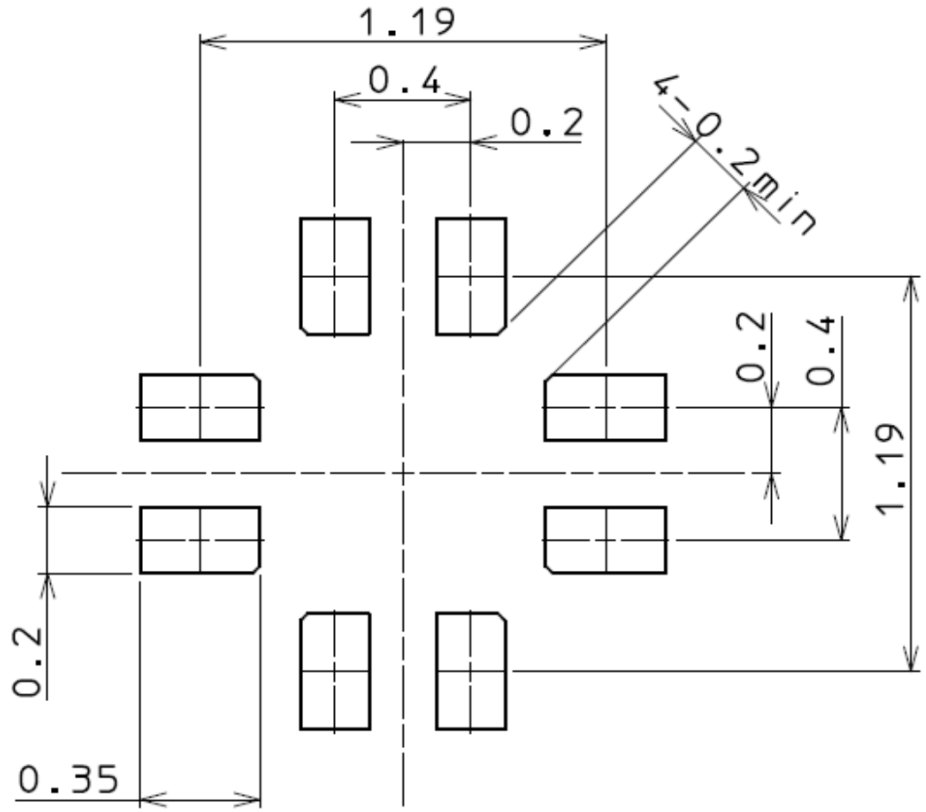


Connection ie at I2C Interface

Notes

- Capaciter recommendation : C1, C2 = 0.1μF

RECOMMENDED LAND PATTERN



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History of revision

Revision	Date	Page	Note
1.0	16.Mar.2012		First edition
1.1	24.Apr.2012	P.2,3,7,26	DVDD Range 2.0-3.6 to 1.8-3.6 [V]
1.2	15.Jun.2012	P.3,10,18 20,21,22	Show TBD value
1.3	18.Jun.2012	P.25	Addition of dimension "G1".
1.4	21.Jun.2012	P.25, 28	Change PAD Size/Layout
1.5	10.Jul,2012	P.10	tof, Vhdv, Vhav Min. value change
1.6	9.Aug,2012	P.10	Vhav Min. value change
1.7	25.Oct.2012	P.20 P.25	Add 15 bit output value Deleate A1 spec.
1.8	14.Dec.2012	P.20	Add Definition on bit7 (bit6) of MSB
1.9	7.Mar.2013	P.3 P.10	Change Measurement Range : ±2.4 to ±7.2 [mT] Supply voltage sequence AVDD ON : 1.75 to 1.53 [V]
2.0	7.Jun,2013	P.13	Add read Margin
2.1	5.Jul.2013	P.2/3/7 P23	AVDD min. 1.8 V -> 1.7 V Correction of errors
2.4	9.Apr,2015	P.2,5,10,11 P.20,22,23 P.25 P.29	Add FIFO AVDD min. 1.8 V -> 1.7 V
2.5	31.Aug,2016	All	ALPS Confidential -> Confidential