MULTI-LAYER CERAMIC CAPACITORS SPECIFICATION

Customer: AVX/KYOCERA ASIA

(RECEIPT.)

Please return one of the specification booklets With your sign of approval.

(Please discard older version of the specification whenever you receive latest version of it.)

Capacitor Division
Electronic Components Group
Kyocera Corporation

No	Date	Contents	PREPD.	CHKD.	APPD.
01	2005.08.	NEW			

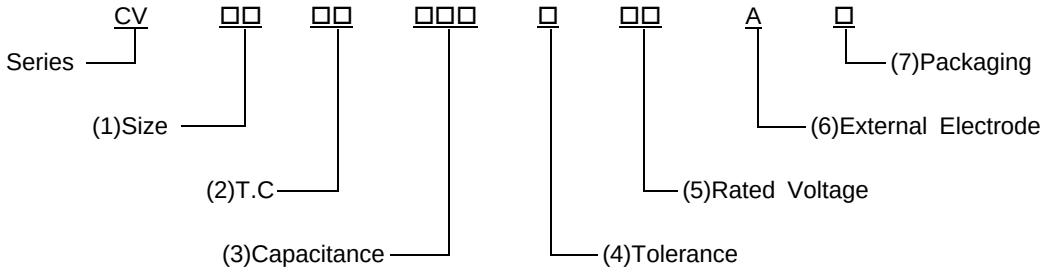
[Part NO.]

Characteristic	K/C Supplier Part NO	Thickness(mm)	Remarks
X5R	CV105X5R106M06AT	0.8±0.2	

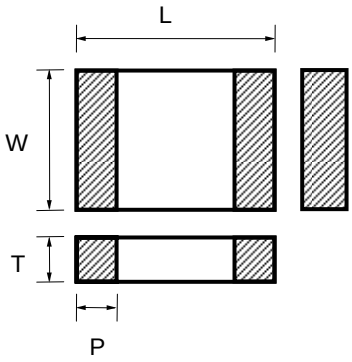
1.Scope:

This specification sheet shall be applied to multilayer ceramic chip capacitors;Kyocera CV series.

2.Nomenclature



(1)External Dimensions(Size)



(unit:mm)

Type	L	W	T	P
105	1.6±0.2	0.8±0.2	*	0.2~0.6

*:Refer to Part No.

(2)Temperature Characteristics

Characteristics	Applied voltage	Change in capacitance	Operating temperature range	Reference
X5R	No applied voltage	Within +/-15%	-55°C~+85°C	25°C

(3)Capacitance Value

Capacitance is indentified by three numbers and a letter (see example as follows). The first and second digits indicate the first two significant figures,and the final digit is a base 10 logarithmic multiplier in picofarads.

106(10.0uF)

(4) Tolerance

Code	M
Tolerance	±20%

(5) Rated Voltage

Code	06
Voltage	6.3VDC

(6) Termination (External Electrode)

A:NICKEL BARRIER

(7) Packaging Configuration

Code	Packaging Configuration	Applying Size
T	Taping(4mm Pitch. ϕ180 Reel)	Refer to Taping specification

3.Operating temperature range

Refer to Item 2-(2)

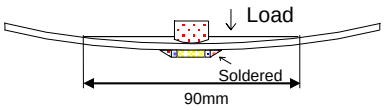
4.Specifications and Test Methods

(Table 1-1)

Item		Specification X5R	Measuring Conditions
Temperature Characteristics		Refer to Item 2-(2)	High Temperature Treetment (Table 2) Measuring frequency 1.0kHz±10% Measuring voltage 1.0±0.2Vrms
Capacitance		Within specified tolerance value	
tanδ		Less than 12.5%	
(*1)Insulation Resistance		10000MΩ or 500MΩ·μF min, whichever is less	Measure after charging with the rated voltage within 2minutes at room conditions.
(*1)Dielectric Strength		No problem observed	Applying 1.25 times of the rated voltage for 1 to 5 seconds.
Appearance		No serious defect	Under Microscope ×10
End Termination adherence		No evidence of peeling on the end termination	After soldering chip capacitors on glass epoxy boards and applying 5N(0.5Kgf) as shown by the arrow mark in the sketch peeling or any sign of peeling should not be found on end terminations. (Refer to Fig.1)
Resistance to Vibration	Appearance	No serious defect	High Temperature Treatment (Table 2) Vibration frequency:10 to 55 (Hz) Swing width:1.5mm Sweep:10→55→10 Hz/1min x,y,z axis 2 hours/each Total 6 hours (Refer to Fig.2)
	Capacitance Variation	Within specified tolerance value	
	tanδ	Satisfies initial specified value	
Resistance to Solder Leaching	Appearance	No serious defect	High Temperature Treatment (Table 2) After dipped molten solder, at 260±5°C for 10±0.5 seconds and kept at room conditions for 48±4 hours, measure and chech the specifications. *Pre-heat before immersion 1st: 80°C to 100°C for 120sec. 2st:150°C to 200°C for 120sec.
	Capacitance Variation	Within ±7.5%	
	tanδ	Satisfies initial specified value	
	(*1)Insulation Resistance	10000MΩ or 500MΩ·μF min, whichever is less	
	(*1)Dielectric Strength	Resist without problem.	
Solderability		Coverage ≥ 90% Each termination end	<Sn62 Solder>235±5°C 2±0.5Sec <Sn-3Ag-0.5Cu>245±5°C 3±0.5Sec

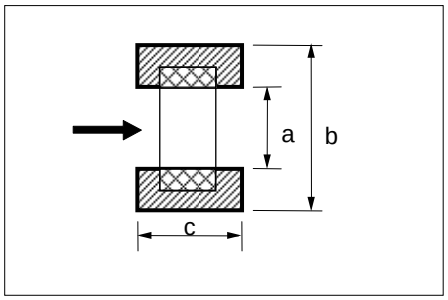
(*1)Insulation Resistance/Dielectric Strength;Charging or discharging current for these tests Is limited under 50mA.

(Table 1-2)

Item		Specification X5R	Measuring Conditions
Temperature Cycling	Appearance	No serious defect	High Temperature Treatment (Table 2) 〈Cycle〉 Room temperature (3 minutes)→ Lowest operating temperature (30 minutes)→Room temperature (3 minutes)→Highest operating temperature (30 minutes). After 5 cycles of the above, Keep for after 48±4 hours at room Conditions then measure. (Refer to Fig.2)
	Capacitance Variation	Within ±7.5%	
	tanδ	Satisfies initial specified value	
	(*1)Insulation Resistance	10000MΩ or 500MΩ·μF min, whichever is less	
	(*1)Dielectric Strength	Resist without problem	
Humidity	Appearance	No serious defect	High Temperature Treatment (Table 2) After Exposed to high temperature, 40℃±2℃ and humidity 90 to 95% RH, for 500+24/-0 hours and keep at room conditions for 48±4 hours then measure and check the specification limits.
	Capacitance Variation	Within ±12.5%	
	tanδ	Less than 2.0 times of the initial value	
	(*1)Insulation Resistance	1000MΩ or 50MΩ·μF min, whichever is less	
High Temperature Life Test	Appearance	No serious defect	Voltage Treatment (Table 2) After appling rated voltage at the highest operation Temperature for 1000+48/−0 hours, and kept at room conditions for 48±4 hours. Measure and check the specifications at room conditions.
	Capacitance Variation	Within ±12.5%	
	Tanδ	Less than 2.0 times of the initial value	
	(*1)Insulation Resistance	1000MΩ or 50MΩ·μF min, whichever is less	
Bending Strength		No mechanical damage	Apply the load as shown;The glass epoxy board is bent up 1mm in 10 sec.  (Refer to Fig.3)

(Table 2)

Initial Treatment	High Temperature Treatment	Keep chip capacitor at 150°C +0/-10°C for one hour,Then leave chip capacitor at room temperature and normal humidity for 48±4 hours.
	Voltage Treatment	Pretreat capacitor for 1 hour at the same condition of the load test,Then leave them at room condition for 48±4 hrs before beginning the Load test.



Unit:mm

type	a	b	C
105	1.0	3.0	1.2

glass epoxy board

Fig.1 End termination adherence (from side).

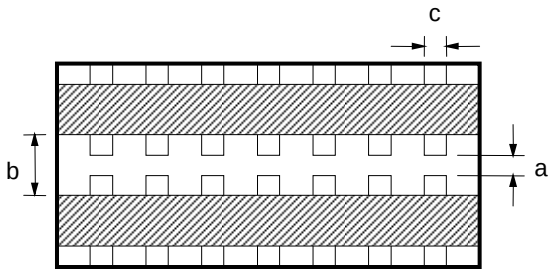


Fig.2 Resistance to vibration, temperature cycling.

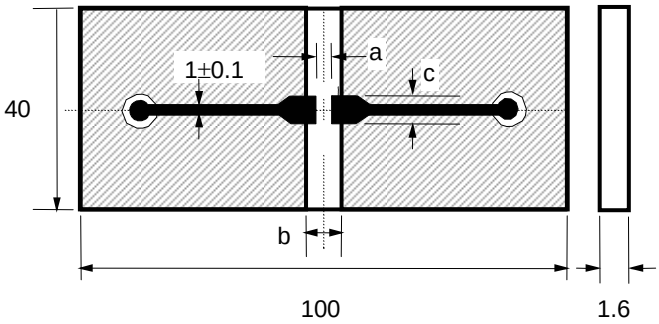
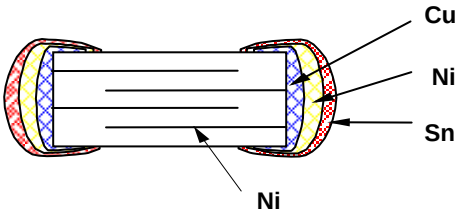


Fig.3 Bend strength.

[Structure]

High Dielectric Constant



[Production facility]

Kagoshima kokubu plant
Kagoshima sendai plant
Shanghai kyocera electronics

[Working Voltage]

4.0V Max.

Taping Specification

1.Application

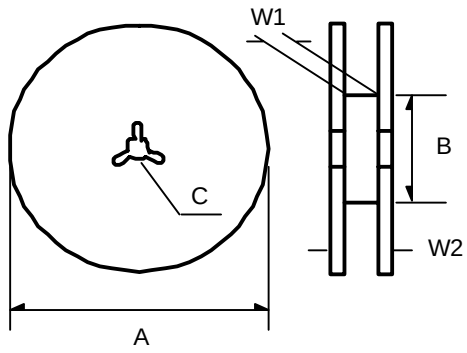
This specification applies to carrier tape of Kyocera multi-layer ceramic chip capacitor.

2.Packing unit

type	thickness (unit:mm)	material of carrier tape		width of carrier tape		ϕ180 reel quantity per reel
		paper	Plastic	8mm	12mm	
105	0.8±0.2	O	-	O	-	3000

3.Shape and dimentions

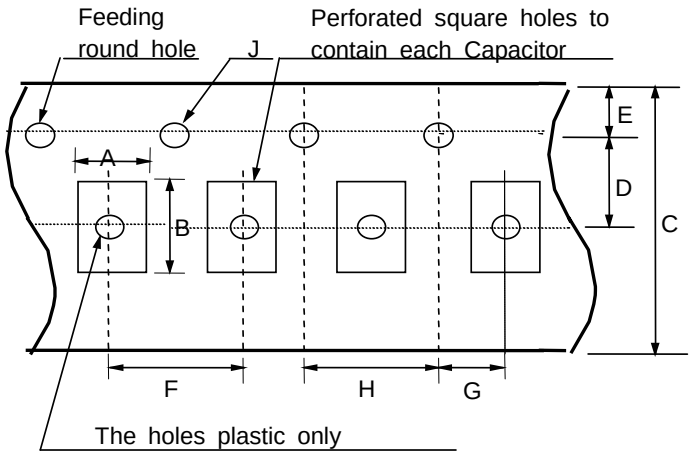
(1)Reel

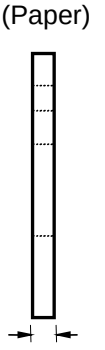


Code	A	B	C
Dimension	ϕ180+0/-2.0	ϕ60min	ϕ13.0±0.5
Code	W1	W2	
Dimension	10.0±1.5	16.5max	

Plastic real Is used

(2)Carrier Tape





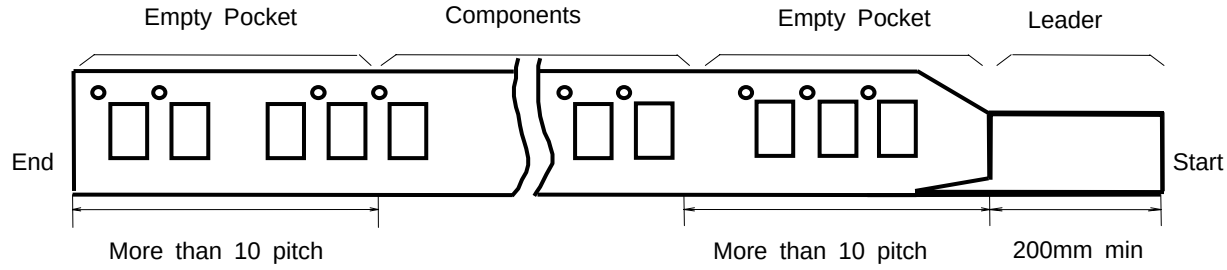
(unit:mm)

Code / Tolerance / Type	A	B	C	D	E	F	G	H	J
	±0.2	±0.2	±0.3	±0.05	±0.1	±0.1	±0.05	±0.1	+0.1/-0
105	1.1	1.9	8.0	3.5	1.75	4.0	2.0	4.0	ϕ1.5

4.Packing method

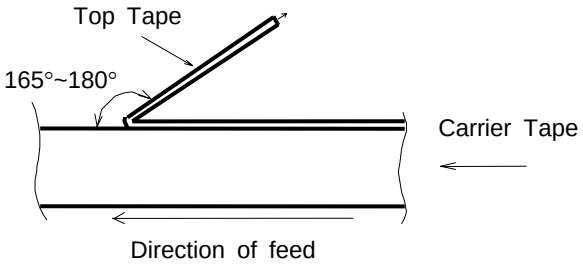
(1)Details of leader and trailer

①The tape will have a empty pocket at the leader and trailer of carrier tape.
②The tape end will not be stucked by glue in order to make it easier to peel off from reel.
③The feeding round hole will be on the right side against t leading direction.



(2)Heat pressure tape

①Peeling strength to be 10~70g when peeling off the top tape by following method.
②When peeling top tape off, the glue will be stuck to the top tape side.
③Chip capacitor will not stuck on heat pressure tape and will be free in the cavity.



The peel-off angle:165~180 degree against the surface of carrier tape.
The peel-off speed:300mm/min.

(3)Carrier tape

①Chip will not fall off from carrier tape or carrier tape will not be damaged by bending than within aradius of 15mm.
②The chip are inserted continuously without any empty pocket.
③Chip will not be mis-mounted because of too big clearance between components and cavity. Also the waste of carrier tape will not fill a nozzle hole of mouting machine.

5.Indication and packing

①There will be following indication on one side of the reel: “PART NUMBER”,”LOT NUMBER”, “QUANTITY”,”DATE OF MANUFACTURE”,”CUSTOMER’S NAME”
②There will be following indication on the reel box: “PART NUMBER”,”LOT NUMBER”, ”QUANTITY OF REEL”,”DATE OF MANUFACTURE”,”CUSTOMER’S NAME”
③We adequately pack the box to prevent chip capacitor from any mechanical damage during transportation.