General Description

The BL24C02P is 2-Kbit I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 256 × 8bits, which is organized in 8 bytes per page. BL24C02P provides the following devices for different application.

Device Selection Table

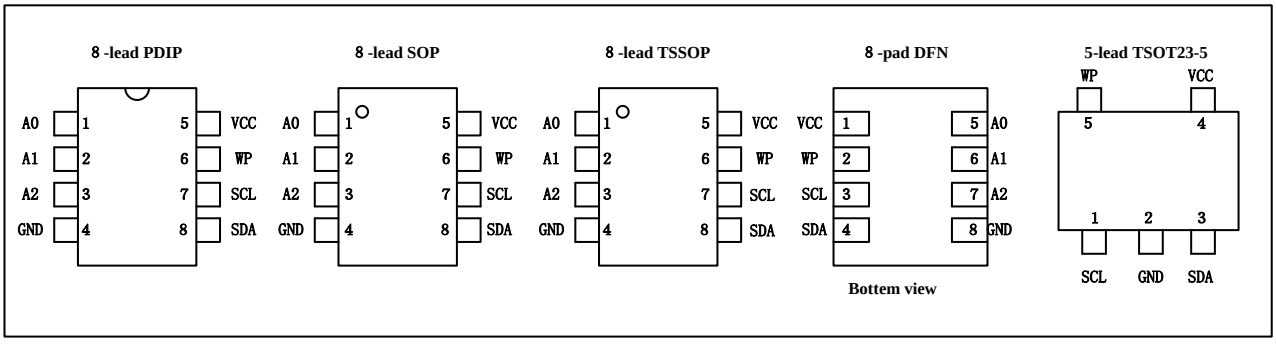
Device Name	Voltage Range	Temp. Range	Max. Clock Frequency
BL24C02P	1.7V~5.5V	-40°C ~ 85°C	1MHz[1]

Note 1: 400 kHz for VCC < 2.5V

Features

- Single Supply Voltage and High Speed
  - Minimum operating voltage down to 1.5V
  - 1 MHz clock from 2.5V to 5.5V
  - 400kHz clock from 1.7V to 2.5V
- Low power CMOS technology
  - Read current 0.6mA, maximum
  - Write current 2.0mA, maximum
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - Endurance: > 1 Million Write Cycles
  - Data Retention: > 100 Years
- Latch-up Capability: +/- 200mA
- Package: PDIP, SOP, TSSOP, DFN, TSOT23-5

1. Pin Configuration



Pin Definition

Pin	Name	Type	Description
1	A0	I/O	Slave Address Setting
2	A1	Input	Slave Address Setting
3	A2	Input	Slave Address Setting
4	GND	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WP	Input	Write Protect, Low Enable Write
8	VCC	Power	Power

Table 1-1 Pin Definition

Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-Ored with any number of other open-drain or open-collector devices.

Device Addresses (A2, A1, A0): The A2, A1 and A0 pins are device address inputs. Typically, the A2, A1 and A0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND.

Write PROTECT (WP): The Write Protect input, when WP is connected directly to VCC, all write operations to the memory are inhibited. When connected to GND, allows normal write operations. If the pin is left floating, the WP pin will be internally pulled down to GND.

2. Block Diagram

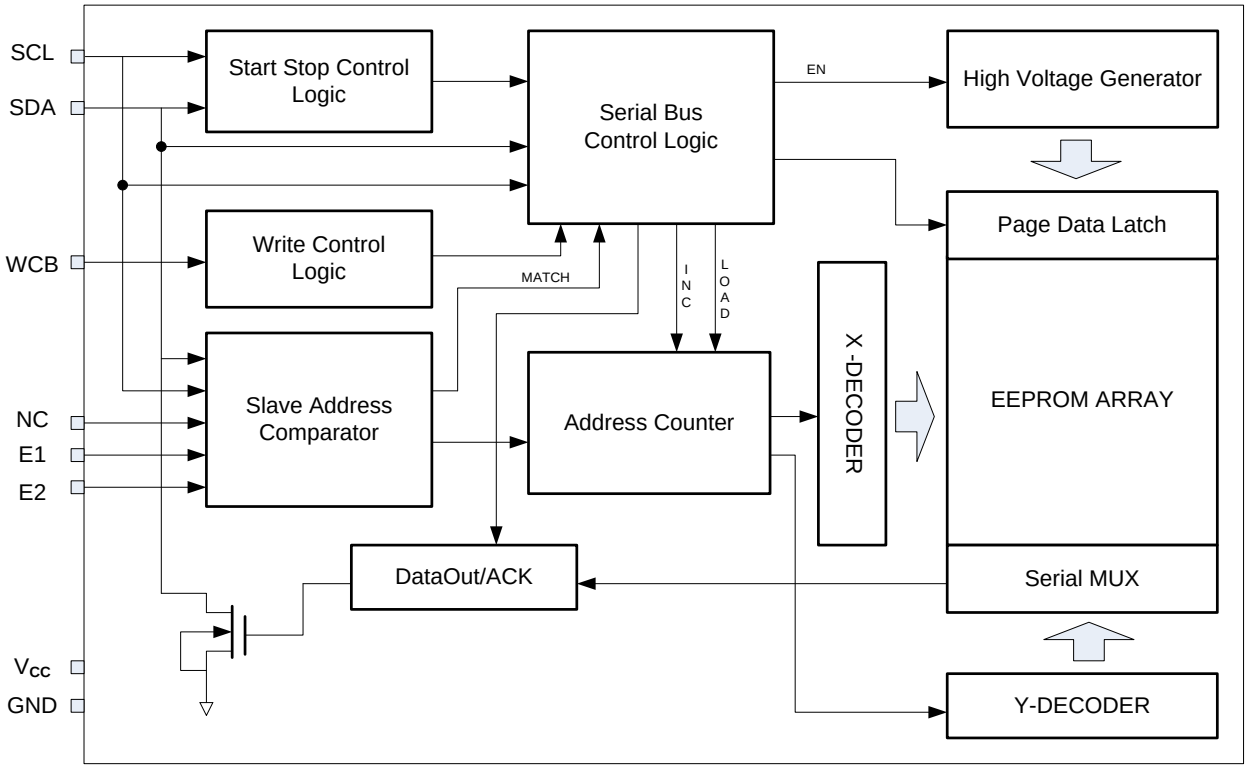


Figure 2-1 Block Diagram

3. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

- Storage Temperature .....-65°C to +150°C
- Operation Temperature .....-40°C to +85°C
- Maximum Operation Voltage..... 6.25V
- Voltage on Any Pin with Respect to Ground .....-1.0V to (Vcc+1.0)V
- DC Output Current 5.0mA

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3-1 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$=GND
C_{IN}	Input Capacitance (A0, A1,A2,WP,SCL)	6	pF	V_{IN}=GND

Note: [1] Test Conditions: TA = 25°C, F = 1MHz, Vcc = 5.0V

Table 3-2 DC Characteristics (Unless otherwise specified, VCC = 1.7V to 5.5V, TA = –40°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	BL24C02P
Isb	Standby Current	-	-	1.0	uA	Vcc = 3.3V, T_A = 85°C
		-	-	3.0	uA	Vcc = 5.5V, T_A = 85°C
I_{CC1}	Supply Current	-	0.3	0.6	mA	Vcc=5.5V, Read at 400Khz
I_{CC2}	Supply Current	-	1.0	1.6	mA	Vcc=5.5V Write at 400Khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = V_{CC} or GND
V_{IL}	Input Low Level	–0.6	-	0.3V_{CC}	V	
V_{IH}	Input High Level	0.7V_{CC}	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC} = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5mA
V_{OL2}	Output Low Level V_{CC} = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1mA

Table 3-3 AC Characteristics

(Unless otherwise specified, VCC=1.7V to 5.5V, TA=- 40°C to 85°C, CL=100pF, Test Conditions are listed in Notes [2])

Symbol	Parameter	$1.7 \le V_{CC} < 2.5$			$2.5 \le V_{CC} \le 5.5$			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WP}$	WP pin Setup Time	1.2	-	-	0.6	-	-	μs
$t_{HD.WP}$	WP pin Hold Time	1.2	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- RL (connects to VCC): 1.3k (2.5V, 5.5V), 10k (1.7V)
- Input pulse voltages: 0.3 VCC to 0.7 VCC
- Input rise and fall times: ≤50ns
- Input and output timing reference voltages: 0.5VCC

Table 3-4 Reliability Characteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET	Data Retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

Figure 3-1 Bus Timing

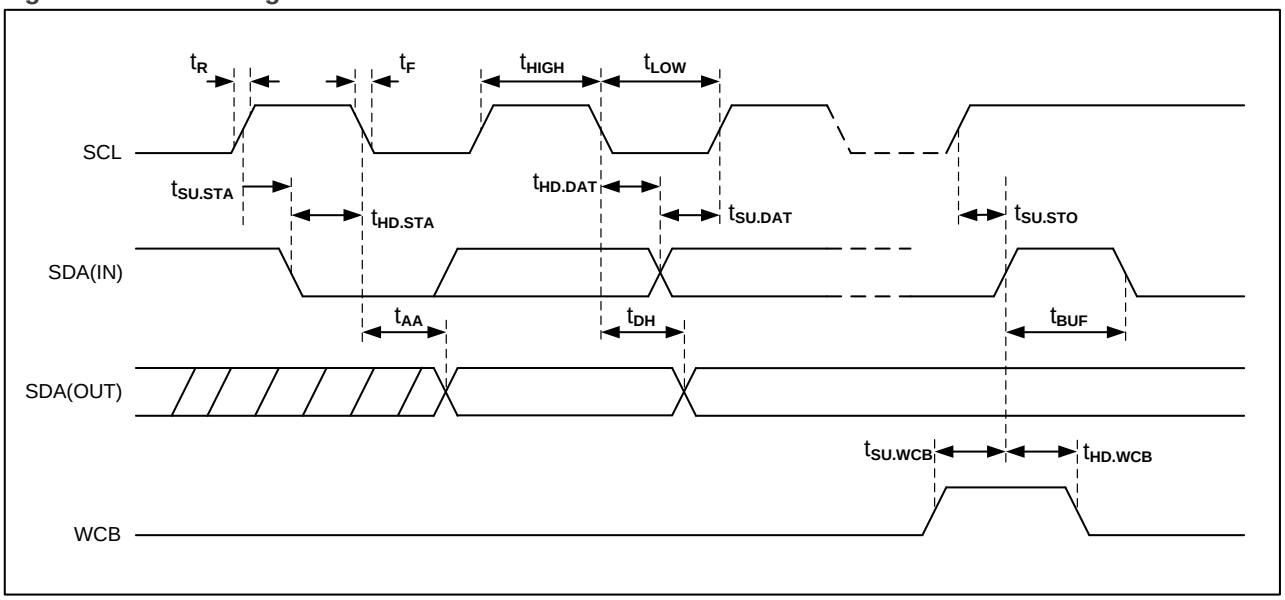
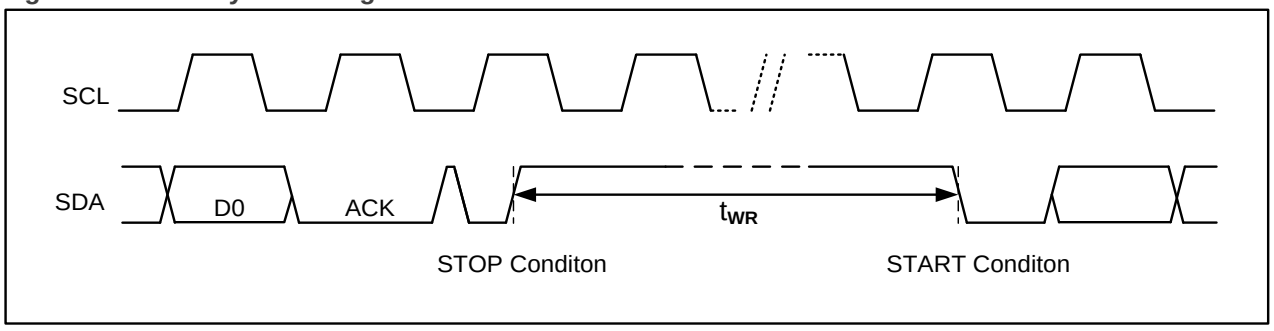


Figure 3-2 Write Cycle Timing



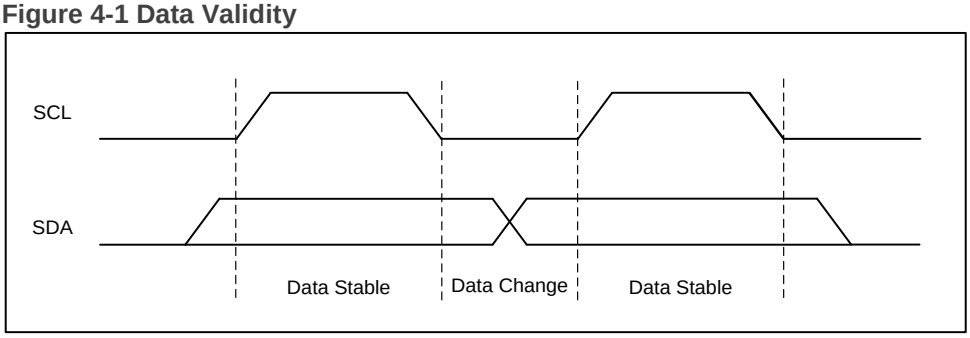
Note: [1] The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Figure 4-1 Data Validity



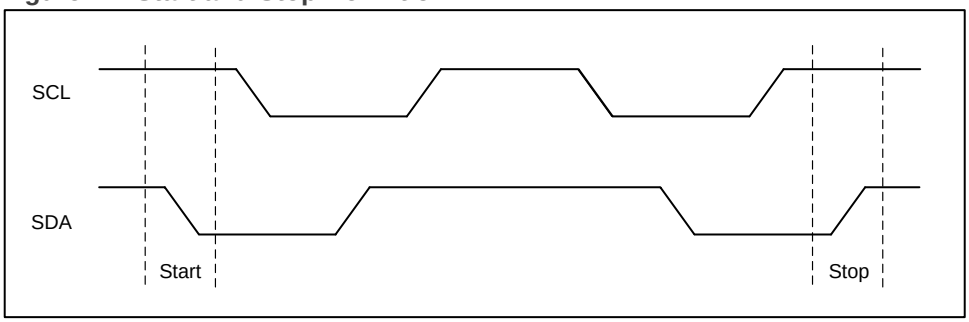
4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the BL24C02P in a standby power mode (see Figure 4-2).

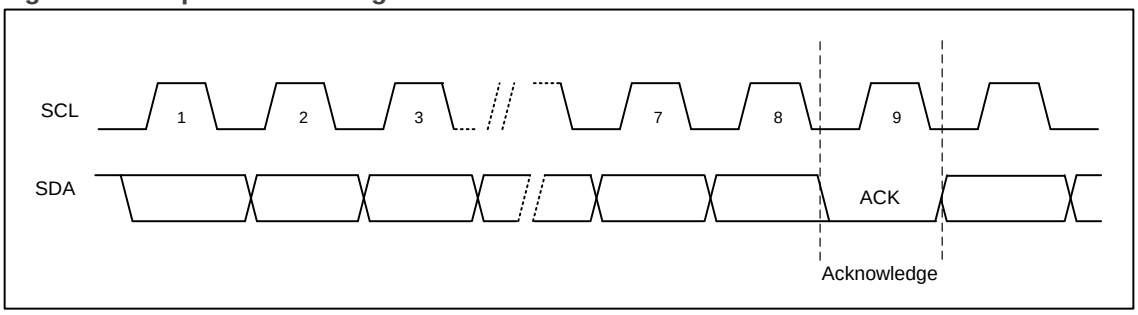
Figure 4-2 Start and Stop Definition



4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the BL24C02P in 8-bit words. The BL24C02P sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 4-3 Output Acknowledge



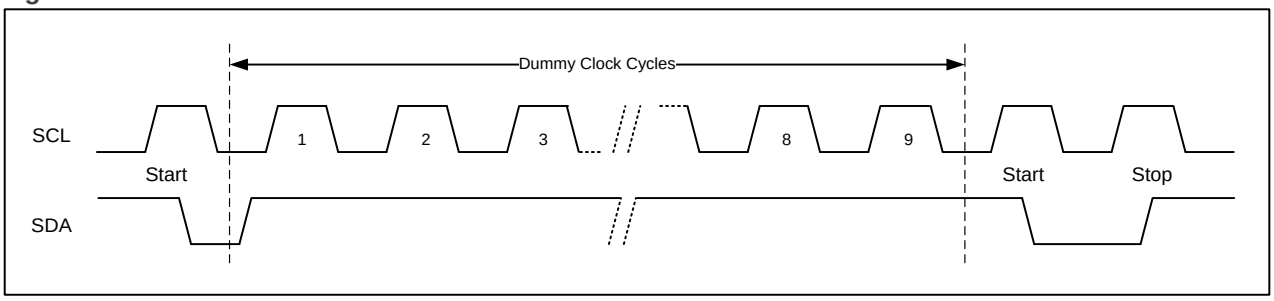
4.5 Standby Mode

The BL24C02P features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.7 Device Addressing

The BL24C02P requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 4-1 Device Address

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	1	0	1	0	A2	A1	A0	R/W

Table 4-2 Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	B7	B6	B5	B4	B3	B2	B1	B0

The A2, A1 and A0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

4.8 Data Security

BL24C02P has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at Vcc.

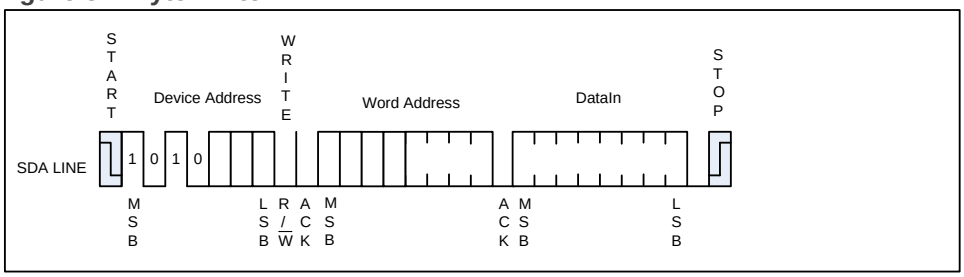
5. Instructions

5.1 Write Operations

5.1.1 BYTE WRITE

A write operation requires a 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the BL24C02P will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the BL24C02P will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the BL24C02P enters an internally timed write cycle, all inputs are disabled during this write cycle and the BL24C02P will not respond until the write is complete (see Figure 5-1).

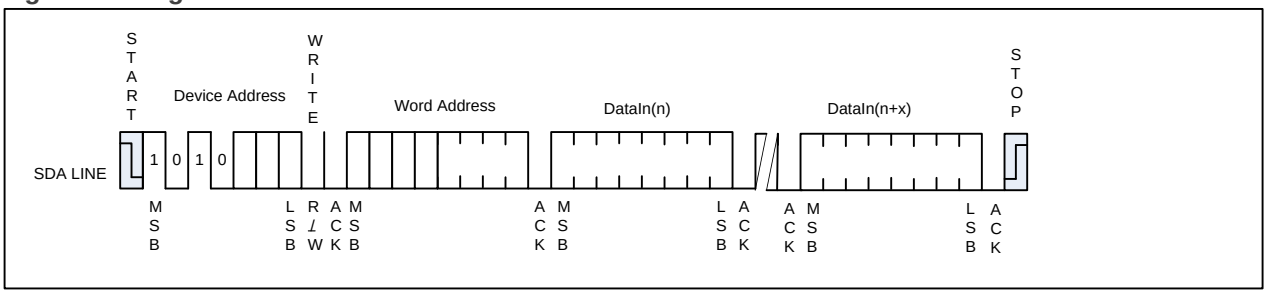
Figure 5-1 Byte Write



5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the BL24C02P acknowledges receipt of the first data word, the master can transmit more data words. The BL24C02P will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 5-2 Page Write



The lower three bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the BL24C02P, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the BL24C02P inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the BL24C02P respond with a "0", allowing the read or write sequence to continue.

5.2 Read Operations

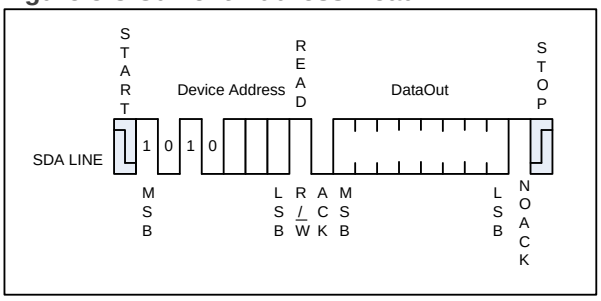
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the BL24C02P, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 5-3).

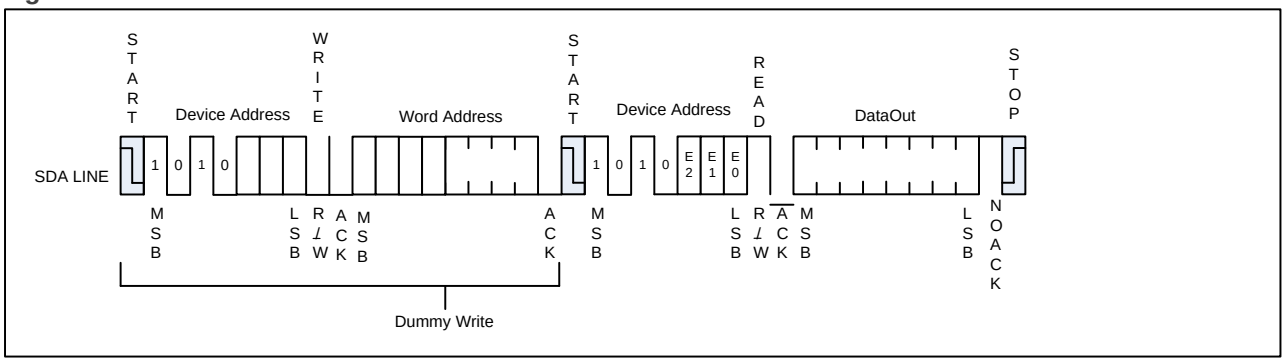
Figure 5-3 Current Address Read



5.2.2 Random Read

A Random Read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the BL24C02P, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The BL24C02P acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-4).

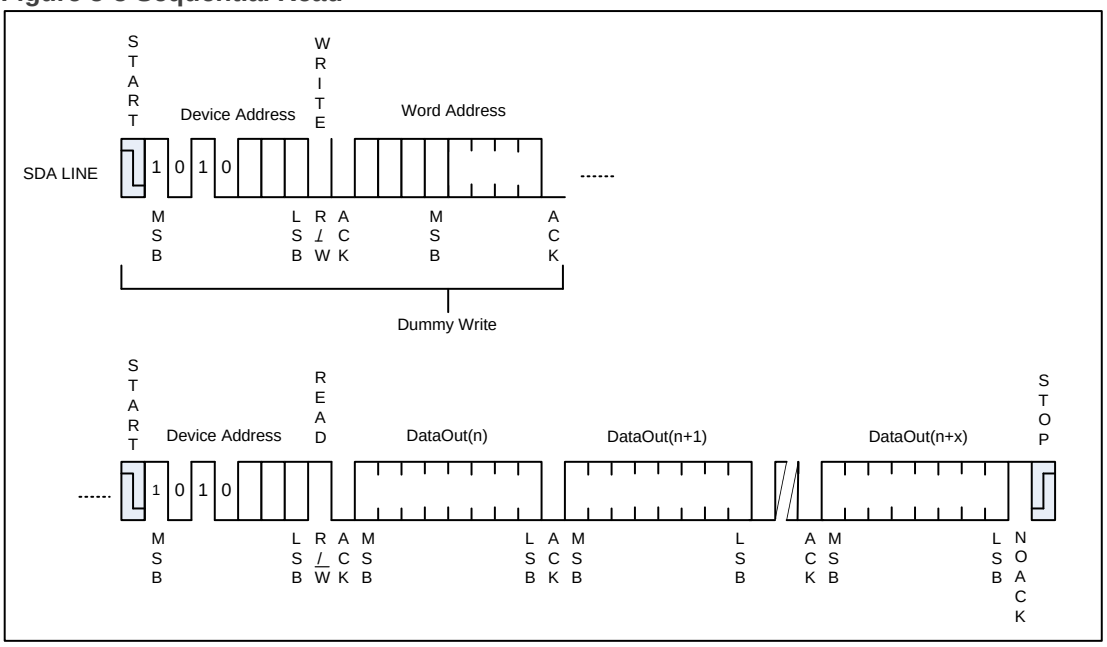
Figure 5-4 Random Read



5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the BL24C02P receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-5)

Figure 5-5 Sequential Read



6. Package Information

8-LEAD PDIP

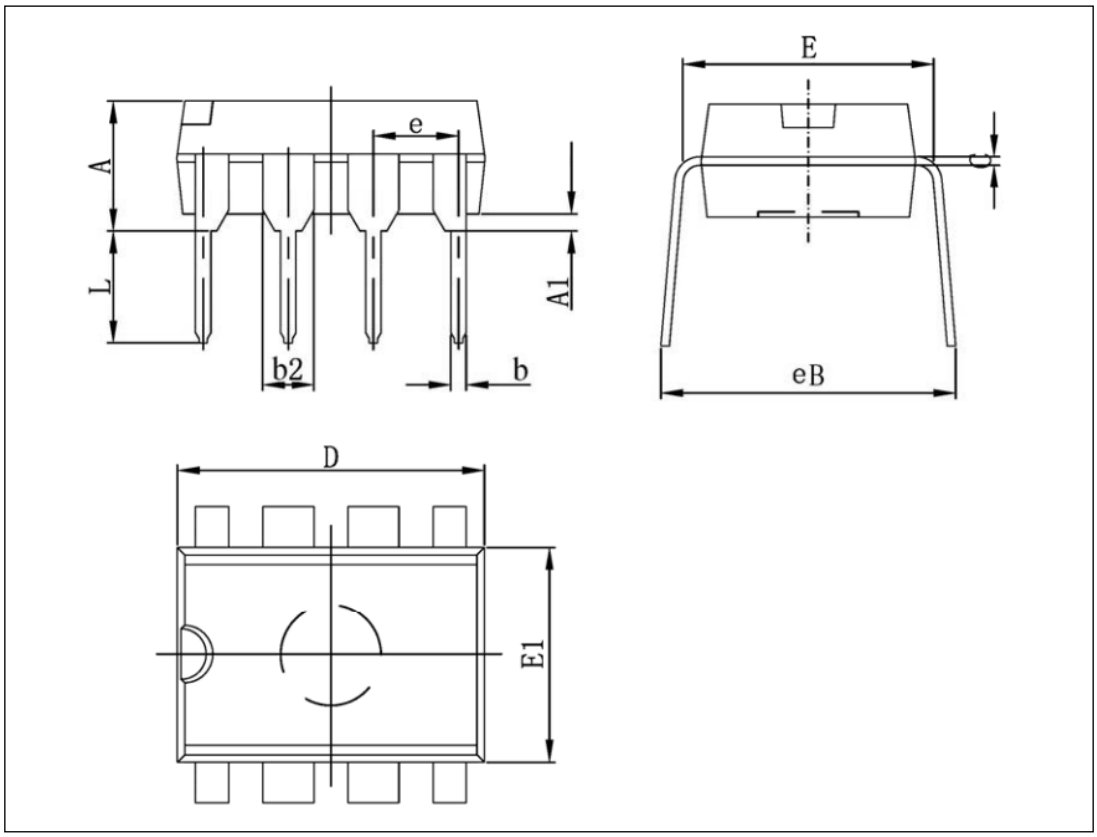


Table 7-1 8-lead PDIP package mechanical data

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	3.71	4.31	0.146	0.17
A1	0.51	0.02		
b	0.38	0.57	0.015	0.022
b2	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.36	0.008	0.014
D	9	9.4	0.354	0.37
E1	6.2	6.6	0.244	0.26
E	7.32	7.92	0.288	0.312
e	2.54(BSC)		0.100 (BSC)	
L	3	3.6	0.118	0.142
eB	8.4	9	0.331	0.354

8-LEAD SOP

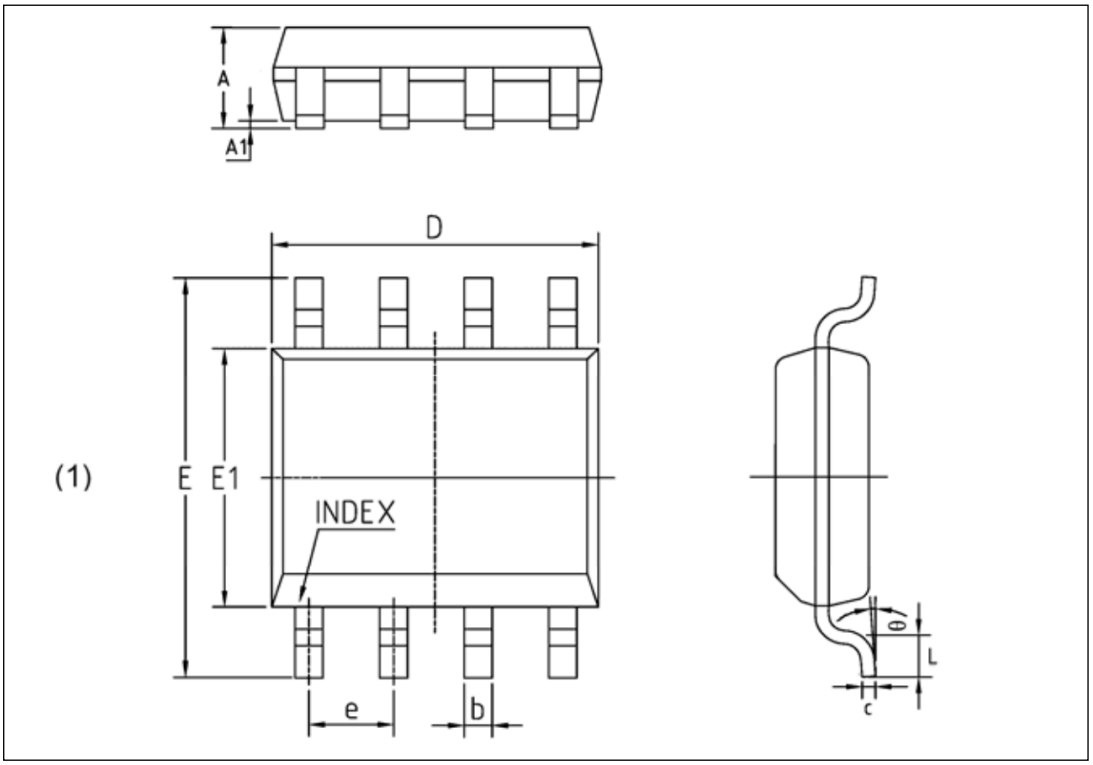


Table 7-2 8-lead SOP package mechanical data

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.53	0.069
A1	0.1	0.25	0.004	0.01
b	0.33	0.51	0.013	0.02
c	0.17	0.25	0.006	0.01
D	4.7	5.1	0.185	0.2
E1	3.8	4	0.15	0.157
E	5.8	6.2	0.228	0.244
e	1.270 (BSC)		0.050(BSC)	
L	0.4	1.27	0.016	0.05
θ	0°	8°	0°	8°

8-LEAD TSSOP

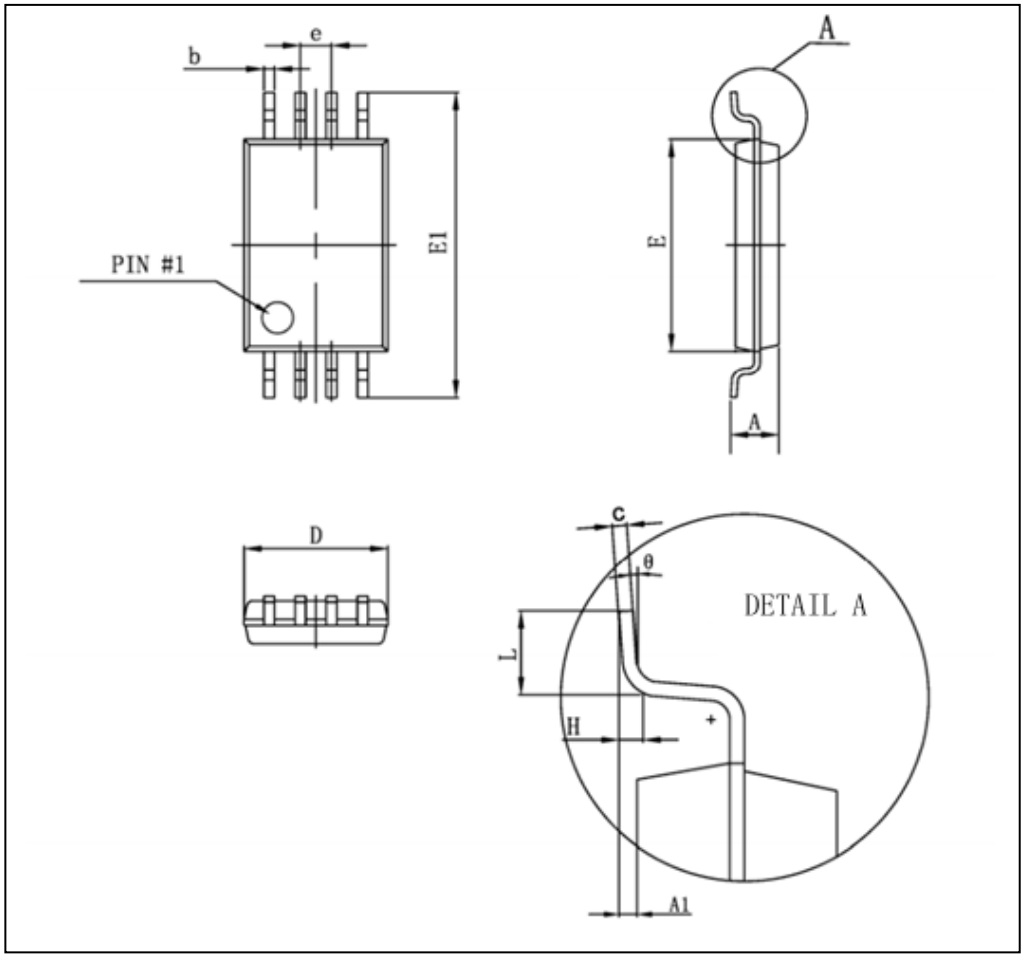


Table 7-3 8-lead TSSOP package mechanical data

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	2.9	3.1	0.114	0.122
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.25	6.55	0.246	0.258
A		1.2		0.047
A1	0.05	0.15	0.002	0.006
e	0.65 (BSC)		0.026(BSC)	
L	0.5	0.7	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

8-LEAD DFN

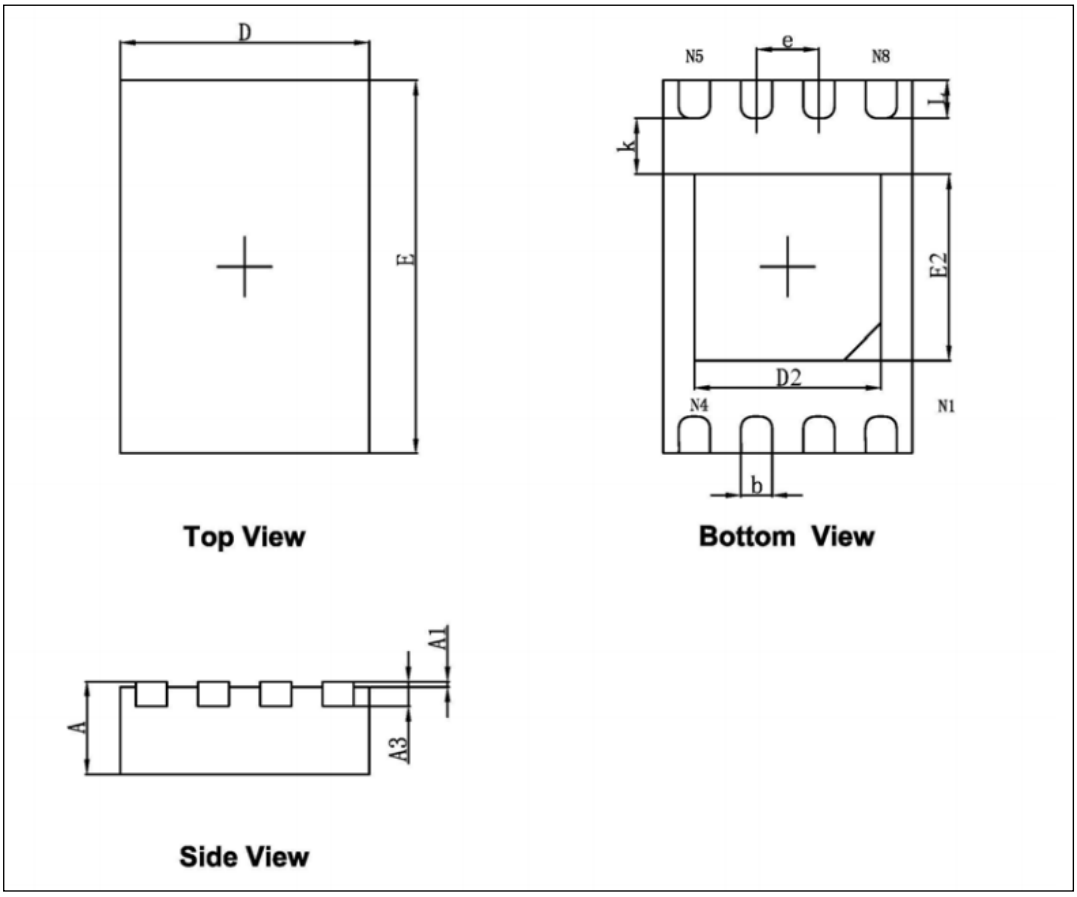


Table 7-4 8-lead DFN package mechanical data

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0	0.05	0	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D2	1.4	1.6	0.055	0.063
E2	1.4	1.6	0.055	0.063
k	0.200MIN.		0.008MIN.	
b	0.2	0.3	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

TSOT23-5

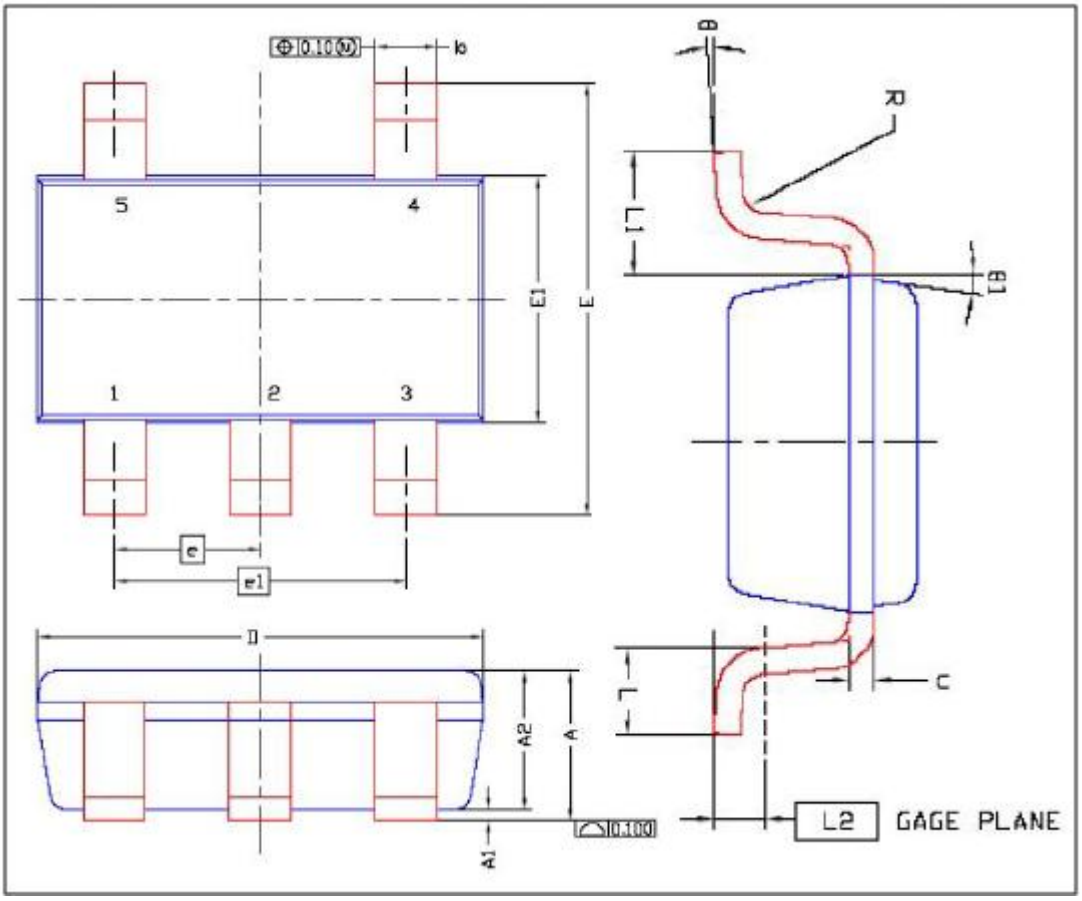


Table 7-5 5-lead TSOT23-5 package mechanical data

Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.80	0.95	1.00	0.0315	0.0374	0.0394
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.875	0.90	0.0276	0.0344	0.0354
b	0.35	0.40	0.50	0.014	0.016	0.020
c	0.10	0.127	0.20	0.004	0.005	0.008
D		2.90BSC			0.114BSC	
E		2.80BSC			0.110BSC	
E1		1.60BSC			0.063BSC	
e		0.95BSC			0.037BSC	
e1		1.90BSC			0.075BSC	
L	0.30	0.40	0.60	0.0118	0.0157	0.024
L1		0.60REF			0.024REF	
L2		0.254BSC			0.010BSC	
R	0.10	---	---	0.004	---	---
θ	0°	4°	8°	0°	4°	8°
θ1		7°NOM			7°NOM	

7. Ordering Information

BL24C02P 1 2 3

Code	Description
1	Package type PA: SOP-8L SF: TSSOP-8L DA: PDIP-8L NO: UDFN-8L TC: SOT23-5L RR: TSOT23-5L MA: M2.2 MB: M3.2 CS: WLCSP-4
2	Packing type R: Tape and Reel T: Tube
3	Feature S: Standard (default, Pb Free RoHS Std.) C: Green (Halogen Free)