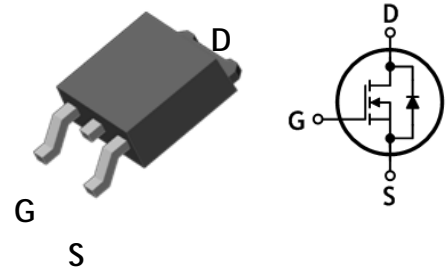


Power Switching Application

Features

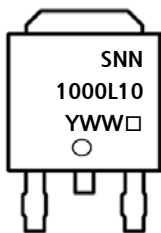
- Drain-source breakdown voltage: $BV_{DSS}=100V$
- Low gate charge device
- Low drain-source On resistance: $R_{DS(on)}=68m\Omega$ (Typ.)
- Advanced trench process technology
- High avalanche energy, 100% test


TO-252

Ordering Information

Part Number	Marking	Package
SNN1000L10D	SNN1000L10	TO-252

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWWN
 -. YWW: Date Code (year, week)
 -. □: Factory Management Code

Absolute maximum ratings ($T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	100	V	
Gate-source voltage	V_{GSS}	± 20	V	
Drain current (DC) *	I_D	$T_C=25^\circ C$	14.6	A
		$T_C=100^\circ C$	9.23	A
Drain current (Pulsed) *	I_{DM}	25	A	
Single pulsed avalanche energy ^(Note 1)	E_{AS}	9	mJ	
Single avalanche current	I_{AS}	6	A	
Power dissipation	P_D	30	W	
Operating junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55 to 150	$^\circ C$	

* Limited only maximum junction temperature

SNN1000L10D

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 4.16	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	1.2	-	2.9	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$	-	-	10	uA
		$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^\circ\text{C}$	-	-	100	
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=5\text{A}$	-	-	100	mΩ
		$V_{GS}=4.5\text{V}$, $I_D=3\text{A}$	-	-	110	mΩ
Forward transfer conductance (Note 2)	g_{fs}	$V_{DS}=5\text{V}$, $I_D=5\text{A}$	-	14	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	1028	-	pF
Output capacitance	C_{oss}		-	46	-	
Reverse transfer capacitance	C_{rss}		-	36	-	
Turn-on delay time (Note 2, 3, 4)	$t_{d(on)}$	$V_{DD}=50\text{V}$, $I_D=5\text{A}$ $R_G=3\Omega$, $V_{GS}=10\text{V}$	-	3.8	-	ns
Rise time (Note 2, 3, 4)	t_r		-	25.8	-	
Turn-off delay time (Note 2, 3, 4)	$t_{d(off)}$		-	16.8	-	
Fall time (Note 2, 3, 4)	t_f		-	8.8	-	
Total gate charge (Note 2, 3, 4)	Q_g	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$ $I_D=5\text{A}$	-	12.5	-	nC
Gate-source charge (Note 2, 3, 4)	Q_{gs}		-	3.5	-	
Gate-drain charge (Note 2, 3, 4)	Q_{gd}		-	1.5	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	14.6	A
Source current (Pulsed)	I_{SM}		-	-	25	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=1\text{A}$	-	-	1.2	V

Note:

1. $L=0.5\text{mH}$, $I_{AS}=6\text{A}$, $V_{DD}=25\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
2. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 1.5\%$
3. Essentially independent of operating temperature typical characteristics
4. Guaranteed by design, not subject to production testing.

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

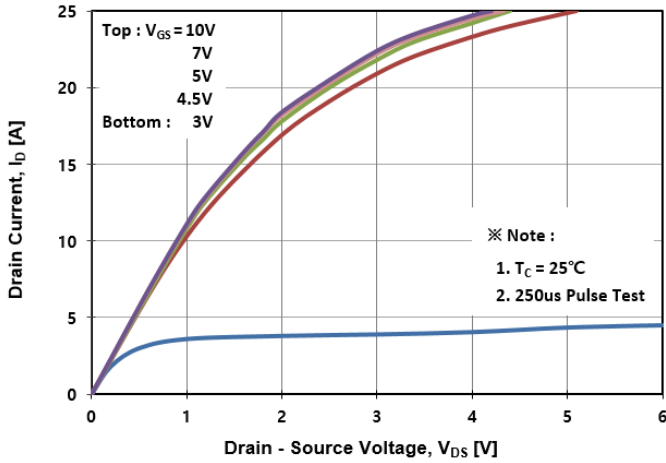


Fig. 2 On-Resistance vs. Gate Source Voltage

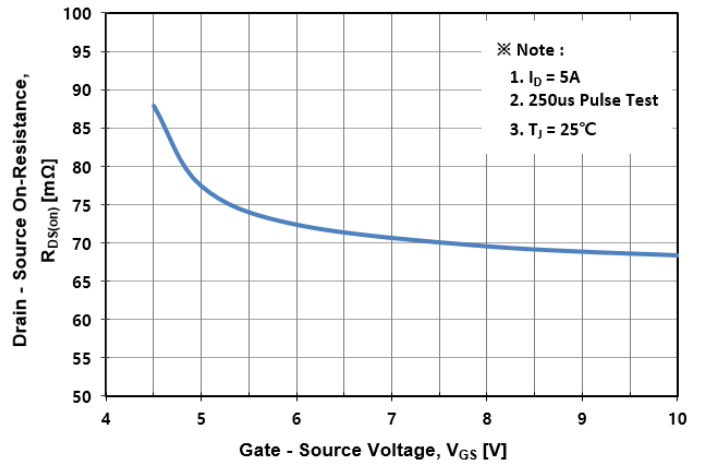


Fig.3 Forward Characteristics of Reverse

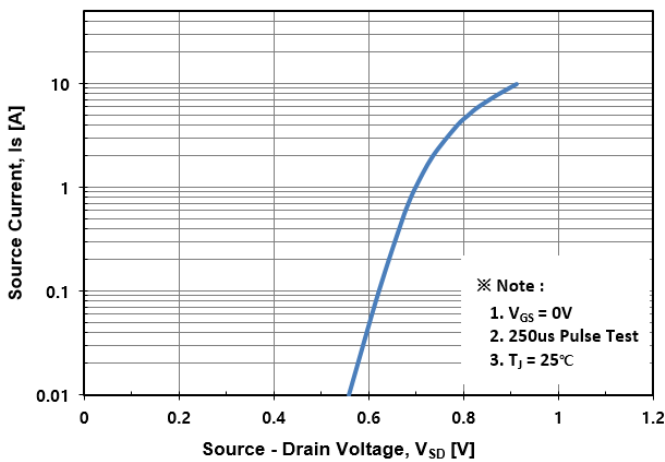


Fig. 4 Safe Operating Area Characteristics

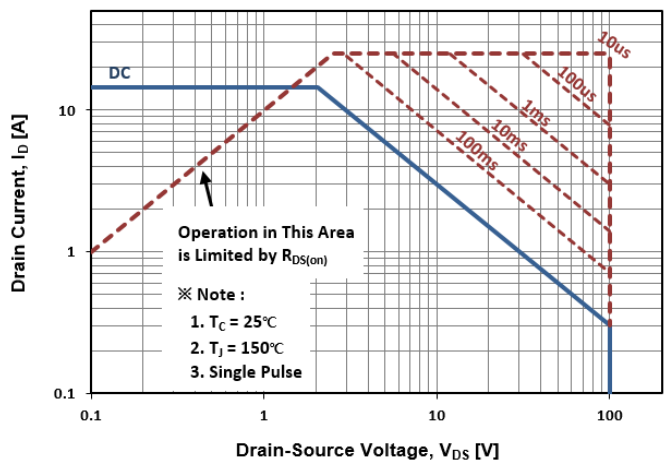


Fig. 5 Capacitance Characteristics

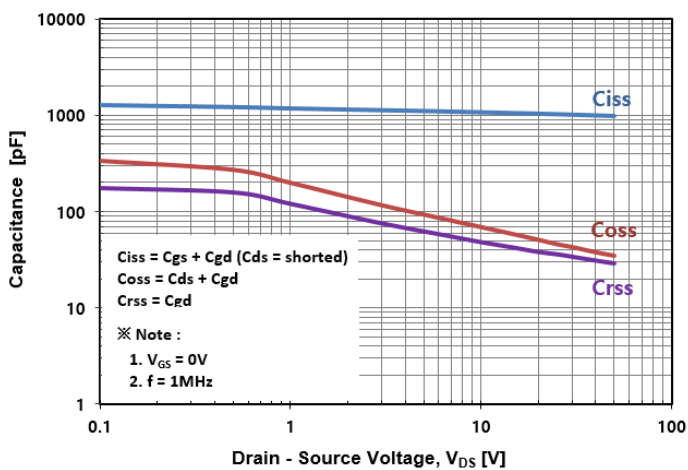


Fig. 6 Total Gate Charge Characteristics

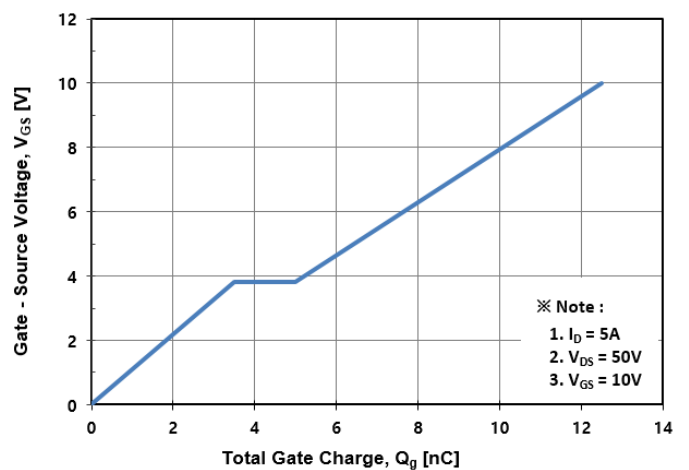


Fig. 7 Normalized $V_{GS(th)}$ vs. T_j Characteristics

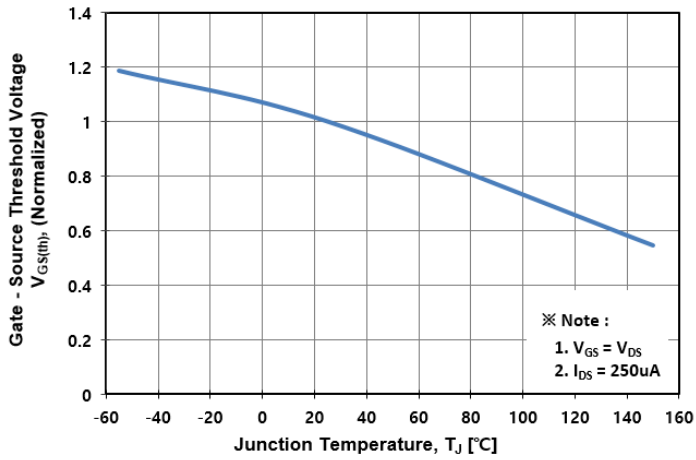


Fig. 8 Normalized $R_{DS(on)}$ vs. T_j Characteristics

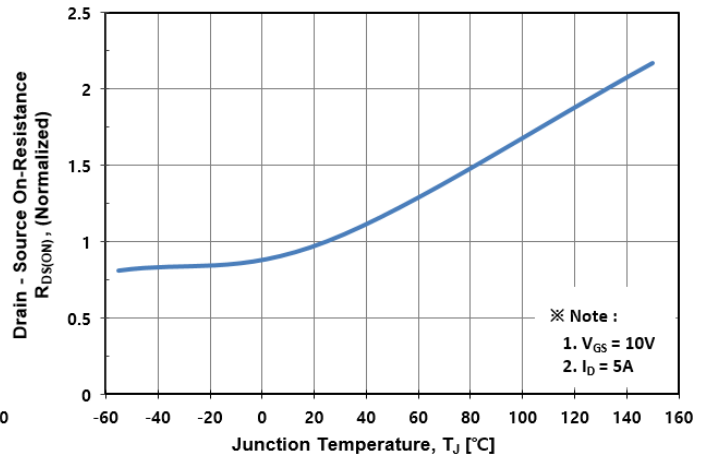


Fig. 9 Maximum Transient Thermal Impedance

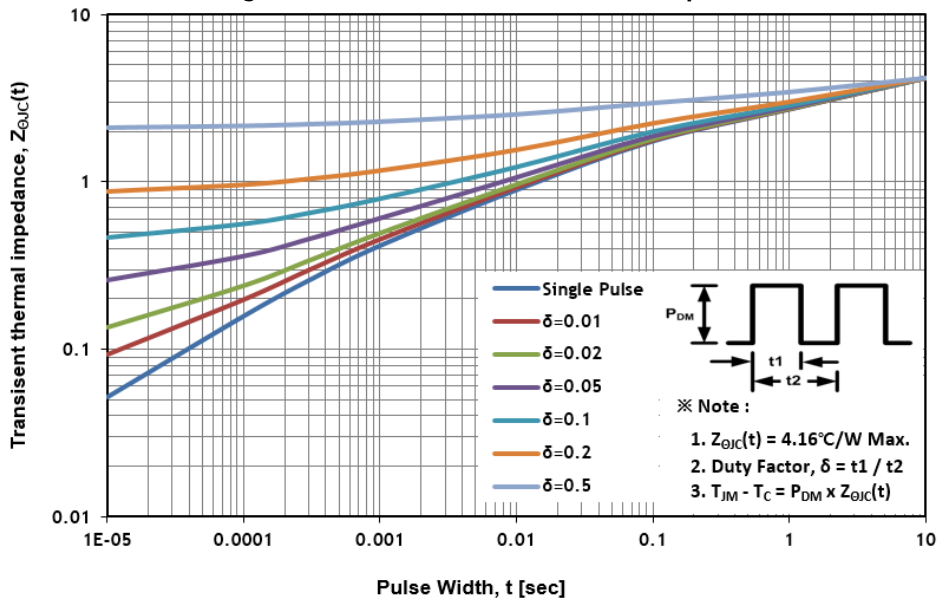


Fig. 10 Gate Charge Test Circuit & Waveform

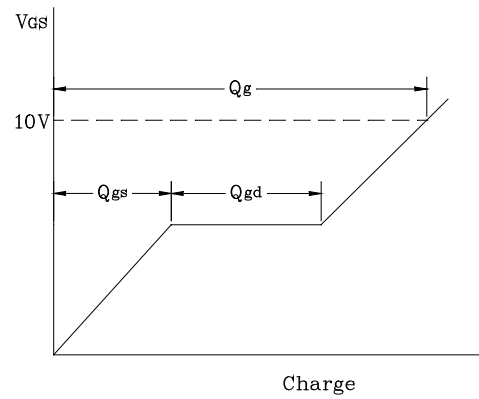
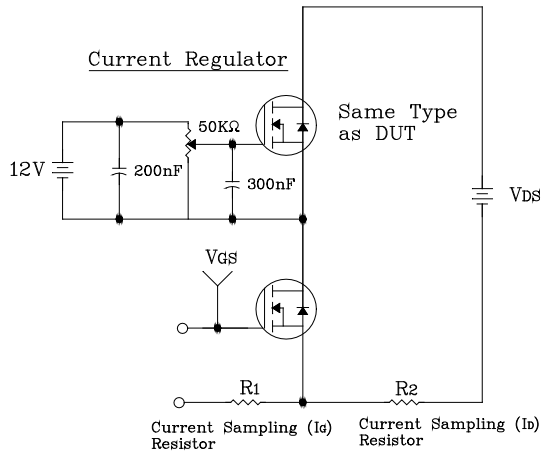


Fig. 11 Resistive Switching Test Circuit & Waveform

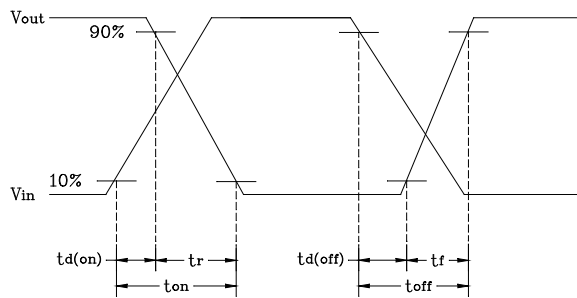
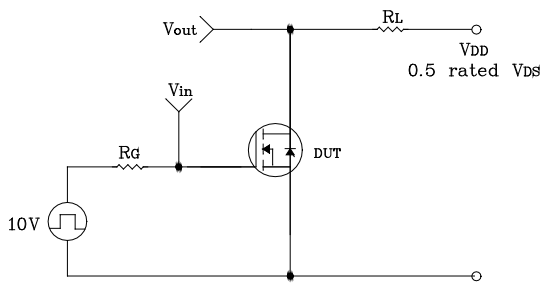


Fig. 12 EAS Test Circuit & Waveform

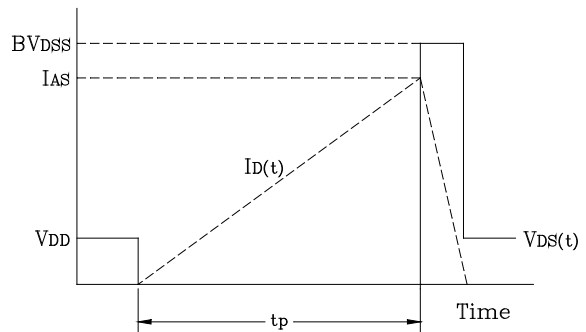
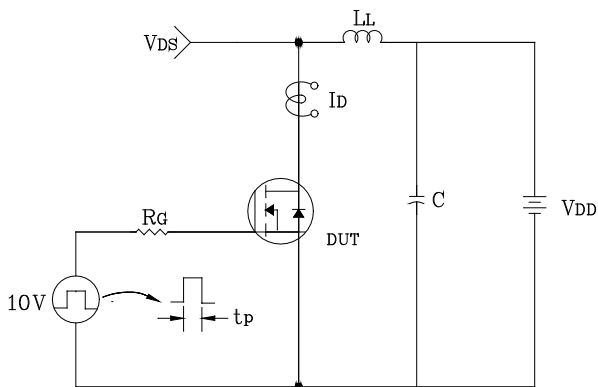
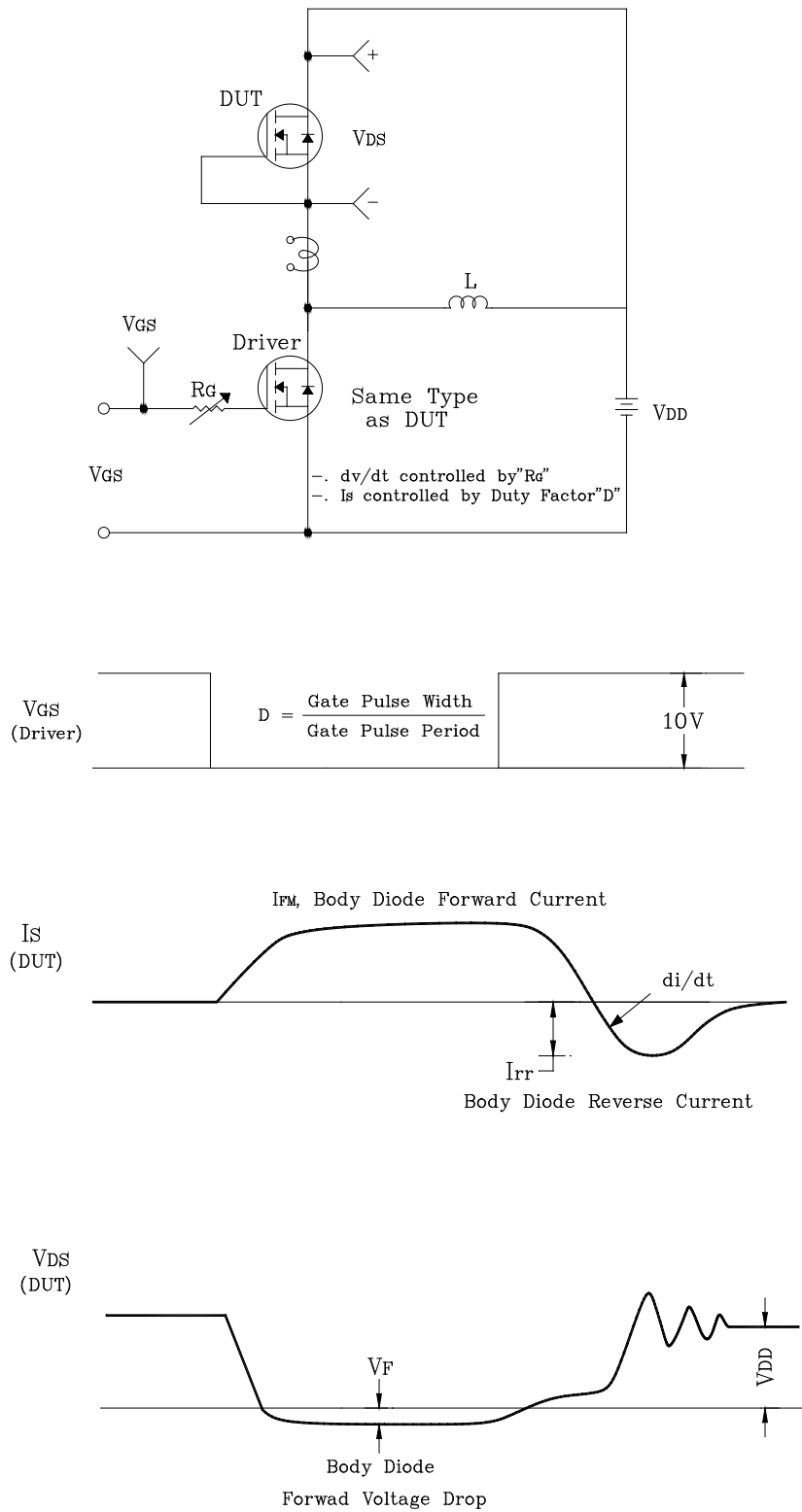
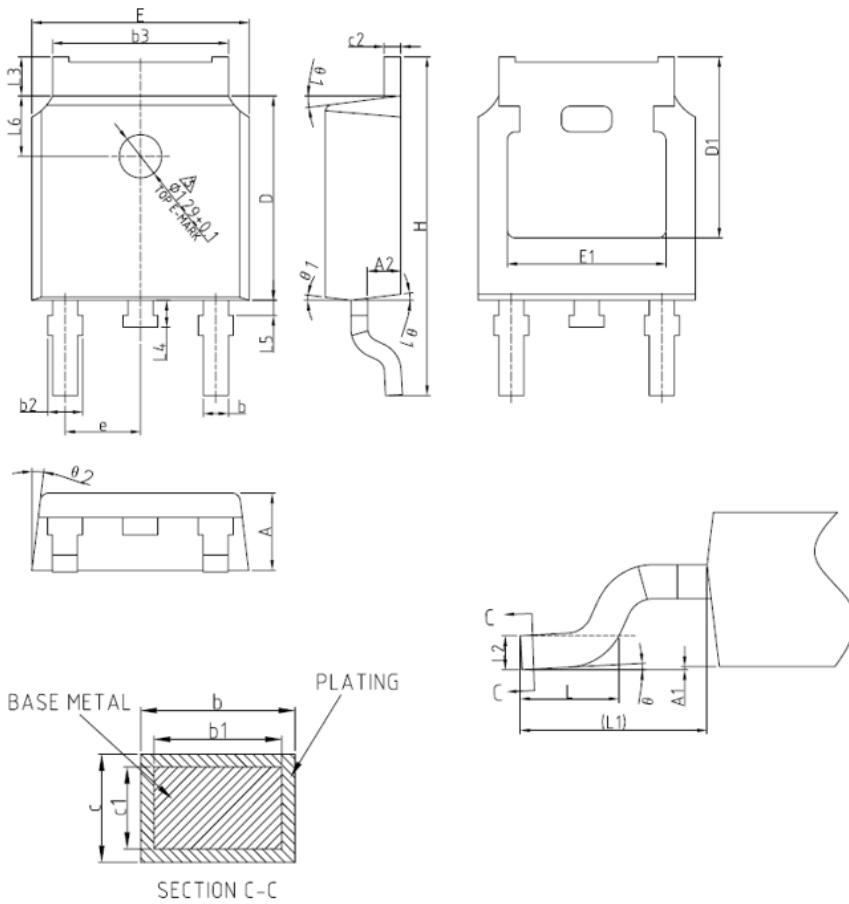


Fig. 13 Diode Reverse Recovery Time Test Circuit & Waveform



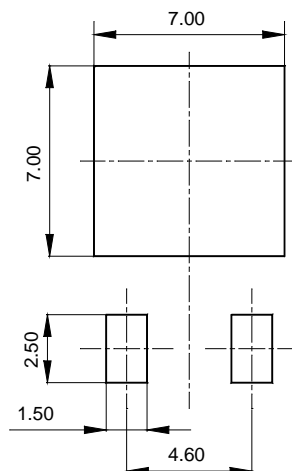
Package Outline Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0	-	0.10
A2	0.90	1.01	1.10
b	0.72	-	0.85
b1	0.71	0.76	0.81
b2	0.72	-	0.90
b3	5.13	5.33	5.46
c	0.47	-	0.60
c1	0.46	0.51	0.56
c2	0.47	-	0.60
D	6.00	6.10	6.20
D1	5.25	-	-
E	6.50	6.60	6.70
E1	4.70	-	-
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	0.15	-	0.75
L6	1.80REF		
θ	0°	-	8°
θ 1	5°	7°	9°
θ 2	5°	7°	9°

Recommended Land Pattern [unit: mm]



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