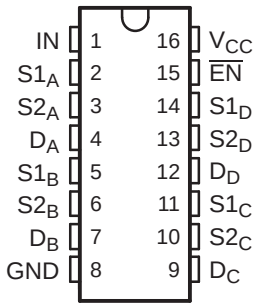
# QUAD SPDT WIDE-BANDWIDTH VIDEO SWITCH WITH LOW ON-STATE RESISTANCE

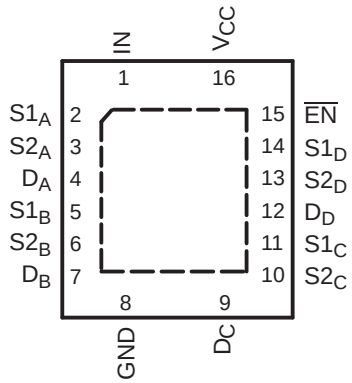
## FEATURES

- **Low Differential Gain and Phase ($D_G$ = 0.64%, $D_P$ = 0.1 Degrees Typ)**
- **Wide Bandwidth (BW = 300 MHz Min)**
- **Low Crosstalk ($X_{TALK}$ = –63 dB Typ)**
- **Low Power Consumption ($I_{CC}$ = 3 μA Max)**
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low ON-State Resistance ($r_{on}$ = 3 Ω Typ)**
- **$V_{CC}$ Operating Range From 4.5 V to 5.5 V**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Data and Control Inputs Provide Undershoot Clamp Diode**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **1000-V Charged-Device Model (C101)**
- **Suitable for Both RGB and Composite-Video Switching**

**D, DBQ, OR PW PACKAGE**
**(TOP VIEW)**




**RGY PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

The TS5V330 video switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ($\overline{EN}$) input. When $\overline{EN}$ is low, the switch is enabled and the D port is connected to the S port. When $\overline{EN}$ is high, the switch is disabled and the high-impedance state exists between the D and S ports. The select (IN) input controls the data path of the multiplexer/demultiplexer.

Low differential gain and phase make this switch ideal for composite and RGB video applications. This device has wide bandwidth and low crosstalk, making it suitable for high-frequency applications as well.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. This switch maintains isolation during power off.

### ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | QFN – RGY | Tape and reel | TS5V330RGYR | TE330 |
| | SOIC – D | Tube | TS5V330D | TS5V330 |
| | | Tape and reel | TS5V330DR | |
| | SSOP (QSOP) – DBQ | Tape and reel | TS5V330DBQR | TE330 |
| | TSSOP – PW | Tube | TS5V330PW | TE330 |
| | | Tape and reel | TS5V330PWR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, $\overline{EN}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### FUNCTION TABLE

| INPUTS | | INPUT/OUTPUT D | FUNCTION |
|---|---|---|---|
| $\overline{EN}$ | IN | | |
| L | L | S1 | D port = S1 port |
| L | H | S2 | D port = S2 port |
| H | X | Z | Disconnect |

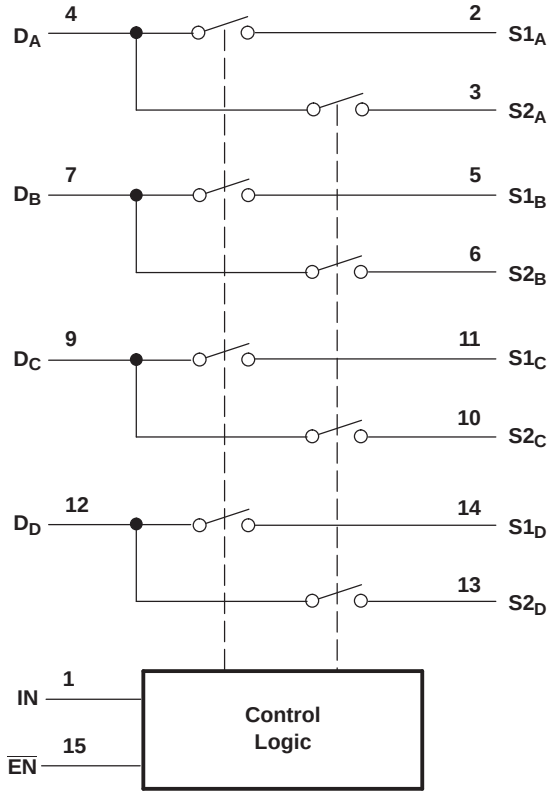
### PIN DESCRIPTION

| PIN | DESCRIPTION |
|---|---|
| S1, S2 | Analog video I/Os |
| D | Analog video I/Os |
| IN | Select input |
| $\overline{EN}$ | Switch-enable input |

## PARAMETER DEFINITIONS

| PARAMETER | DESCRIPTION |
|---|---|
| $r_{on}$ | Resistance between the D and S ports, with the switch in the ON state |
| $I_{OZ}$ | Output leakage current measured at the D and S ports, with the switch in the OFF state |
| $I_{OS}$ | Short-circuit current measured at the I/O pins |
| $V_{IN}$ | Voltage at IN |
| $V_{EN}$ | Voltage at $\overline{EN}$ |
| $C_{IN}$ | Capacitance at the control ($\overline{EN}$, IN) inputs |
| $C_{OFF}$ | Capacitance at the analog I/O port when the switch is OFF |
| $C_{ON}$ | Capacitance at the analog I/O port when the switch is ON |
| $V_{IH}$ | Minimum input voltage for logic high for the control ($\overline{EN}$, IN) inputs |
| $V_{IL}$ | Minimum input voltage for logic low for the control ($\overline{EN}$, IN) inputs |
| $V_{hys}$ | Hysteresis voltage at the control ($\overline{EN}$, IN) inputs |
| $V_{IK}$ | I/O and control ($\overline{EN}$, IN) inputs diode clamp voltage |
| $V_I$ | Voltage applied to the D or S pins when D or S is the switch input |
| $V_O$ | Voltage applied to the D or S pins when D or S is the switch output |
| $I_{IH}$ | Input high leakage current of the control ($\overline{EN}$, IN) inputs |
| $I_{IL}$ | Input low leakage current of the control ($\overline{EN}$, IN) inputs |
| $I_I$ | Current into the D or S pins when D or S is the switch input |
| $I_O$ | Current into the D or S pins when D or S is the switch output |
| $I_{off}$ | Output leakage current measured at the D or S ports, with $V_{CC}$ = 0 |
| $t_{ON}$ | Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned ON |
| $t_{OFF}$ | Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned OFF |
| BW | Frequency response of the switch in the ON state measured at –3 dB |
| $X_{TALK}$ | Unwanted signal coupled from channel to channel. Measured in –dB. $X_{TALK}$ = 20 log $V_O/V_I$. This is a nonadjacent crosstalk. |
| $O_{IRR}$ | Off isolation is the resistance (measured in –dB) between the input and output with the switch OFF. |
| $D_G$ | Magnitude variation between analog input and output pins when the switch is ON and the dc offset of composite-video signal varies at the analog input pin. In the NTSC standard, the frequency of the video signal is 3.58 MHz, and dc offset is from 0 to 0.714 V. |
| $D_P$ | Phase variation between analog input and output pins when the switch is ON and the dc offset of composite-video signal varies at the analog input pin. In the NTSC standard, the frequency of the video signal is 3.58 MHz, and dc offset is from 0 to 0.714 V. |
| $I_{CC}$ | Static power-supply current |
| $I_{CCD}$ | Variation of $I_{CC}$ for a change in frequency in the control ($\overline{EN}$, IN) inputs |
| $\Delta I_{CC}$ | This is the increase in supply current for each control input that is at the specified voltage level, rather than $V_{CC}$ or GND. |

### FUNCTIONAL DIAGRAM (POSITIVE LOGIC)




## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_{IN}$ | Control input voltage range(2)(3) | | –0.5 | 7 | V |
| $V_{I/O}$ | Switch I/O voltage range(2)(3)(4) | | –0.5 | 7 | V |
| $I_{IK}$ | Control input clamp current | $V_{IN}$ < 0 | | –50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O}$ < 0 | | –50 | mA |
| $I_{I/O}$ | ON-state switch current(5) | | | ±128 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance | D package(6) | | 73 | °C/W |
| | | DBQ package(6) | | 90 | |
| | | PW package(6) | | 108 | |
| | | RGY package(7) | | 39 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
(5) $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) The package thermal impedance is calculated in accordance with JESD 51-5.

## Recommended Operating Conditions(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | 4 | 5.5 | V |
| $V_{IH}$ | High-level control input voltage range ($\overline{EN}$, IN) | 2 | 5.5 | V |
| $V_{IL}$ | Low-level control input voltage range ($\overline{EN}$, IN) | 0 | 0.8 | V |
| $V_{ANALOG}$ | Analog I/O voltage range | 0 | Vcc | V |
| $T_A$ | Operating free-air temperature range | –40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ±10% (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS(1) | | | | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $\overline{EN}$, IN | $V_{CC}$ = 4.5 V, | $I_{IN}$ = –18 mA | | | | | –1.8 | V |
| $V_{hys}$ | $\overline{EN}$, IN | | | | | | 150 | | mV |
| $I_{IH}$ | $\overline{EN}$, IN | $V_{CC}$ = 5.5 V, | $V_{IN}$ and $V_{EN}$ = $V_{CC}$ | | | | | ±1 | µA |
| $I_{IL}$ | $\overline{EN}$, IN | $V_{CC}$ = 5.5 V, | $V_{IN}$ and $V_{EN}$ = GND | | | | | ±1 | µA |
| $I_{OZ}$(3) | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0, | Switch OFF | | | ±1 | µA |
| $I_{OS}$(4) | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 $V_{CC}$, | $V_I$ = 0, | Switch ON | 50 | | | mA |
| $I_{off}$ | | $V_{CC}$ = 0 V, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0 | | | | 1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_{I/O}$ = 0, | Switch ON or OFF | | | | 3 | µA |
| $\Delta I_{CC}$ | $\overline{EN}$, IN | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other inputs at $V_{CC}$ or GND | | | | 2.5 | mA |
| $I_{CCD}$ | | $V_{EN}$ = GND, $V_{CC}$ = 5.5 V, D and S ports open, $V_{IN}$ input switching 50% duty cycle | | | | | | 0.25 | mA/MHz |
| $C_{IN}$ | $\overline{EN}$, IN | $V_{IN}$ of $V_{EN}$ = 0, f = 1 MHz | | | | | 3.5 | | pF |
| $C_{OFF}$ | D port | $V_I$ = 0, | f = 1 MHz, | Outputs open, | Switch OFF | | 6 | | pF |
| | S port | | | | | | 4 | | |
| $C_{ON}$ | | $V_I$ = 0, | f = 1 MHz, | Outputs open, | Switch ON | | 14 | | pF |
| $r_{on}$(5) | | $V_{CC}$ = 4.5 V | $V_I$ = 1 V, | $I_O$ = 13 mA, | $R_L$ = 75 Ω | | 3 | 7 | Ω |
| | | | $V_I$ = 2 V, | $I_O$ = 26 mA, | $R_L$ = 75 Ω | | 7 | 10 | |

(1) $V_I$, $V_O$, $I_I$, and $I_O$ refer to I/O pins.
(2) All typical values are at $V_{CC}$ = 5 V (unless otherwise noted), $T_A$ = 25°C.
(3) For I/O ports, $I_{OZ}$ includes the input leakage current.
(4) The $I_{OS}$ test is applicable to only one ON channel at a time. The duration of this test is less than 1 s.
(5) Measured by the voltage drop between the D and S terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (D or S) terminals.

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 10%, $R_L$ = 75 Ω, $C_L$ = 20 pF (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{ON}$ | S | D | | 2.5 | 6 | ns |
| $t_{OFF}$ | S | D | | 1.1 | 6 | ns |

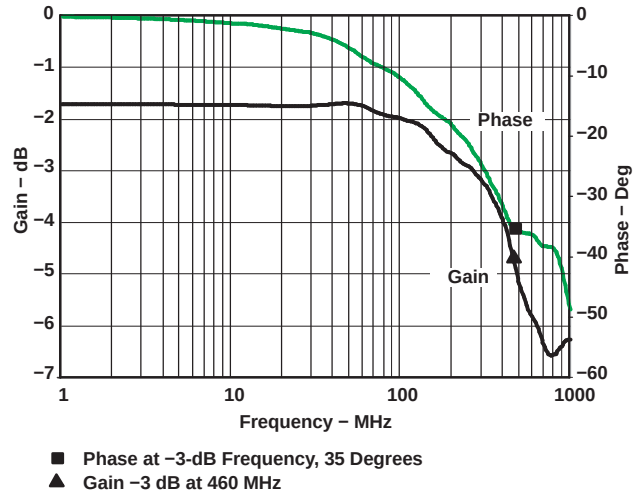
## Dynamic Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 10% (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $D_G$(2) | $R_L$ = 150 Ω, | f = 3.58 MHz, | See Figure 6 | | | 0.64 | | % |
| $D_P$(2) | $R_L$ = 150 Ω, | f = 3.58 MHz, | See Figure 6 | | | 0.1 | | Deg |
| BW | $R_L$ = 150 Ω, | See Figure 7 | | | 300 | | | MHz |
| $X_{TALK}$ | $R_L$ = 150 Ω, | f = 10 MHz, | RIN = 10 Ω, | See Figure 8 | | –63 | | dB |
| $O_{IRR}$ | $R_L$ = 150 Ω, | f = 10 MHz, | See Figure 9 | | | –60 | | dB |

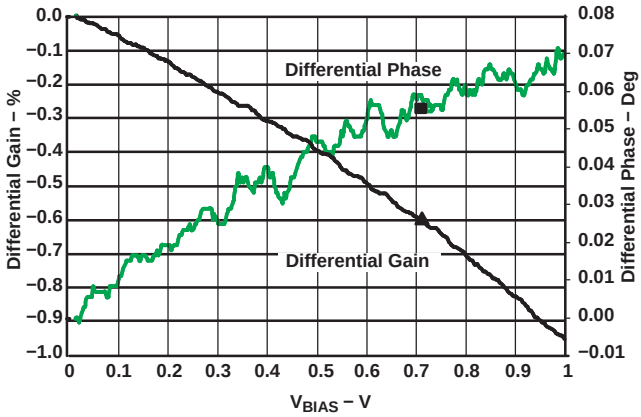
(1) All typical values are at $V_{CC}$ = 5 V (unless otherwise noted), $T_A$ = 25°C.
(2) $D_G$ and $D_P$ are expressed in absolute magnitude.

## OPERATING CHARACTERISTICS




■ Phase at −3-dB Frequency, 35 Degrees
▲ Gain −3 dB at 460 MHz

**Figure 1. Gain/Phase vs Frequency**




■ Differential Phase at 0.714, 0.056 Degrees
▲ Differential Gain at 0.714, −0.63%

**Figure 2. Differential Gain/Phase vs $V_{BIAS}$**

## OPERATING CHARACTERISTICS

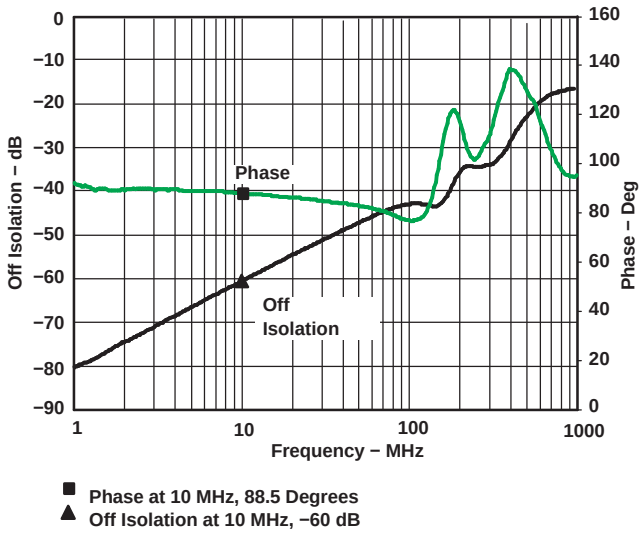



**Figure 3. Off Isolation vs Frequency**

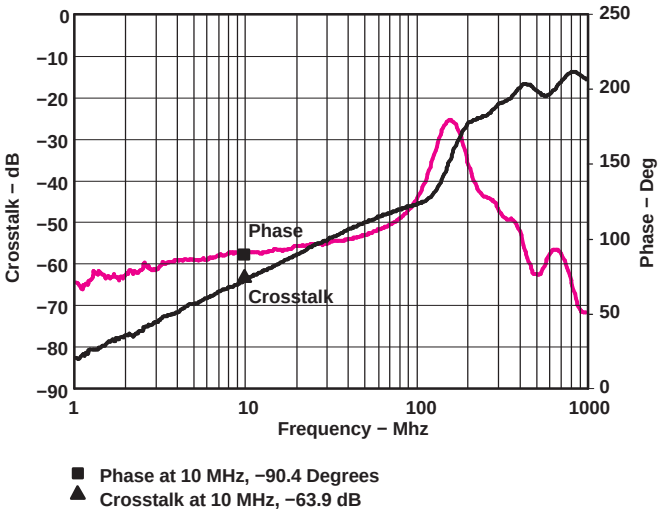
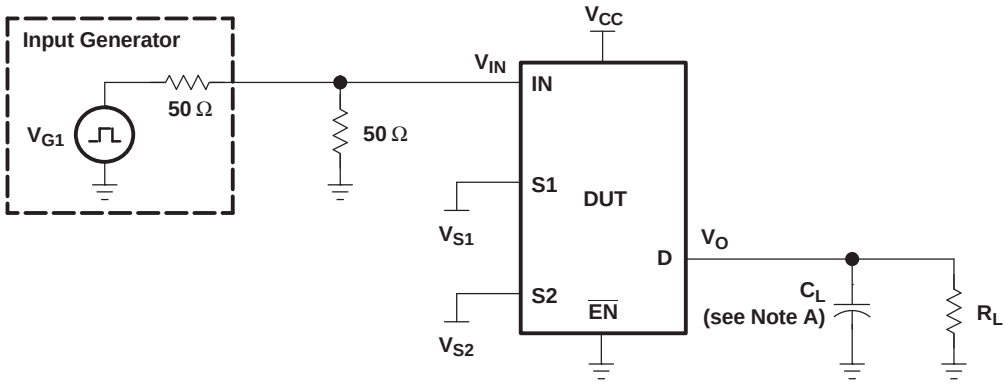


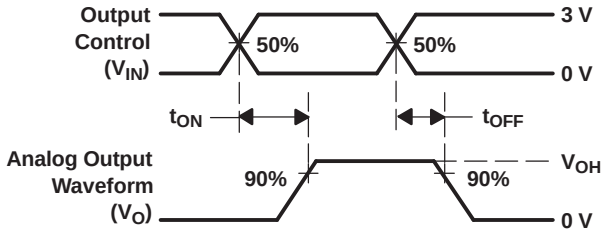

**Figure 4. Crosstalk vs Frequency**

## PARAMETER MEASUREMENT INFORMATION




| TEST | $V_{CC}$ | $R_L$ | $C_L$ | $V_{S1}$ | $V_{S2}$ |
|---|---|---|---|---|---|
| $t_{ON}$ | 5 V ± 0.5 V | 75 | 20 | GND | 3 V |
| | 5 V ± 0.5 V | 75 | 20 | 3 V | GND |
| $t_{OFF}$ | 5 V ± 0.5 V | 75 | 20 | GND | 3 V |
| | 5 V ± 0.5 V | 75 | 20 | 3 V | GND |

TEST CIRCUIT

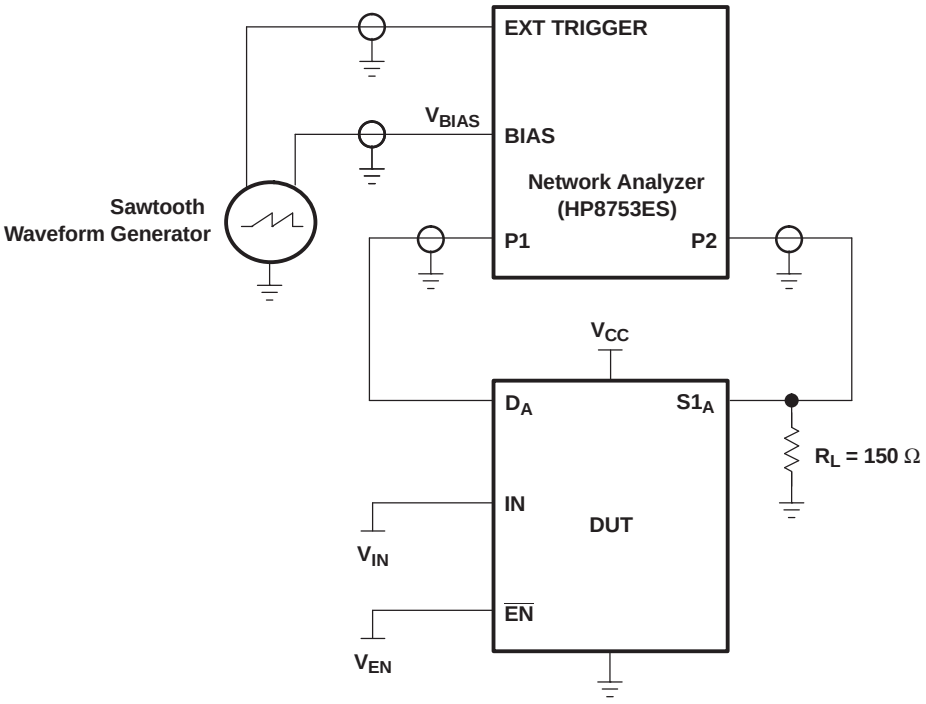



VOLTAGE WAVEFORMS
$t_{ON}$ AND $t_{OFF}$ TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.

**Figure 5. Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTE A: For additional information on measurement method, refer to the TI application report, *Measuring Differential Gain and Phase*, literature number SLOA040.

**Figure 6. Test Circuit for Differential Gain/Phase Measurement**

Differential gain and phase are measured at the output of the ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and DA is the input, the output is measured at $S1_A$.

### HP8753ES Setup

| | | |
|---|---|---|
| Average = 20<br>RBW = 300 Hz<br>ST = 1.381 s<br>P1 = –7 dBM<br>CW frequency = 3.58 MHz | | |

### Sawtooth Waveform Generator Setup

| |
|---|
| $V_{BIAS}$ = 0 to 1 V<br>Frequency = 0.905 Hz |

## PARAMETER MEASUREMENT INFORMATION

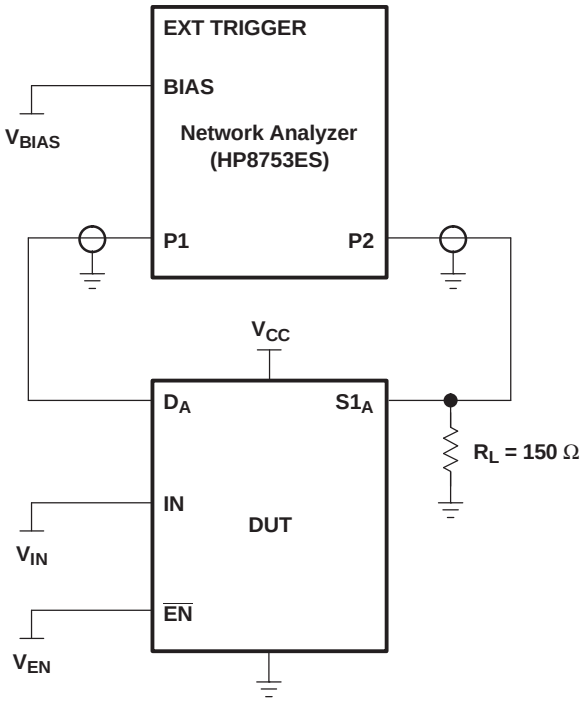


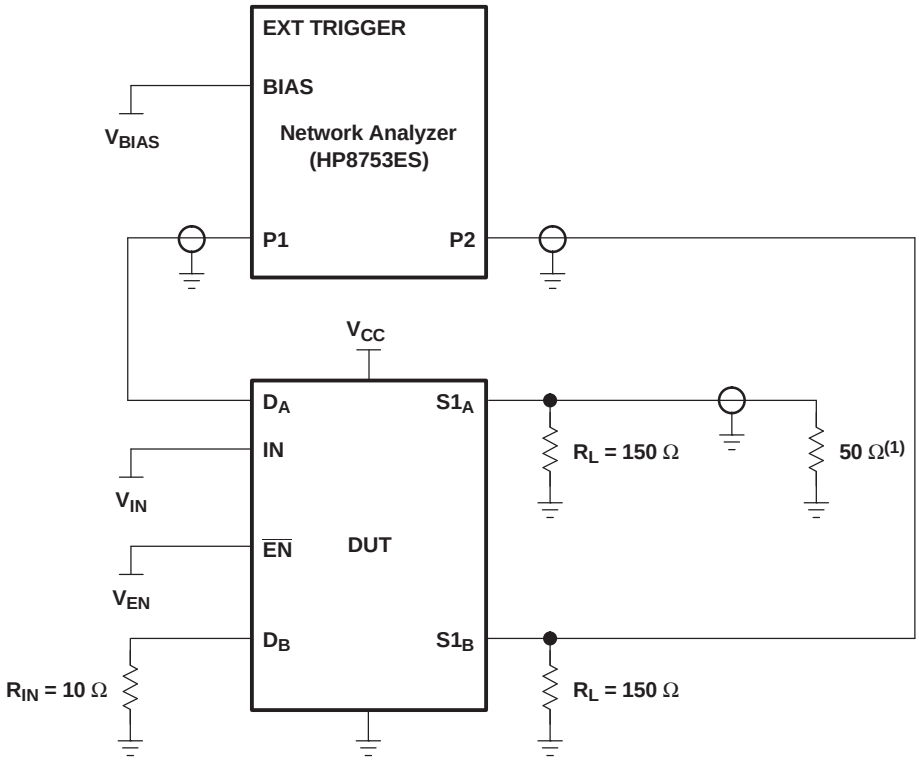

**Figure 7. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S1_A$. All unused analog I/O ports are left open.

### HP8753ES Setup

| | | |
|---|---|---|
| Average = 4<br>RBW = 3 Hz<br>$V_{BIAS}$ = 0.35 V<br>ST = 2 s<br>P1 = 0 dBM | | |

## PARAMETER MEASUREMENT INFORMATION




(1) A 50-Ω termination resistor is needed for the network analyzer.

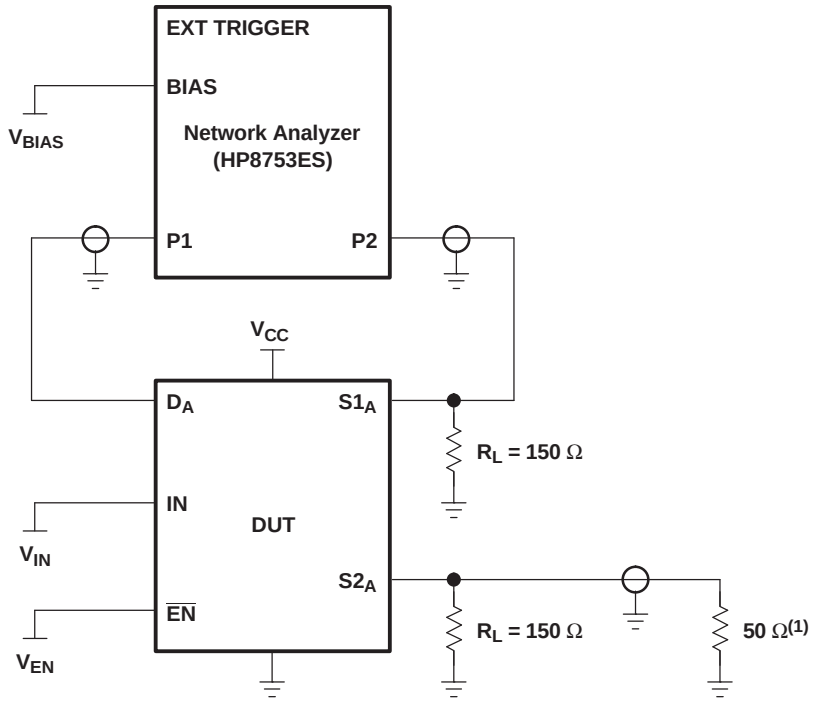
**Figure 8. Test Circuit for Crosstalk ($X_{TALK}$)**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S1_B$. All unused analog input (D) ports and output (S) ports are connected to GND through 10-Ω and 50-Ω pulldown resistors, respectively.

### HP8753ES Setup

| | | |
|---|---|---|
| Average = 4<br>RBW = 3 kHz<br>$V_{BIAS}$ = 0.35 V<br>ST = 2 s<br>P1 = 0 dBM | | |

## PARAMETER MEASUREMENT INFORMATION




(1) A 50-Ω termination resistor is needed for the network analyzer.

**Figure 9. Test Circuit for Off Isolation ($O_{IRR}$)**

Off isolation is measured at the output of the OFF channel. For example, when $V_{IN}$ = $V_{CC}$, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S1_A$. All unused analog input (D) ports are left open, and output (S) ports are connected to GND through 50-Ω pulldown resistors.

### HP8753ES Setup

| | | |
|---|---|---|
| Average = 4<br>RBW = 3 kHz<br>$V_{BIAS}$ = 0.35 V<br>ST = 2 s<br>P1 = 0 dBM | | |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5V330D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS5V330 | Samples |
| TS5V330DBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TE330 | Samples |
| TS5V330DBQRG4 | ACTIVE | SSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TE330 | Samples |
| TS5V330DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS5V330 | Samples |
| TS5V330DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS5V330 | Samples |
| TS5V330DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TS5V330 | Samples |
| TS5V330PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TE330 | Samples |
| TS5V330PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TE330 | Samples |
| TS5V330PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TE330 | Samples |
| TS5V330RGYR | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TE330 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

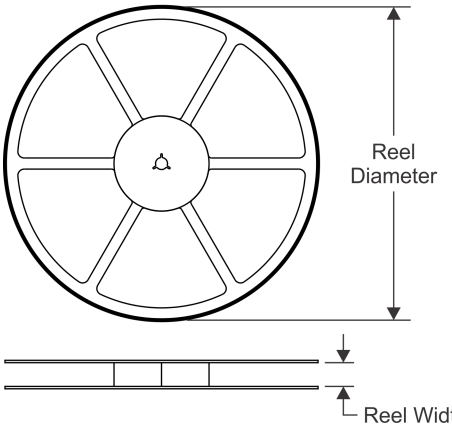
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

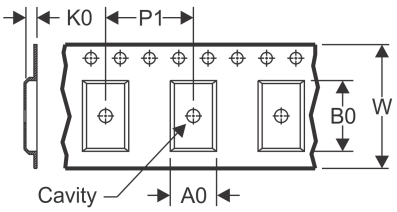
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

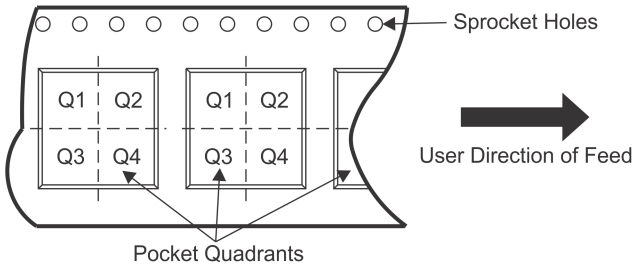



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

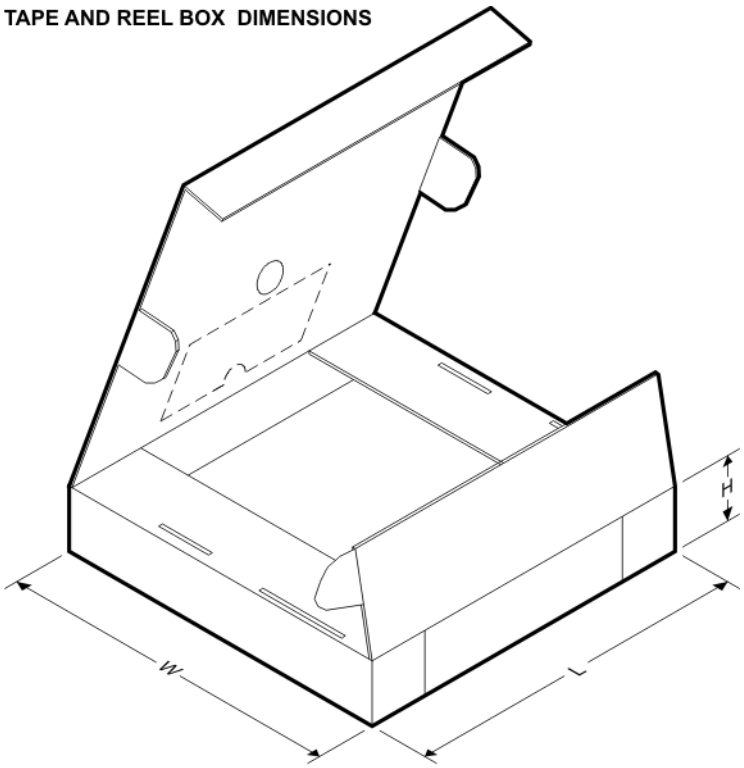
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5V330DBQR | SSOP | DBQ | 16 | 2500 | 330.0 | 12.5 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TS5V330DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TS5V330PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TS5V330RGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

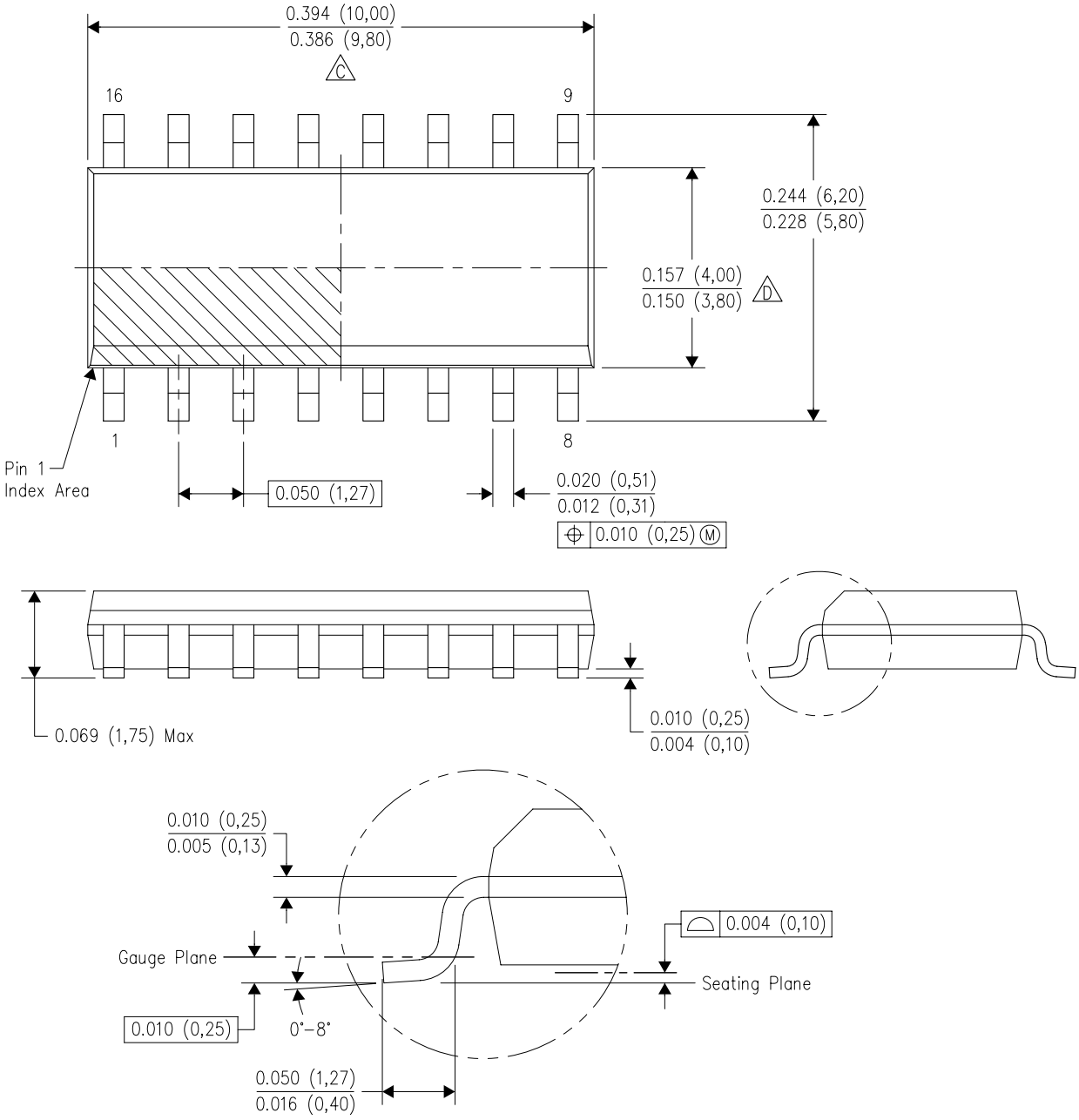
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

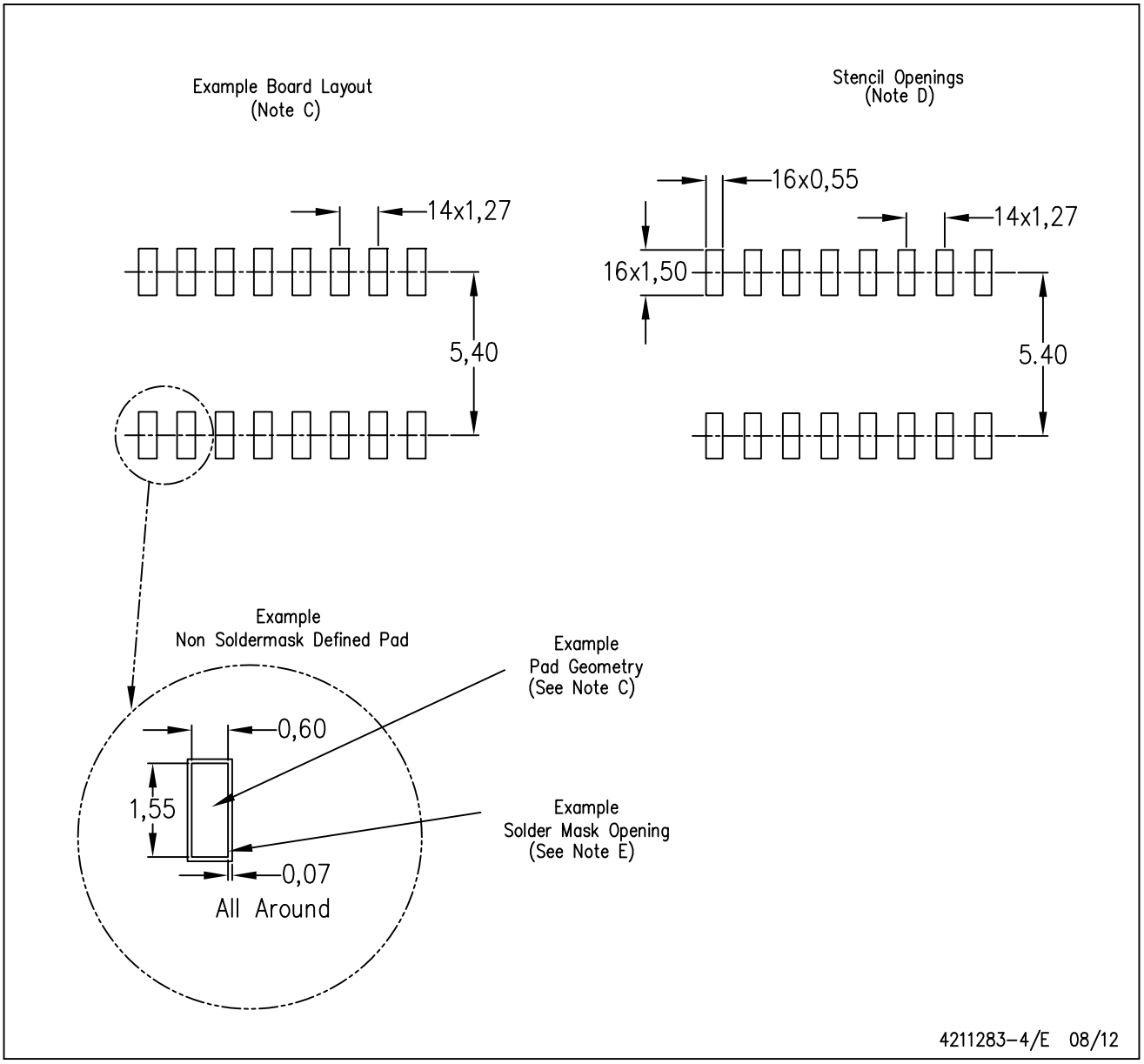
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS5V330DBQR | SSOP | DBQ | 16 | 2500 | 340.5 | 338.1 | 20.6 |
| TS5V330DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| TS5V330PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TS5V330RGYR | VQFN | RGY | 16 | 3000 | 367.0 | 367.0 | 35.0 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



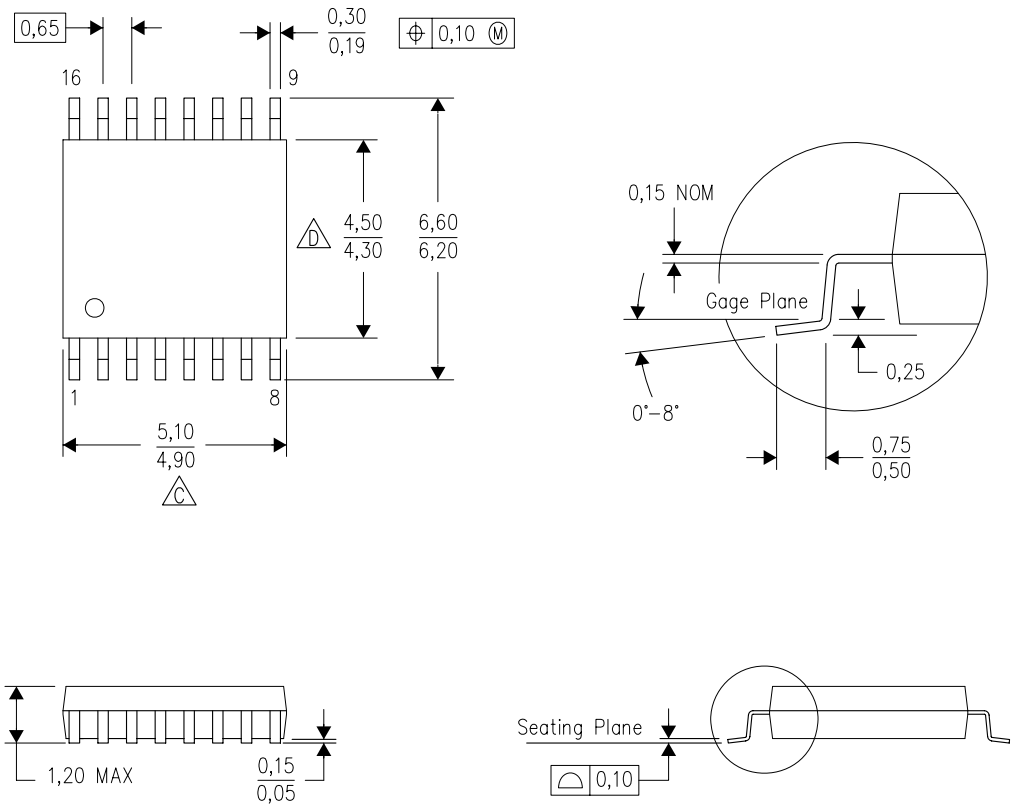

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

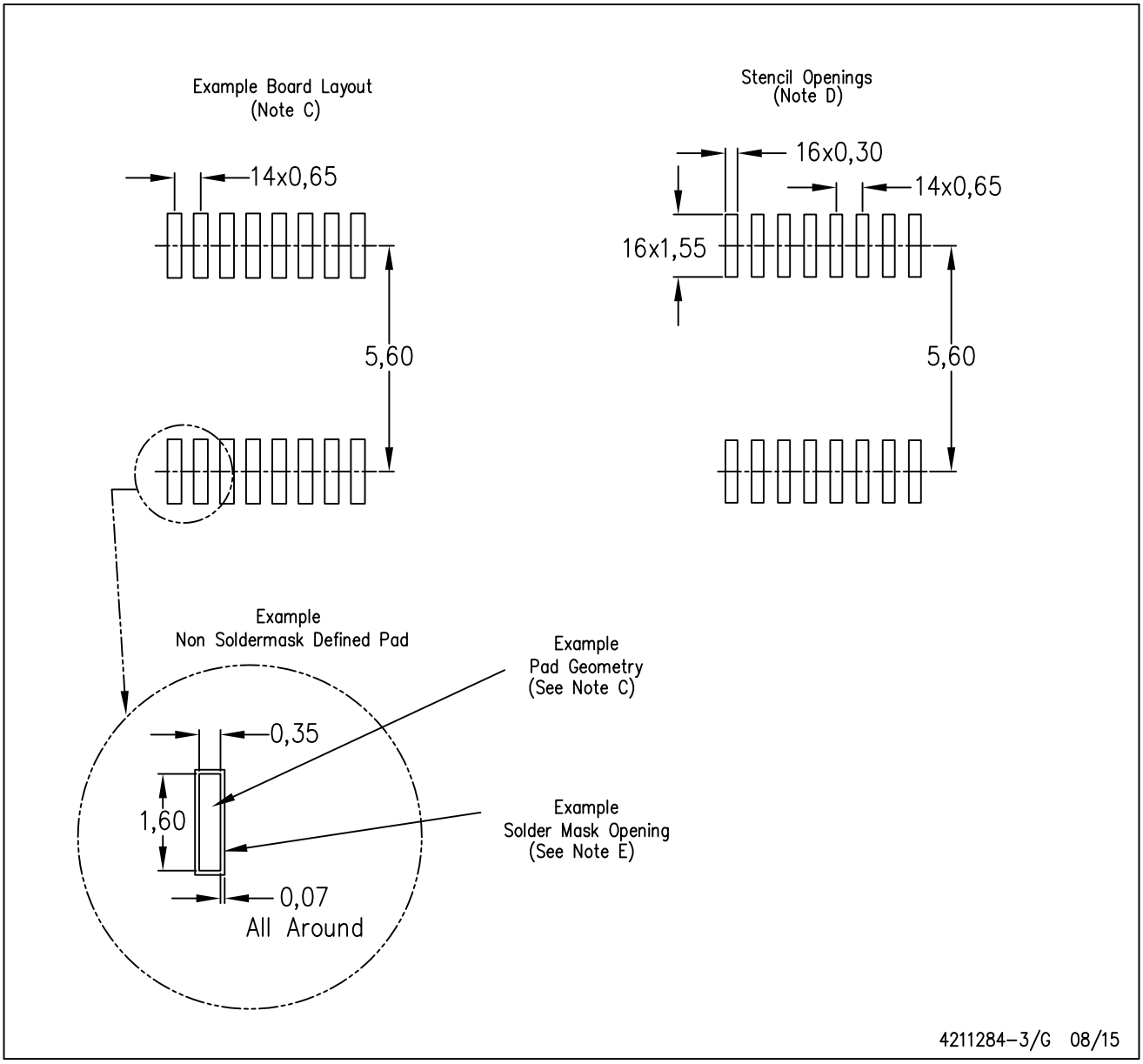
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

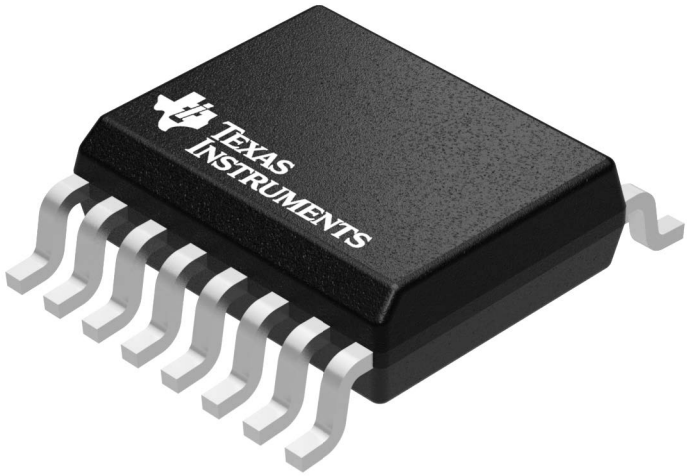



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

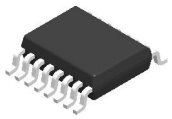
# GENERIC PACKAGE VIEW

## DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

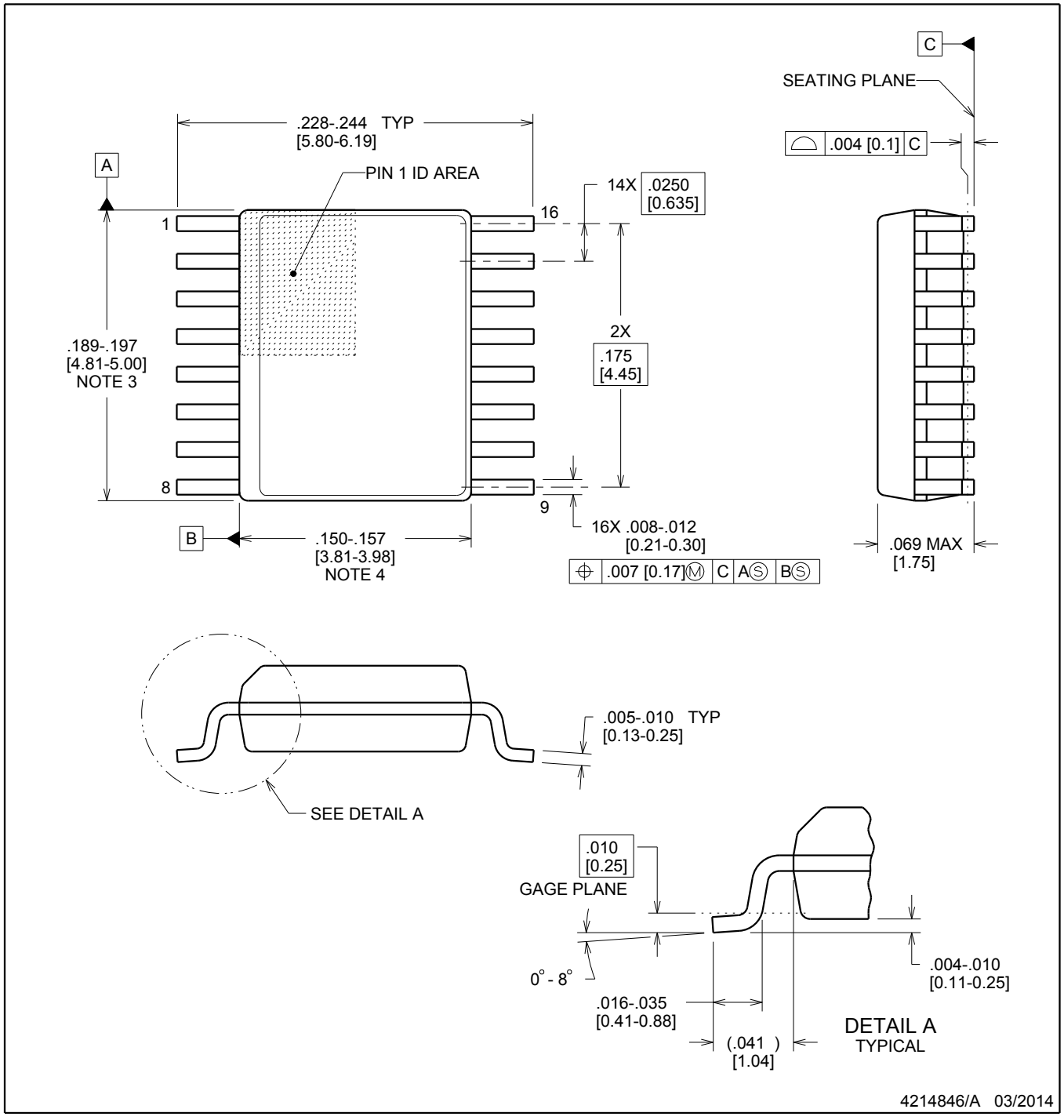


# PACKAGE OUTLINE

## DBQ0016A

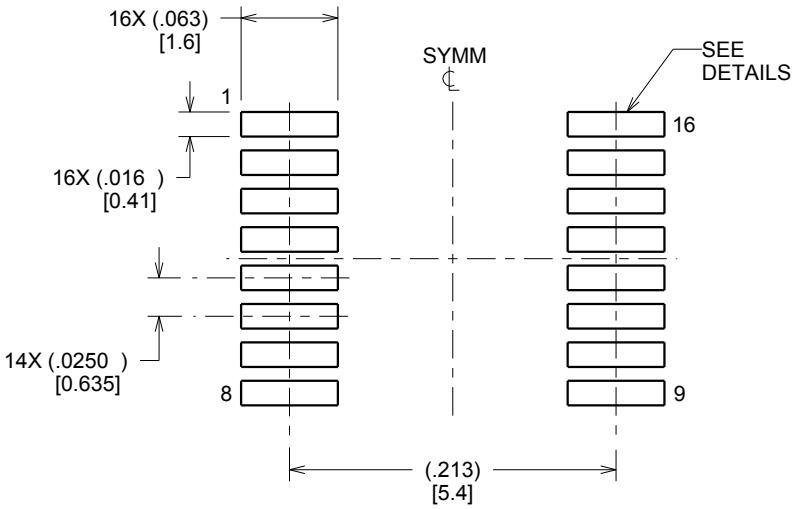
## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

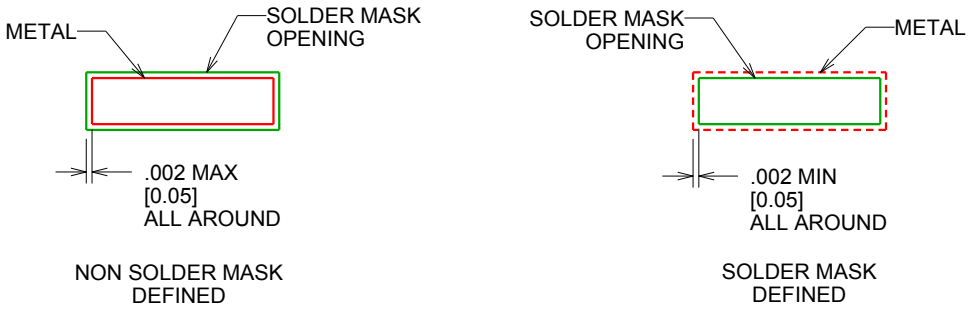



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

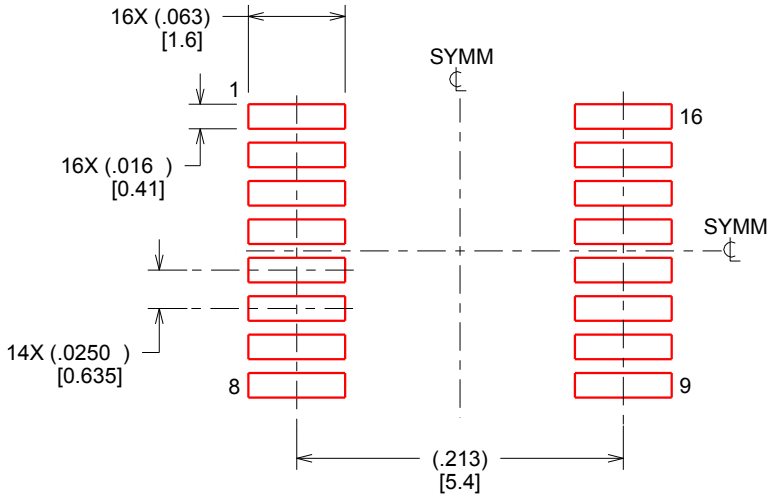
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DBQ0016A

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



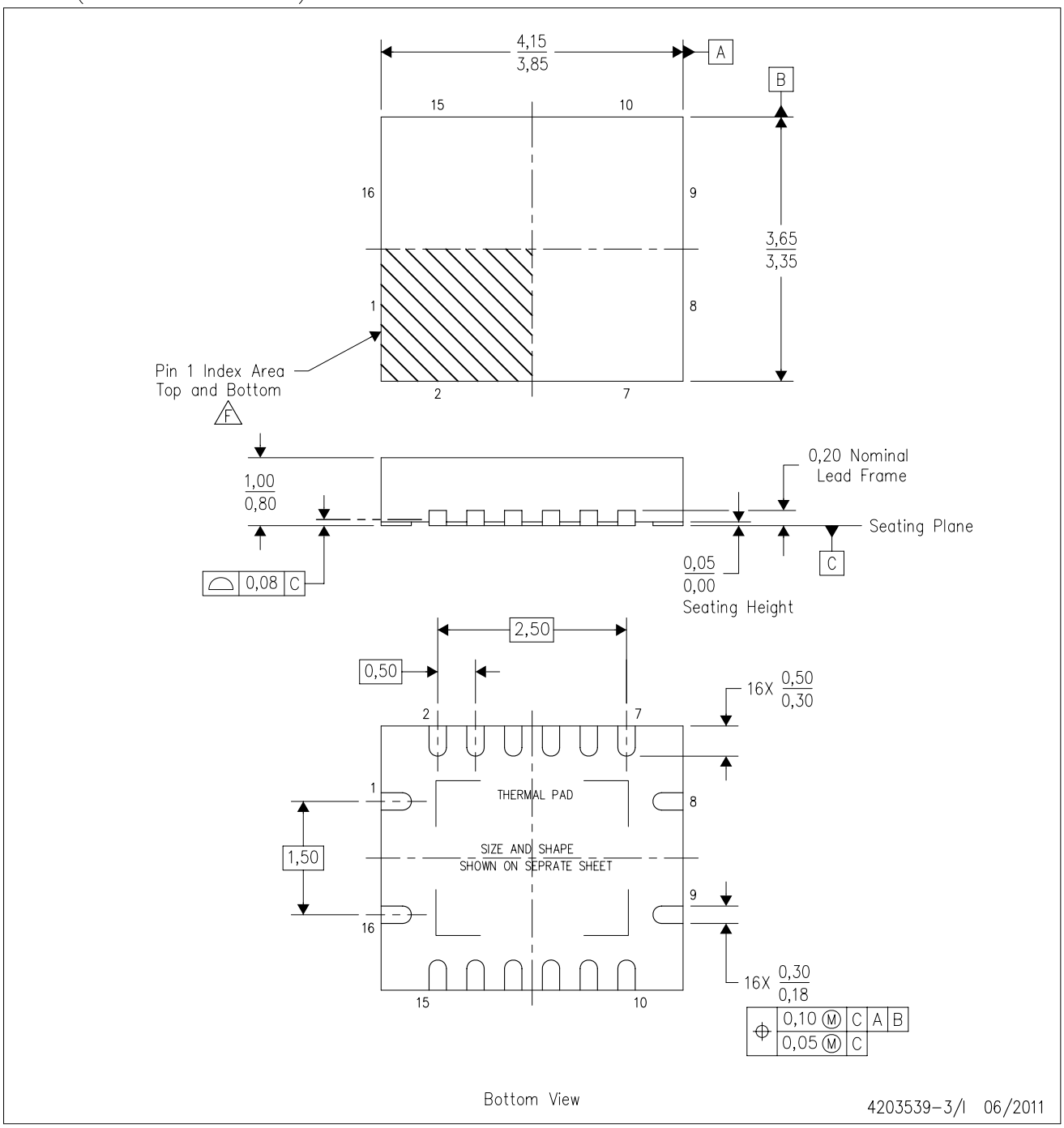

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

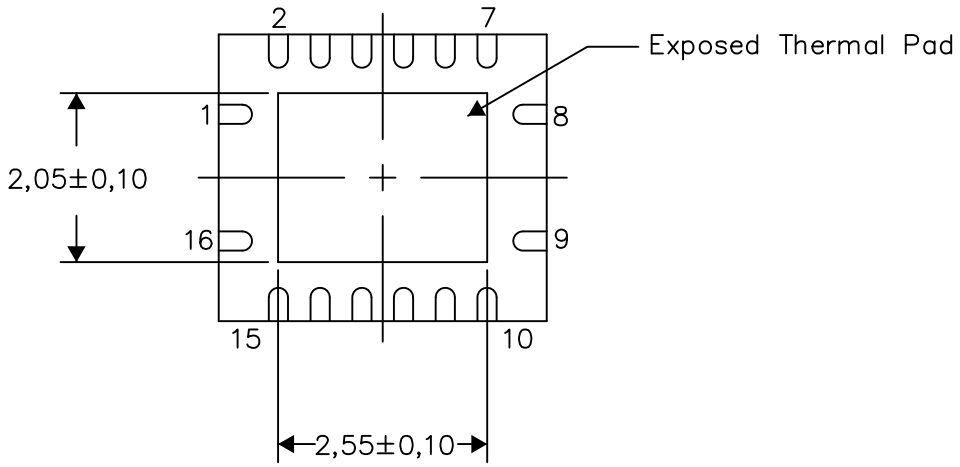
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



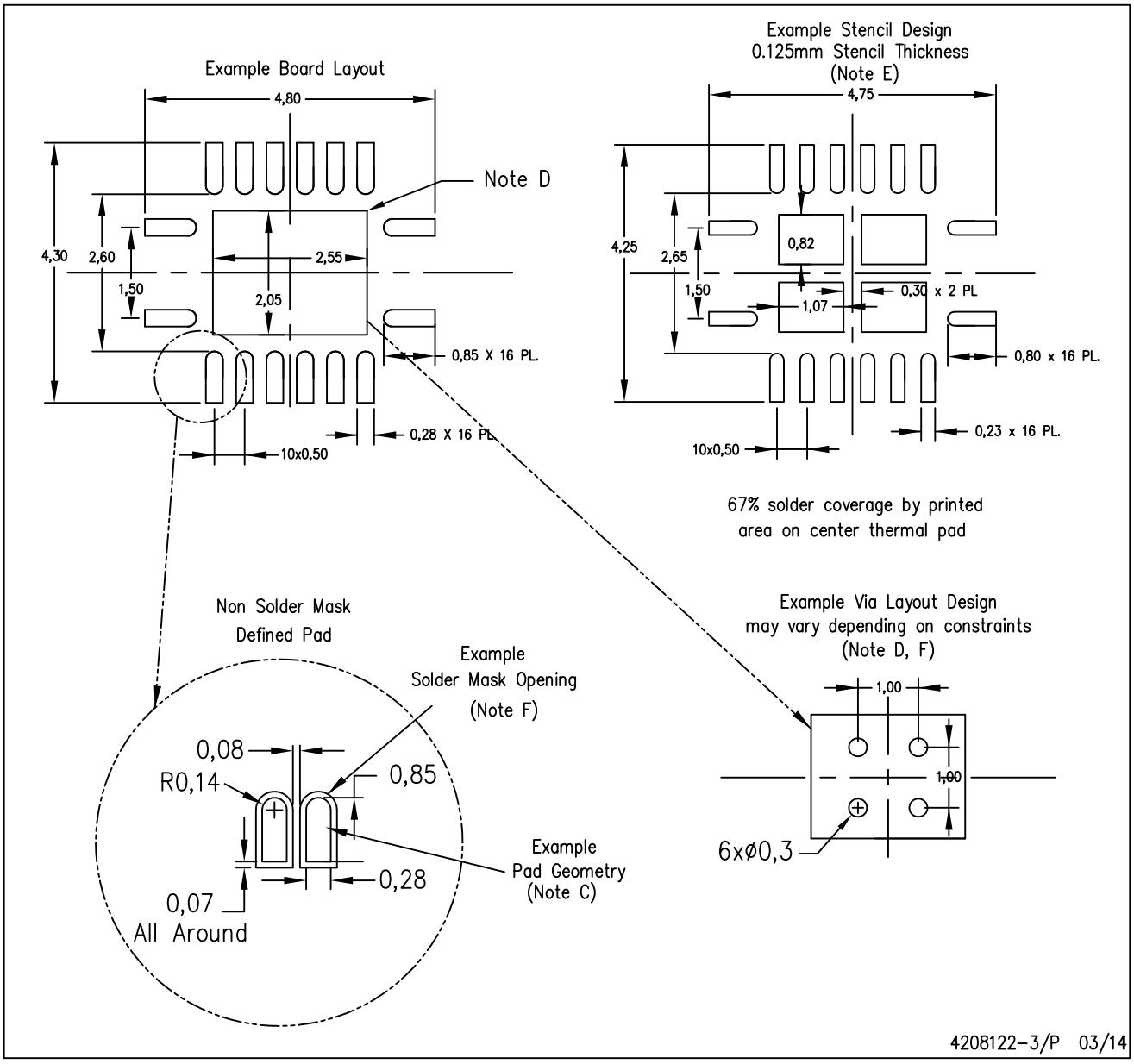

Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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