CEZ3P08

P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

■ -30V, -61A, $R_{DS(ON)}$= 9 mΩ @V_{GS} = -10V.

$R_{DS(ON)}$ = 13 mΩ @V_{GS} = -4.5V.

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

■ High power and current handing capability.

■ Lead-free plating ; RoHS compliant.

■ Surface mount Package.
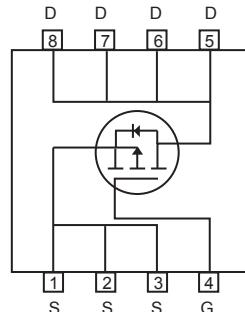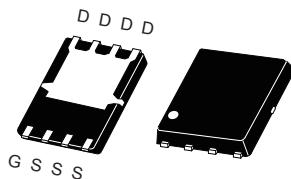
PR-PACK (5*6)

## ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

| Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	$\pm$20	V
Drain Current-Continuous	I_D @T_A	-21	A
Drain Current-Continuous	I_D @T_C	-61	A
Drain Current-Pulsed [a]	I_{DM} @T_A	-84	A
Drain Current-Pulsed [a]	I_{DM} @T_C	-244	A
Maximum Power Dissipation	P_D	54.3	W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150	$^\circ$C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.3	$^\circ$C/W
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	20	C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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CEZ3P08

Electrical Characteristics $T_A = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V$, $V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V$, $V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V$, $V_{DS} = 0V$			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	-1		-3	V
Static Drain-Source	$R_{DS(on)}$	$V_{GS} = -10V$, $I_D = -13A$		7.4	9	$m\Omega$
On-Resistance		$V_{GS} = -4.5V$, $I_D = -10A$		9	13	$m\Omega$
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	$V_{DS} = -15V$, $V_{GS} = 0V$, f = 1.0 MHz		4165		pF
Output Capacitance	C_{oss}			475		pF
Reverse Transfer Capacitance	C_{rss}			365		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V$, $I_D = -15A$, $V_{GS} = -10V$, $R_{GEN} = 6\Omega$		18		ns
Turn-On Rise Time	t_r			13		ns
Turn-Off Delay Time	$t_{d(off)}$			122		ns
Turn-Off Fall Time	t_f			48		ns
Total Gate Charge	Q_g	$V_{DS} = -15V$, $I_D = -13A$, $V_{GS} = -5V$		44		nC
Gate-Source Charge	Q_{gs}			9		nC
Gate-Drain Charge	Q_{gd}			13		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-61	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	$V_{GS} = 0V$, $I_S = -13A$			-1.1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.
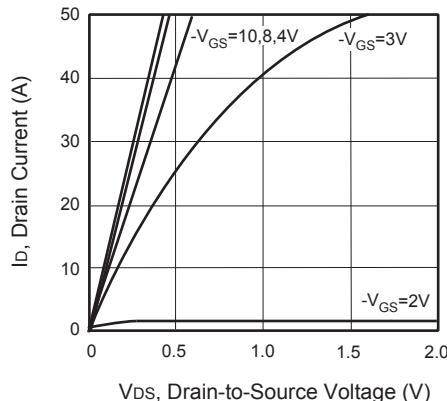
Figure 1. Output Characteristics
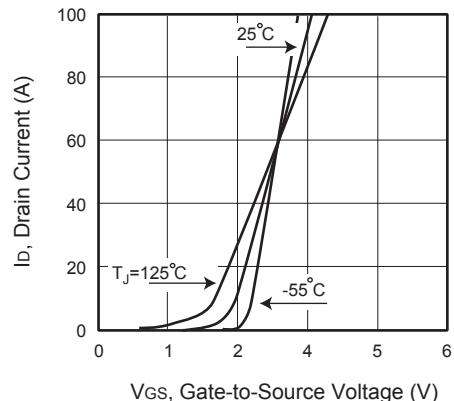
**Figure 2. Transfer Characteristics**
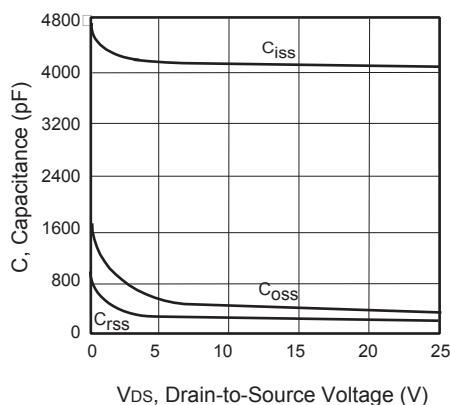
Figure 3. Capacitance
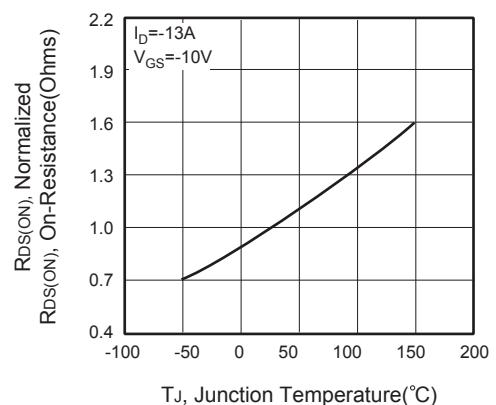
**Figure 4. On-Resistance Variation with Temperature**
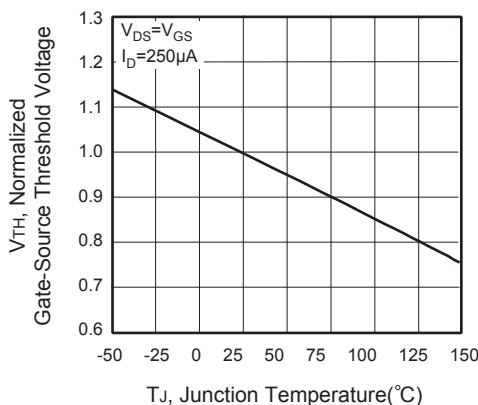
Figure 5. Gate Threshold Variation with Temperature
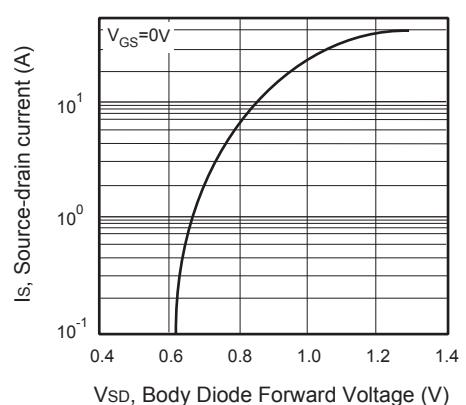
Figure 6. Body Diode Forward Voltage Variation with Source Current
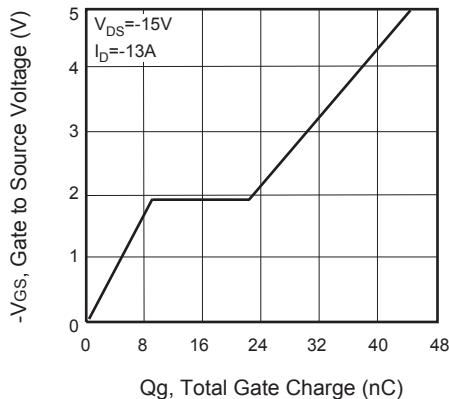
Figure 7. Gate Charge
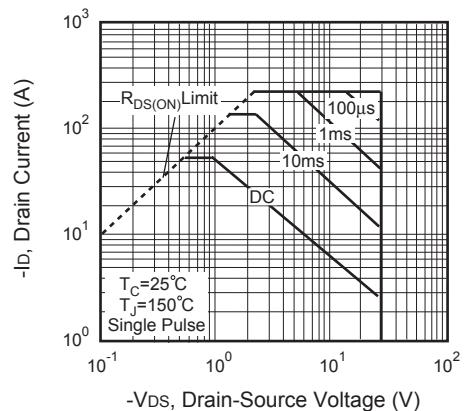
Figure 8. Maximum Safe Operating Area
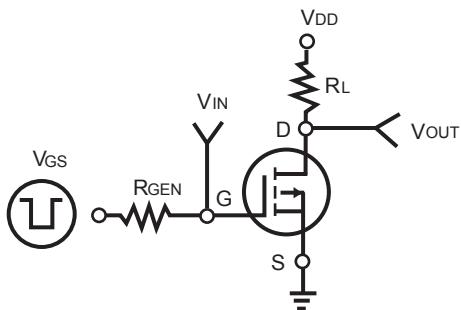
Figure 9. Switching Test Circuit
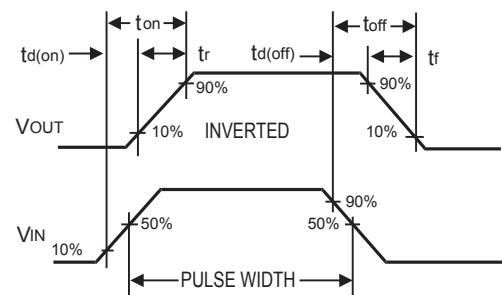
Figure 10. Switching Waveforms

1. $R_{\theta JC}(t) = r(t) * R_{\theta JC}$
2. $R_{\theta JC}$=See Datasheet
3. T_{JM}-T_C = P* $R_{\theta JC}(t)$
4. Duty Cycle, $D = t_1/t_2$
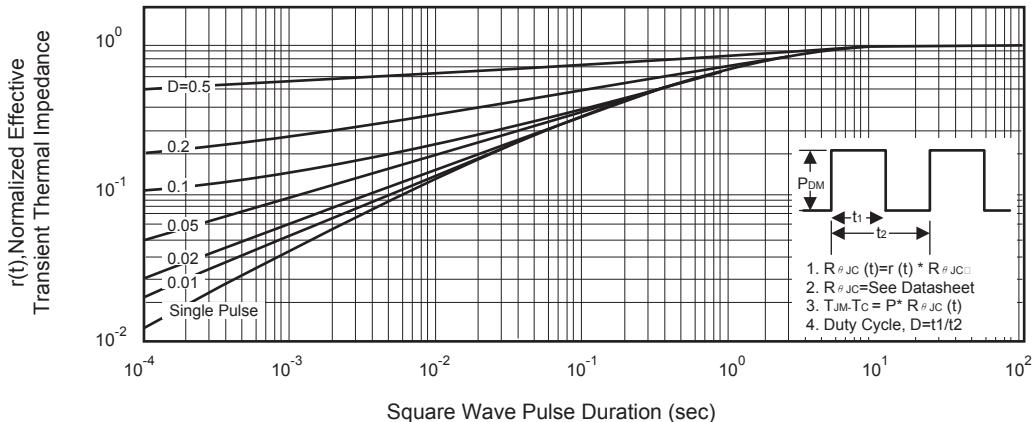
Figure 11. Normalized Thermal Transient Impedance Curve