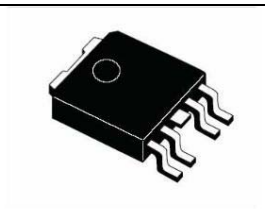
VN751PT

High-side driver

Datasheet - production data



PPAK

Features

- 8 V to 36 V supply voltage range
- Up to I_{OUT} = 2.5 A operating current
- $R_{DS(on)}$: 60 mΩ
- CMOS compatible input
- Thermal shutdown
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Fast demagnetization of inductive loads
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV
- Open drain status output

Description

The VN751PT is a monolithic device developed using STMicroelectronics' VIPower M03 technology, intended to drive any kind of load with one side connected to ground. Active VCC pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in conformity with IEC 61131-2 programmable controller international standard.

Table 1. Device summary

Order code	Package	Packing
VN751PT	PPAK	Tube
VN751PTTR		Tape and reel

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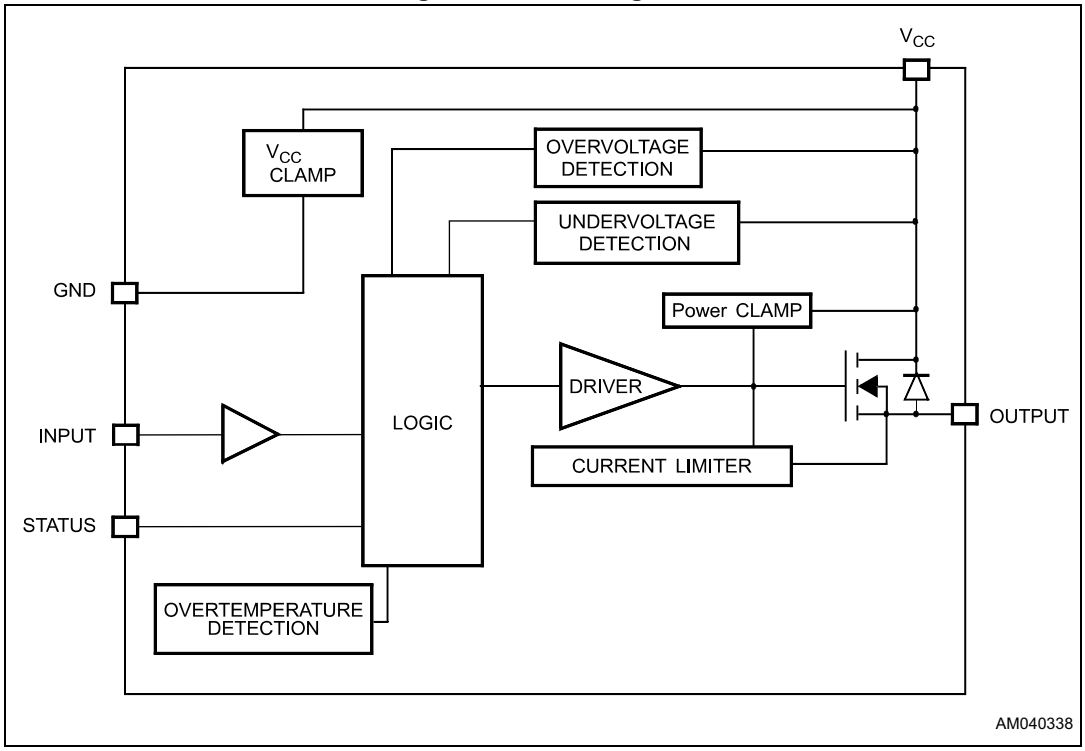
1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Connection diagram (top view)

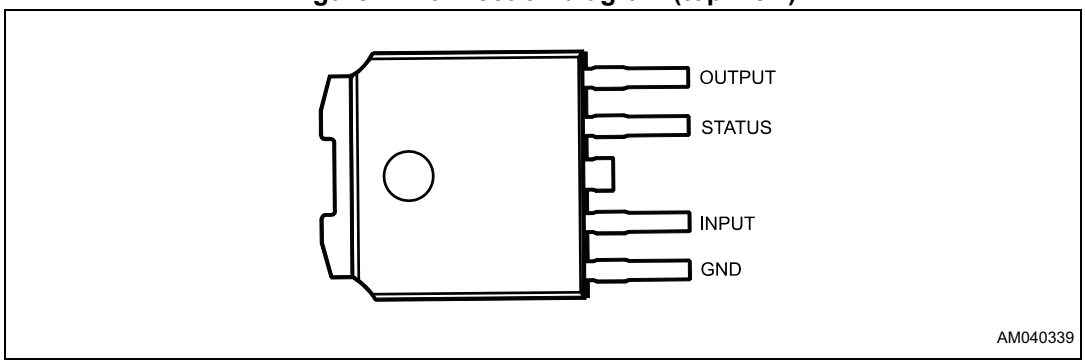
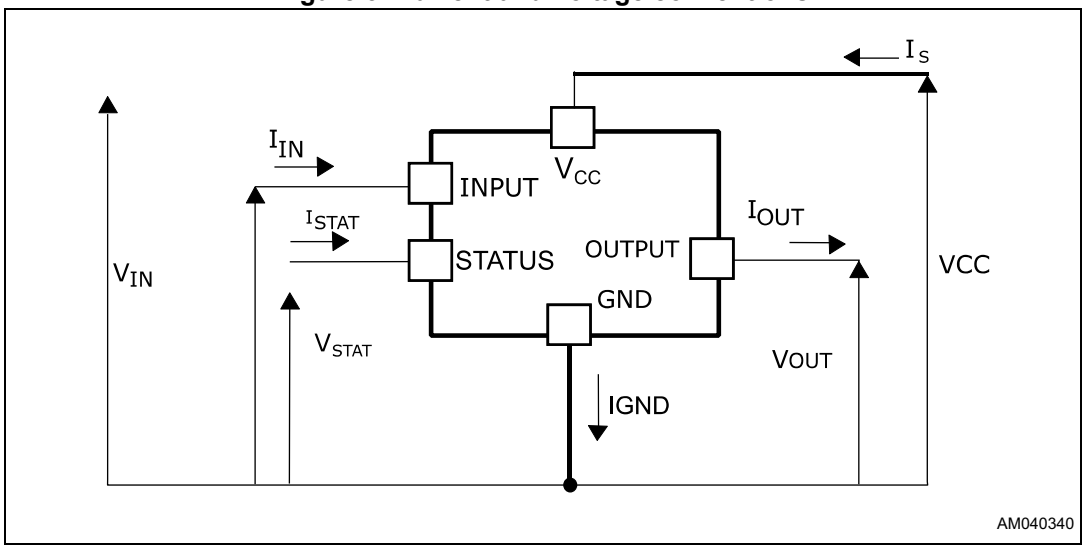


Figure 3. Current and voltage conventions



3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current -	5	A
I_{IN}	DC input current -	1 to +10	mA
I_{STAT}	DC status current -	1 to +10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	5000	V
E_{AS}	Single pulse avalanche energy (T_{amb} = 125 °C, V_{CC} = 24 V, I_{load} = 2.0 A)	5.5	J
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited	W
T_J	Junction operating temperature	Internally limited	°C
T_C	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Table 3. Thermal data

Symbol	Parameter		Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	Max.	3	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	Max.	50(1)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm2 of Cu (at least 35 μm) thick connected to all VCC pins.

4 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 4. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	-	5.5	-	36	V
$R_{DS(on)}$	On-state resistance	I_{OUT} = 2 A at T_J = 25 °C	-	60	-	mΩ
		I_{OUT} = 2 A	-		180	
I_S(1)	Supply current	OFF-state, V_{CC} = 24 V, T_J = 25 °C,	-	10	20	µA
		ON-state, V_{CC} = 24 V, T_J = 25 °C,	-	3.5	-	mA
		ON-state, V_{CC} = 24 V, T_J = 100 °C	-	-	3.8	mA
V_{USD}	Undervoltage shutdown	-	3	4	5.5	V
V_{OV}	Overvoltage shutdown	-	36	-	-	V
$I_{L(off)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0	-	10	µA

1. Status: floating.

Table 5. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn-on delay time	R_L = 12 Ω from V_{IN} rising edge to V_{OUT} = 2.4 V	-	12	-	µs
$t_{d(OFF)}$	Turn-on delay time of output current	R_L = 12 Ω from V_{IN} falling edge to V_{OUT} = 21.6 V	-	35	-	µs
$dV_{OUT}/dt_{(on)}$	Turn -on voltage slope	R_L = 12 Ω from V_{OUT} = 2.4 V to V_{OUT} = 19.2 V	-	0.80	-	V/µs
$dV_{OUT}/dt_{(off)}$	Turn -off voltage slope	R_L = 12 Ω from V_{OUT} = 21.6 V to V_{OUT} = 2.4 V	-	0.30	-	

Table 6. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level	-		1.25	-	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1	-	-	µA
V_{IH}	Input high level	-	3.25	-	-	V
I_{IH}	High level input current	V_{IN} = 3.25 V	-	-	10	µA
$V_{I(HYST)}$	Input hysteresis voltage	-	0.5	-	-	V
I_{IN}	Input current	V_{IN} = V_{CC} = 5 V	-	-	10	µA
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		II_{IN} = -1 mA	-	-0.7	-	

Table 7. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA	-	-	0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5 V	-	-	10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V	-	-	100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1 mA	6	6.8	8	µA
		I_{STAT} = -1 mA	-	-0.7	-	V

Table 8. Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{demag}	Turn-off output clamp voltage	R_L = 12 Ω; L = 6 mH	V_{CC} -47	V_{CC} -52	V_{CC} -57	V
T_{TSD}	Shutdown temperature	-	150	175	200	°C
I_{lim}	Current limitation	V_{CC} = 24 V; R_{LOAD} = 10 mΩ, t = 0.4 ms	2.7	-	6.0	A
T_{hyst}	Thermal hysteresis	-	7	20	-	°C
T_R	Reset temperature	-	135	-	-	°C

5 Test circuits

Figure 4. Peak short-circuit current

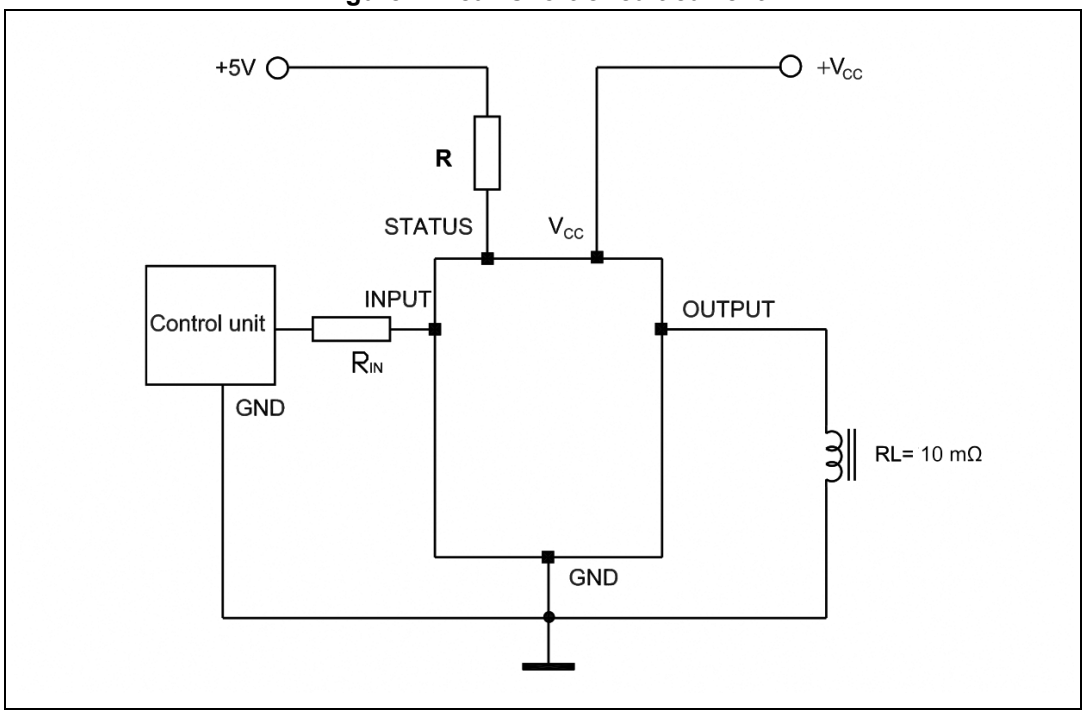
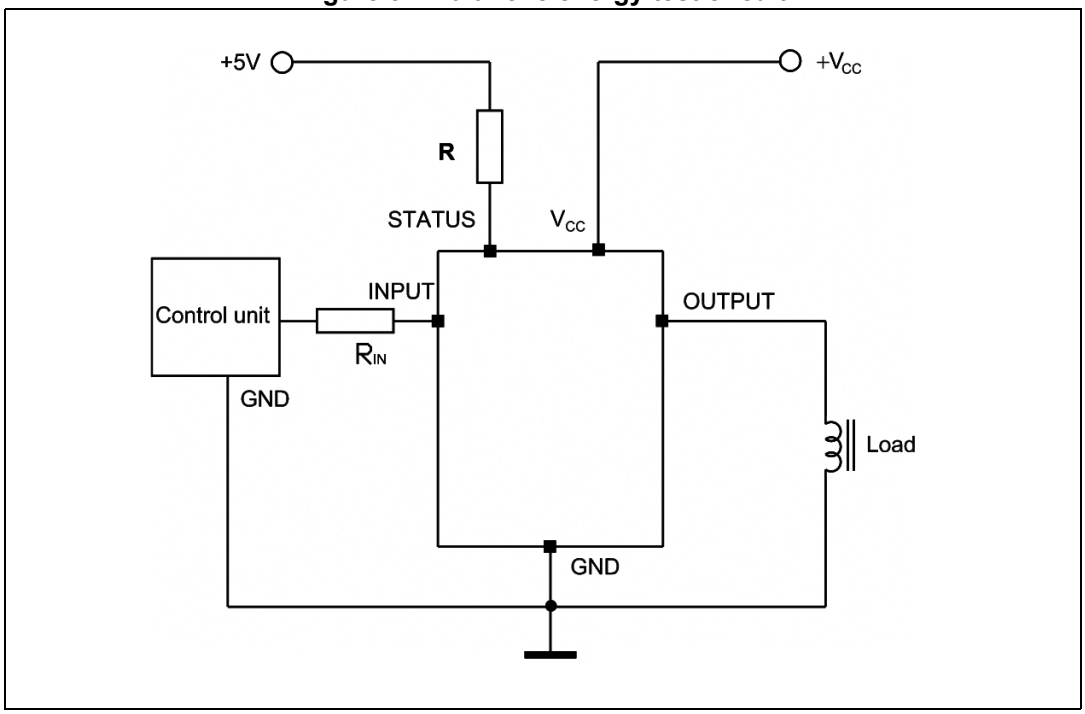


Figure 5. Avalanche energy test circuit



6 Switching time waveforms and truth table

Figure 6. Switching time waveforms

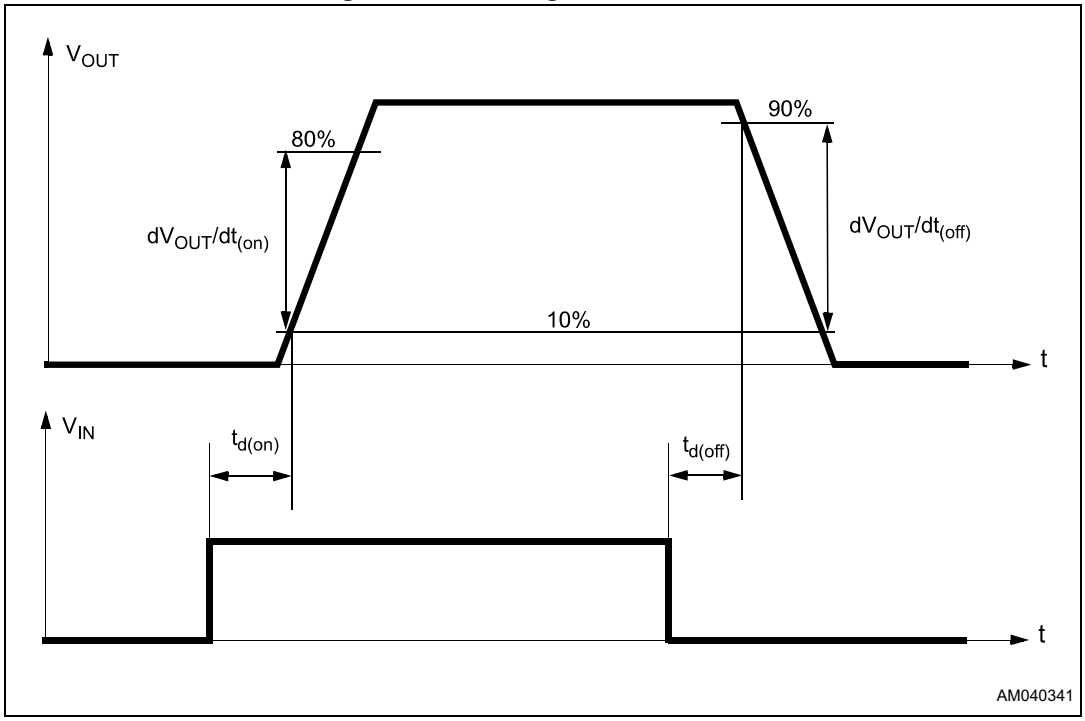
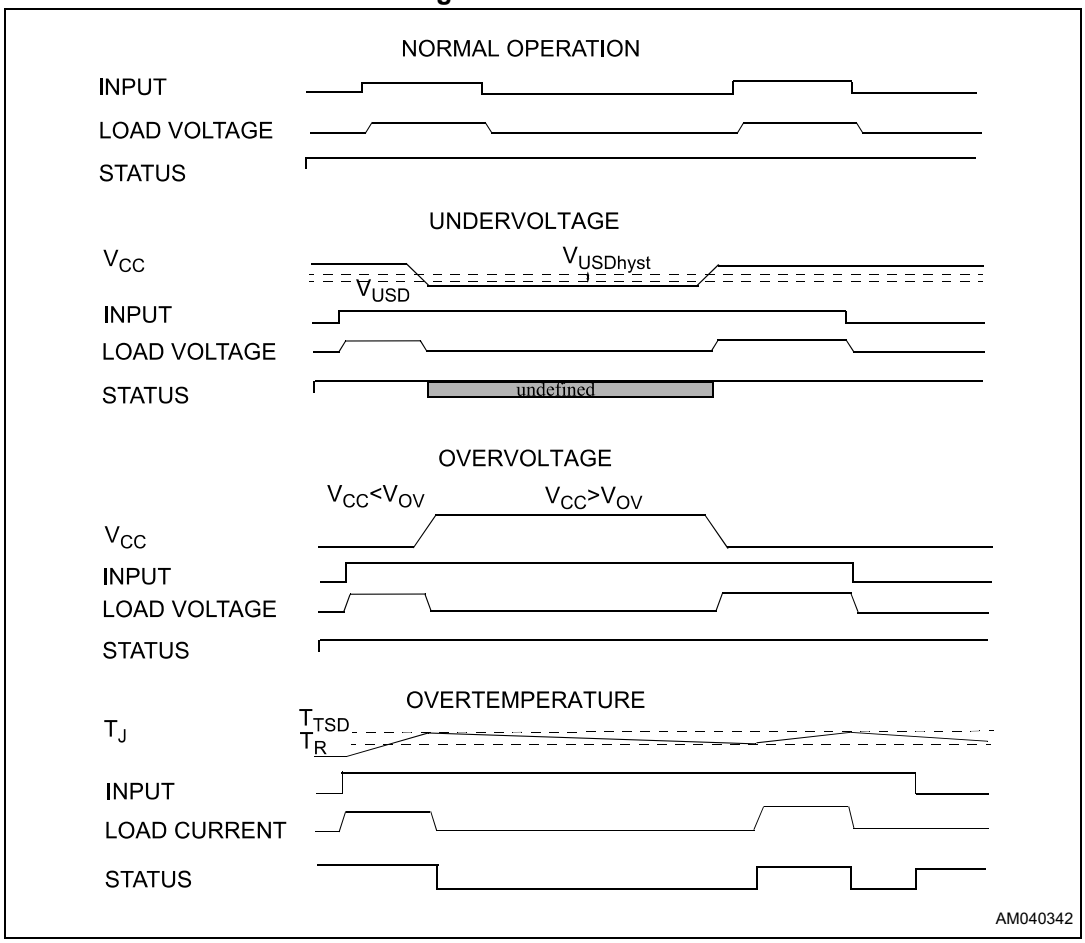


Table 9. Truth table

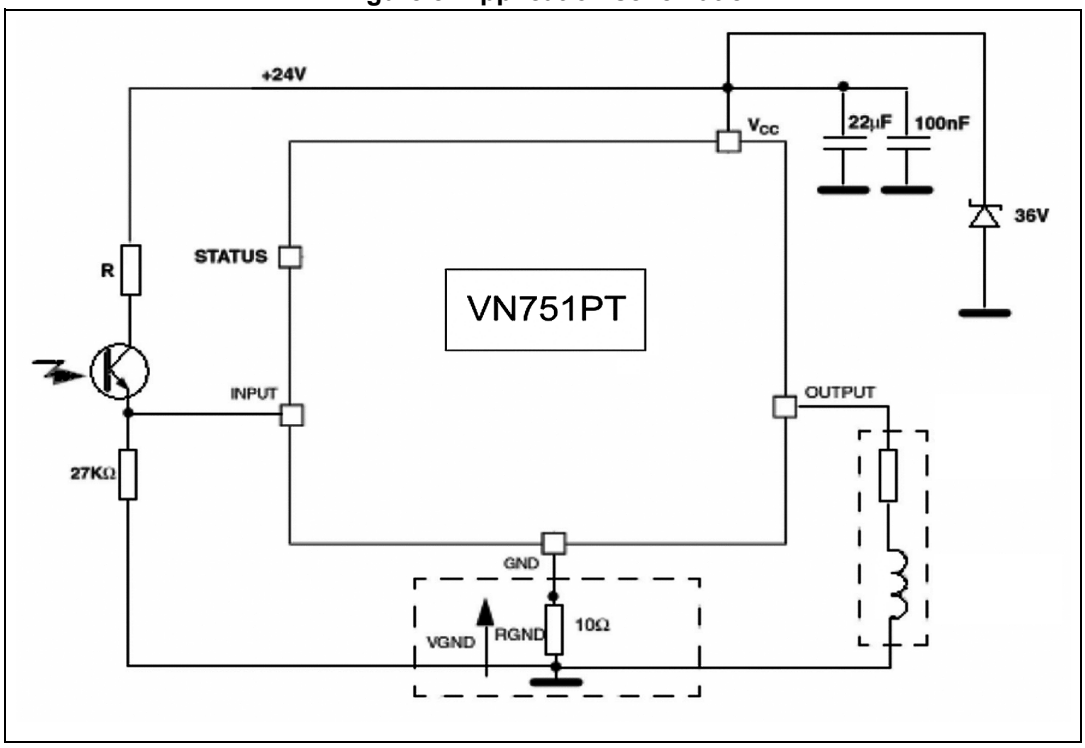
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	($T_J < T_{TSD}$) H
	H	X	($T_J > T_{TSD}$) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Figure 7. Waveforms



7 Application schematic

Figure 8. Application schematic



8 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC. The R_{GND} resistor value can be selected according to the following conditions:

Equation 1

$$R_{GND} \leq 600\ mV / (I_S \text{ in ON-state max.})$$

Equation 2

$$R_{GND} \geq (-V_{CC}) / (-I_{GND})$$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

The power dissipation associated to R_{GND} during reverse polarity condition is:

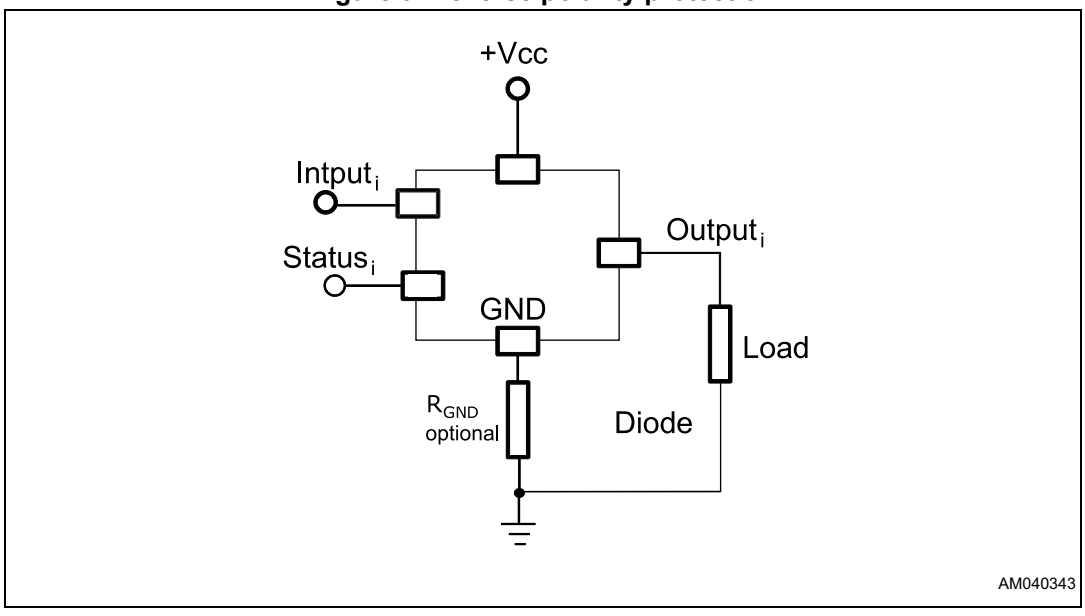
Equation 3

$$P_D = (-V_{CC})2 / R_{GND}$$

This resistor can be shared by several different ICs.

In such case I_S value in *Equation 1* is the sum of the maximum ON-state currents of the different devices. Please note that if the microprocessor ground and the device ground are separated, the voltage drop across the R_{GND} (given by I_S in ON-state max. * R_{GND}) produces a difference between the generated input level and the IC input signal level. This voltage drop varies depending on how many devices are ON in case of several high-side switches sharing the same R_{GND}.

Figure 9. Reverse polarity protection



9 Active VDS clamp

Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage is detected on output.

The OUT pin is pulled down to V_{demag}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at about V_{demag} until the load energy has been dissipated. The energy is dissipated both in IC internal switch and in load resistance.

Figure 10. Active clamp equivalent principle schematic

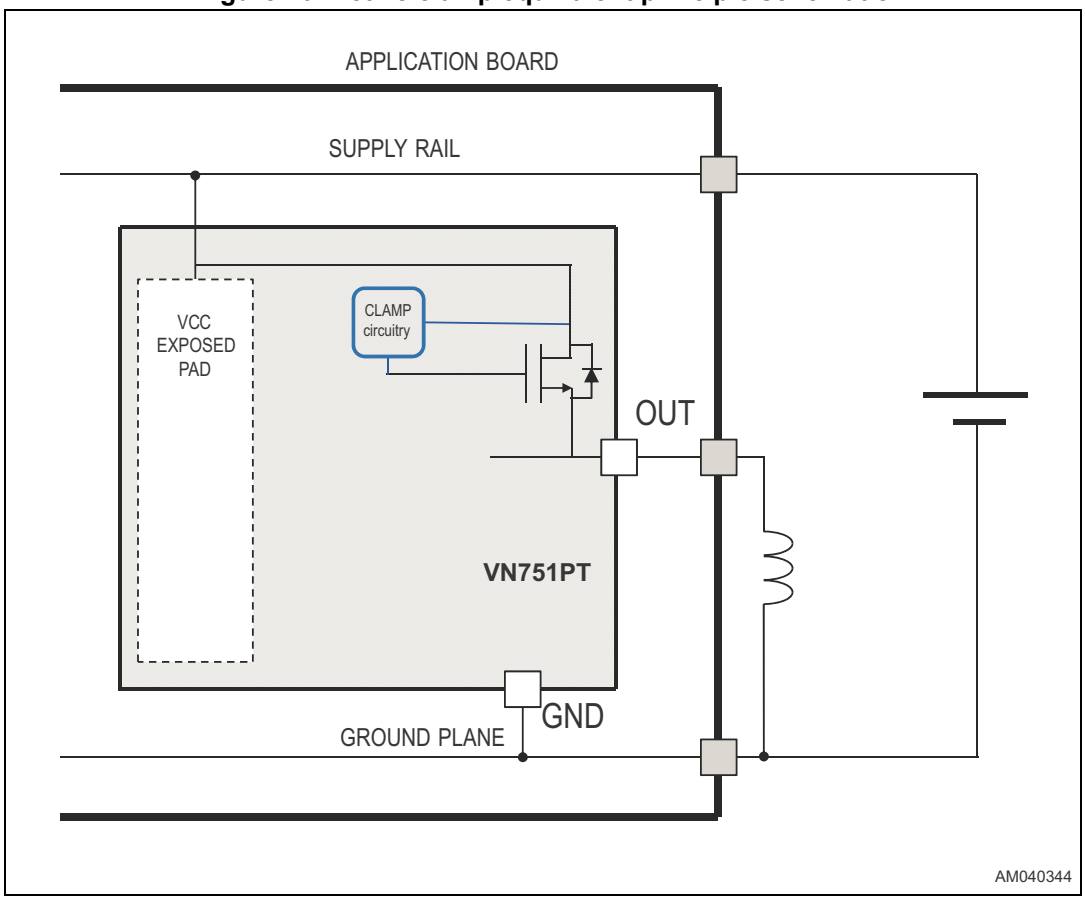
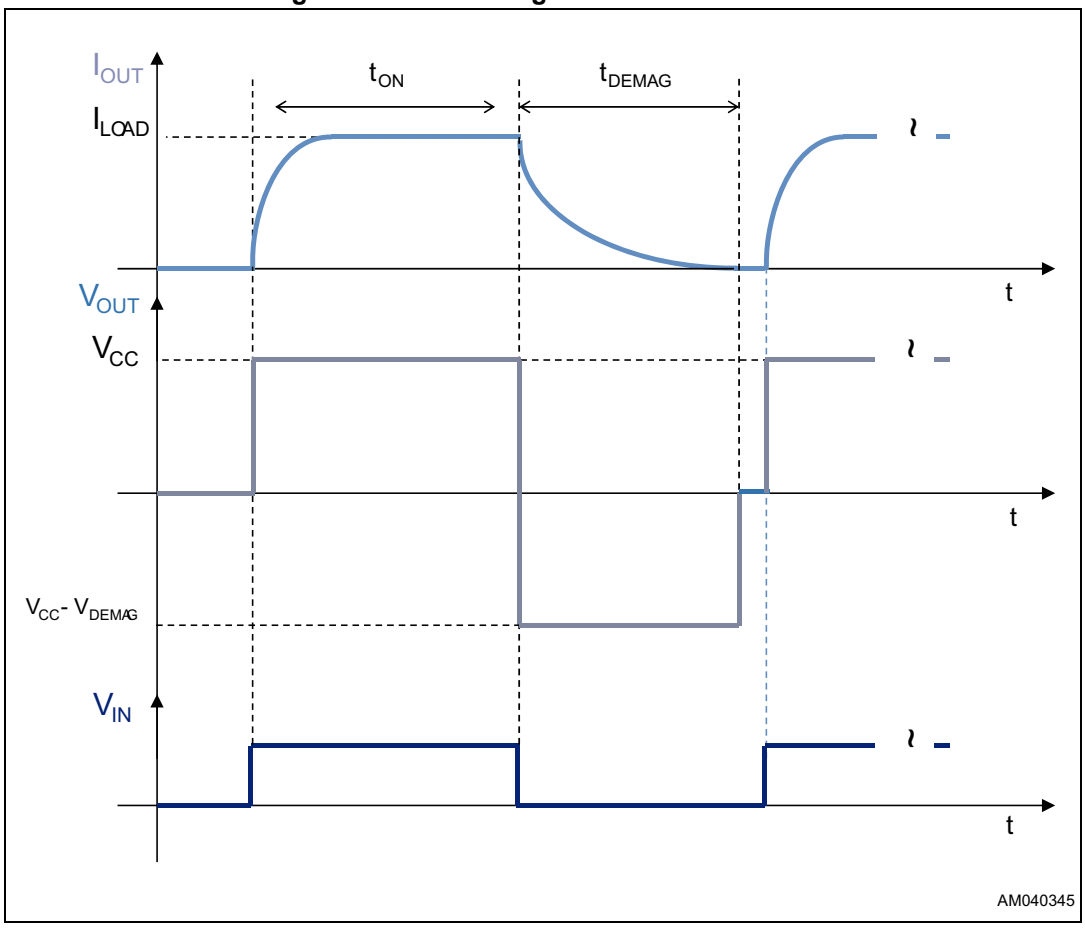
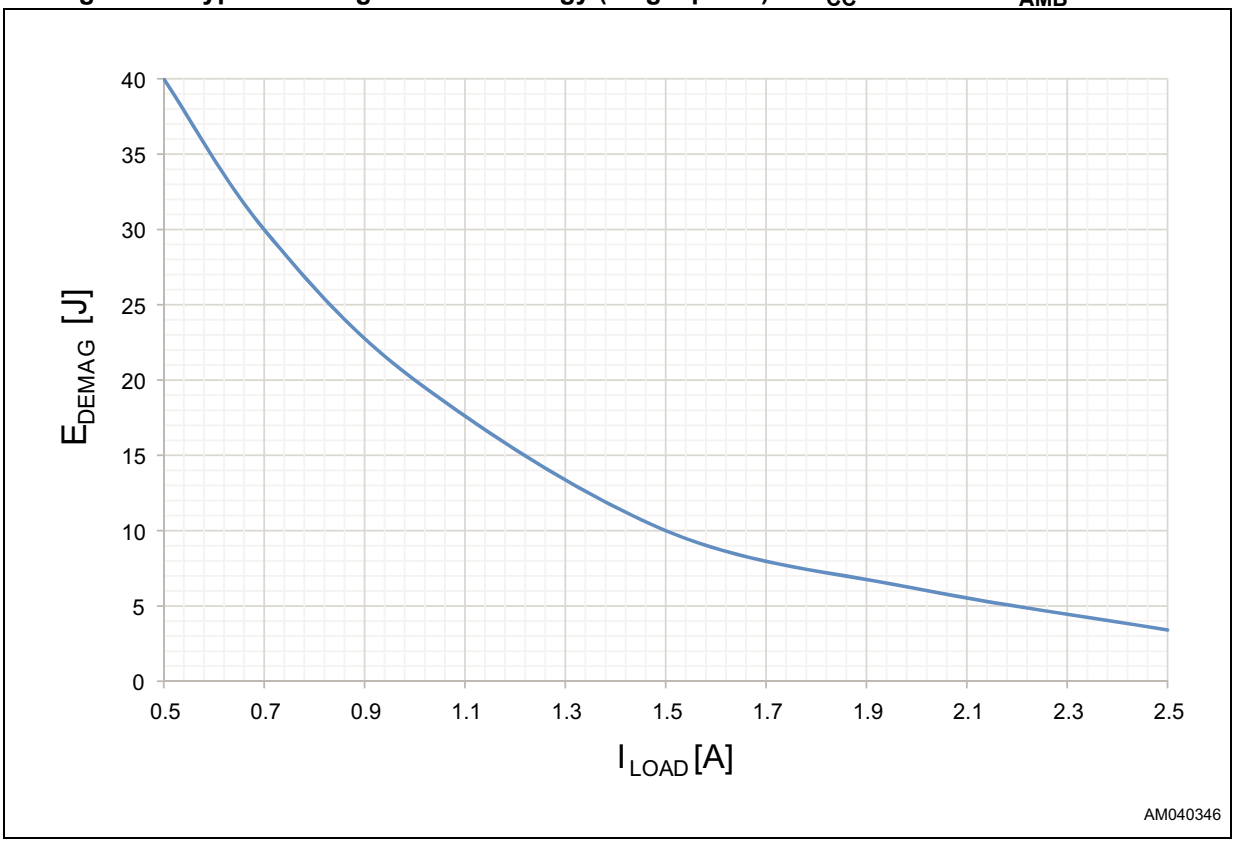


Figure 11. Fast demagnetization waveforms



The demagnetization of inductive load causes a huge electrical and thermal stress to the IC. The curve plotted below shows the maximum demagnetization energy that the IC can support in a single demagnetization pulse with V_{CC} = 24 V and T_{AMB} = 125 °C. If higher demagnetization energy is required then an external free-wheeling Schottky diode has to be connected between OUT (cathode) and GND (anode) pins. Note that in this case the fast demagnetization is inhibited.

Figure 12. Typical demagnetization energy (single pulse) at V_{CC} = 24 V and T_{AMB} = 125 °C

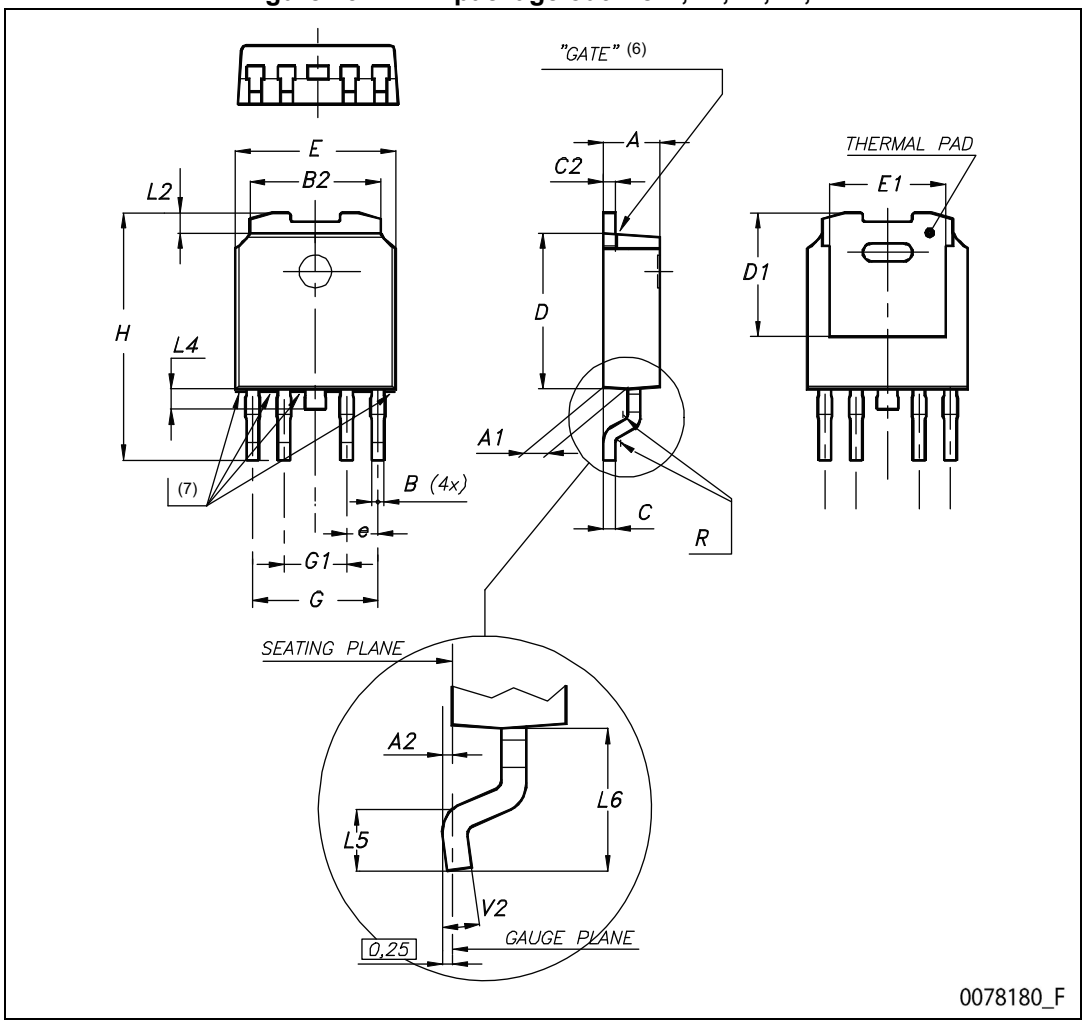


10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 PPAK package information

Figure 13. PPAK package outline(1), (2), (3), (4), (5)



1. Burrs larger than 0.25 mm are not allowed on the upper surface of the dissipater (FRONT). On the lower surface (REAR) the maximum allowed is: 0.05 mm.
2. The side of the dissipater to be connected to the external dissipater must be flat within 30 micron.
3. The leads size is comprehensive of the thickness of the leads finishing material.
4. Package outline exclusive of any mold flashes dimensions.
5. Package outline exclusive of metal burrs dimensions.
6. Max. resin gate protrusion: 0.5 mm.
7. Max. resin protrusion: 0.25 mm.

Table 10. PPAK package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	2.2	-	2.4
A1	0.9	-	1.1
A2	0.03	-	0.23
B	0.4	-	0.6
B2	5.2	-	5.4
C	0.45	-	0.6
C2	0.48	-	0.6
D	6	-	6.2
D1	-	5.1	-
E	6.4		6.6
E1	-	4.7	-
e	-	1.27	-
G	4.9	-	5.25
G1	2.38	-	2.7
H	9.35	-	10.1
L2		0.8	1
L4	0.6	-	1
L5	1	-	-
L6	-	2.8	-
R	-	0.20	-
V2	0°	-	8°

10.2 PPAK packing information

Figure 14. PPAK tape outline

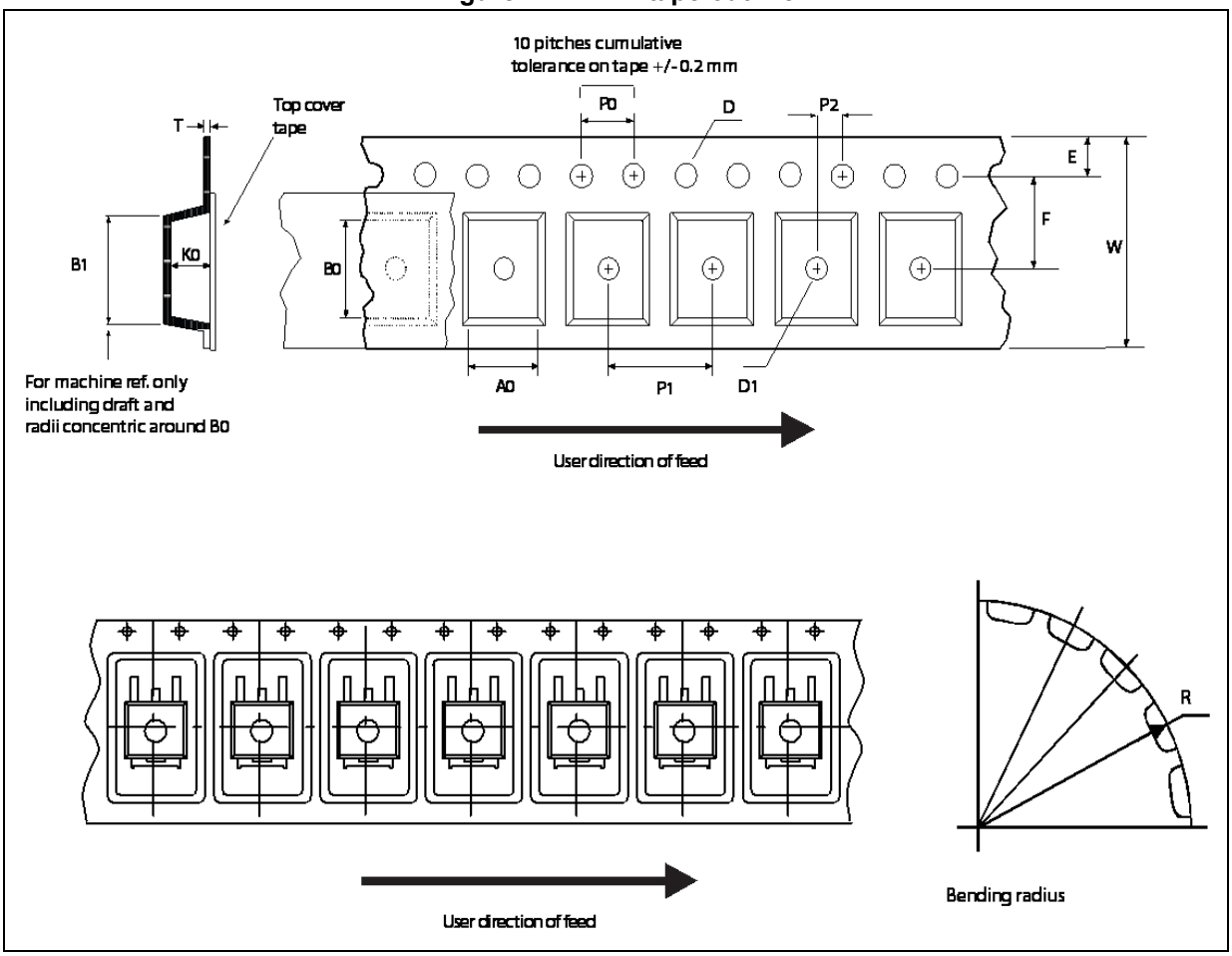


Figure 15. PPAK reel outline

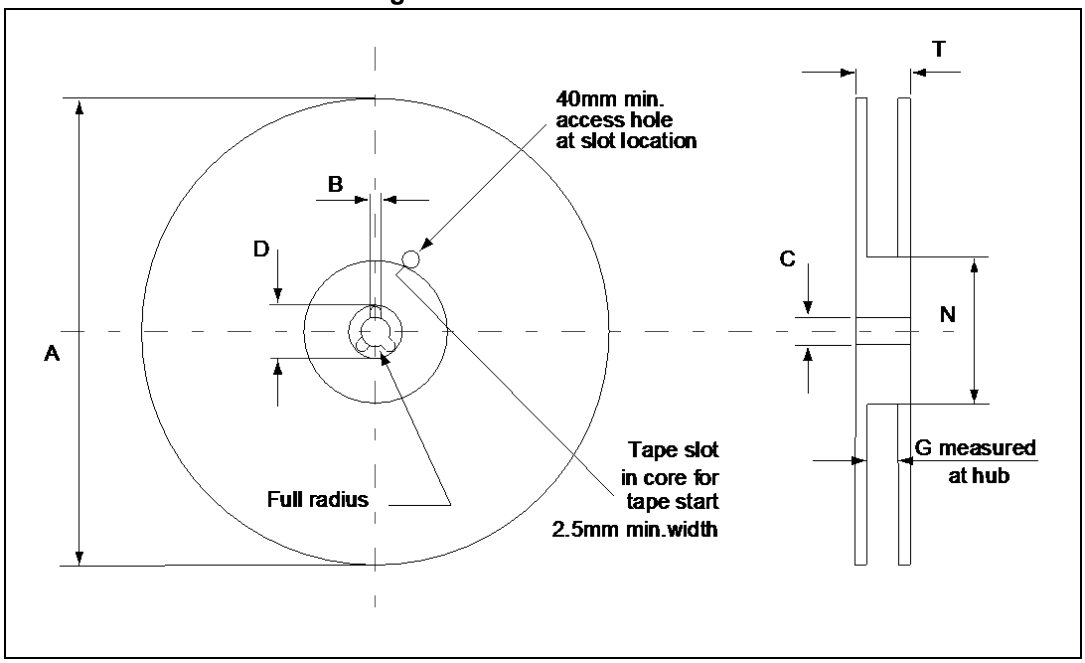


Table 11. PPAK tape and reel mechanical data

Tape			Reel		
	Dimensions (mm)		Dimensions (mm)		
Symbol	Min.	Max.	Symbol	Min.	Max.
A0	6.8	7	A	-	330
B0	10.4	10.6	B	1.5	-
B1	-	12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	-
D1	1.5	-	G	16.4	18.4
E	1.65	1.85	N	50	-
F	7.4	7.6	T	-	22.4
K0	2.55	2.75	-	-	-
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1	-	-	-
R	40	-	-	-	-
T	0.25	0.35	-	-	-
W	15.7	16.3	-	-	-

11 Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Mar-2006	1	Initial release.
31-Mar-2006	2	Added V_{SCL}.
10-Jul-2006	3	Updated V_{CC} value *table 1*, I_{lim} min. value *table 7*.
12-Mar-2007	4	Typo in *table 4*, updated P_{tot} value *table 1*.
15-May-2007	5	Typo in *table 1*, V_{ESD}.
18-Sep-2007	6	Added I_{STAT} value in *table 1*.
08-Jul-2008	7	Added *section 7*.
30-Nov-2009	8	Updated *cover page* and *section 6*.
12-Jul-2016	9	Updated *Table 4: "Power"*.
09-May-2018	10	Updated *Section : Features on page 1*. Updated *Table 2 on page 7* (updated E_{AS} parameter and value). Updated *Figure 8 on page 13* (removed output values). Added *Section 9 on page 15*. Added notes below *Figure 13 on page 18*. Minor modifications throughout document.