

## Description

The 60N06 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

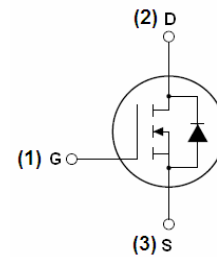
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$V_{DSS}$	$R_{DS(ON)}$ @4.5V(Typ)	$R_{DS(ON)}$ @10V(Typ)	$I_D$
60V	18 m $\Omega$	14 m $\Omega$	60A

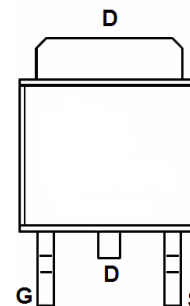
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

## Application

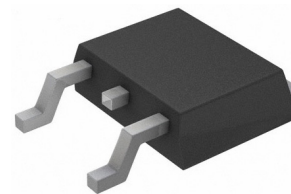
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252

## Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	60	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	42	A
Pulsed Drain Current	$I_{DM}$	200	A
Maximum Power Dissipation	$P_D$	85	W
Derating factor		0.57	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	300	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ\text{C}$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.8	°C/W
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## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.75	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	14	20	m $\Omega$
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=20A$	-	18	24	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=20A$	18	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2050	-	PF
Output Capacitance	$C_{oss}$		-	158	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	120	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=6.7\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	7.4	-	nS
Turn-on Rise Time	$t_r$		-	5.1	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	28.2	-	nS
Turn-Off Fall Time	$t_f$		-	5.5	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=30V, I_D=20A,$ $V_{GS}=10V$	-	50	-	nC
Gate-Source Charge	$Q_{gs}$		-	6	-	nC
Gate-Drain Charge	$Q_{gd}$		-	15	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	50	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	28	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	40	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

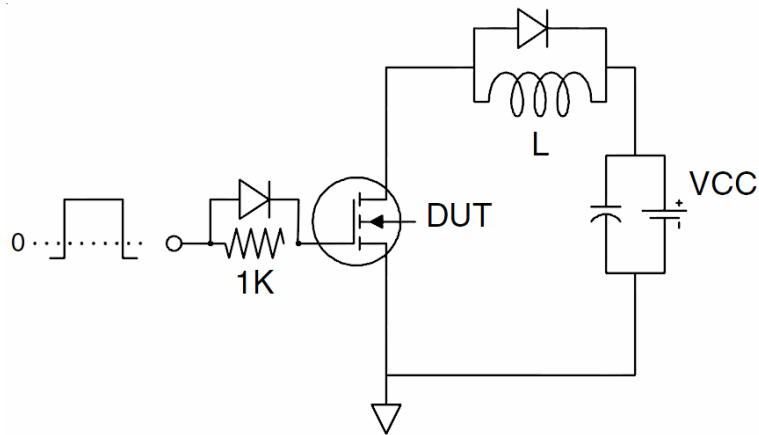
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^\circ\text{C}, V_{DD}=30V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

## Test Circuit

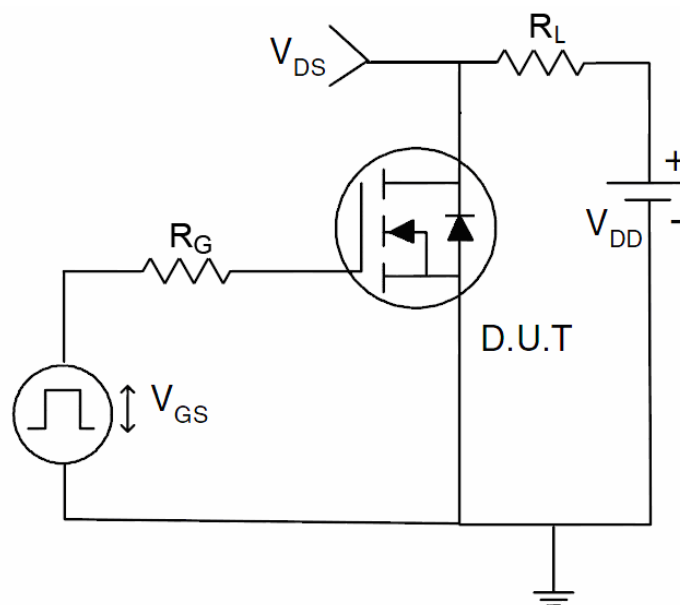
### 1) $E_{AS}$ test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

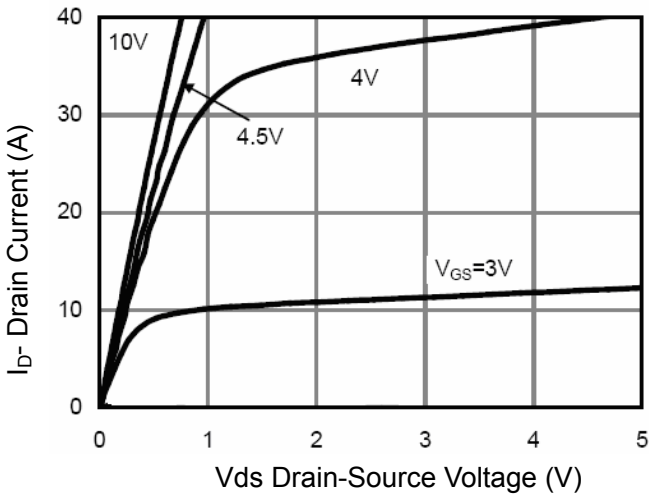


Figure 1 Output Characteristics

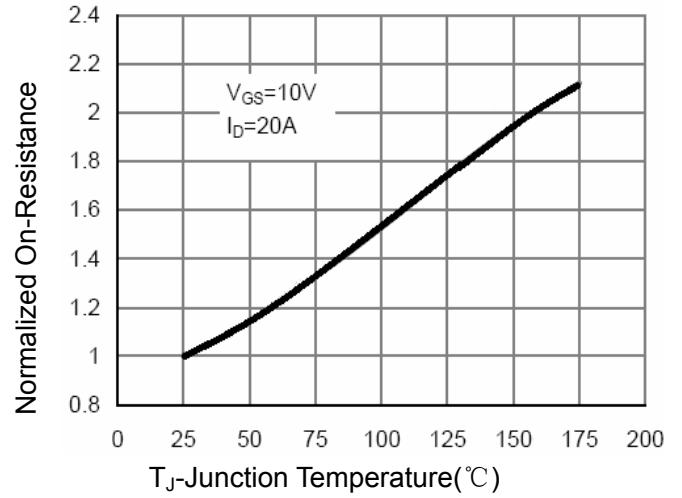


Figure 4 Rds(on)-Junction Temperature

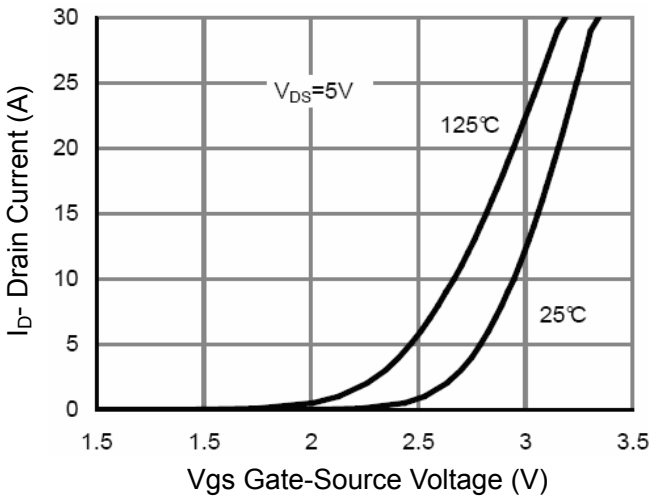


Figure 2 Transfer Characteristics

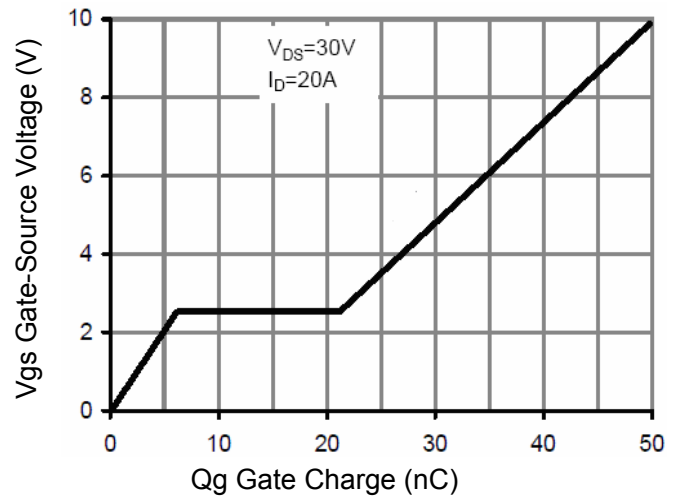


Figure 5 Gate Charge

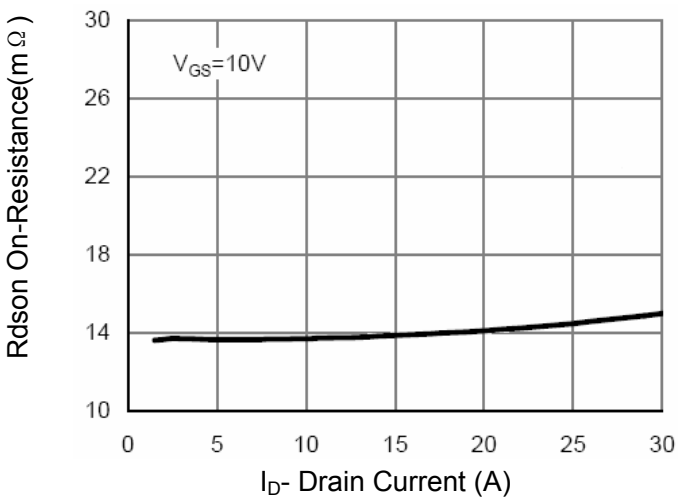


Figure 3 Rds(on)- Drain Current

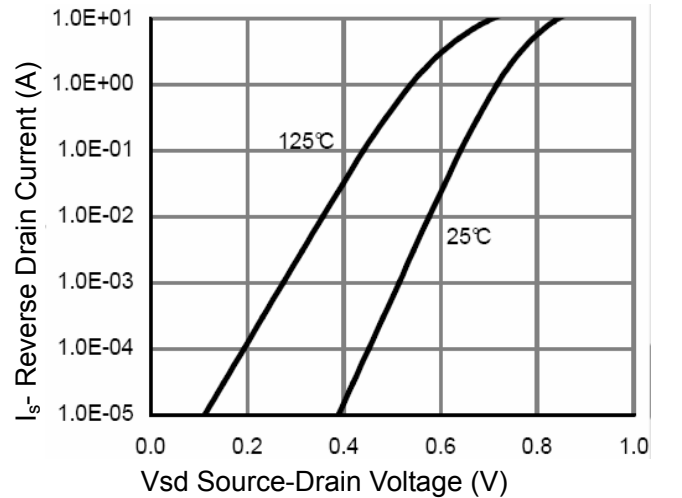


Figure 6 Source- Drain Diode Forward

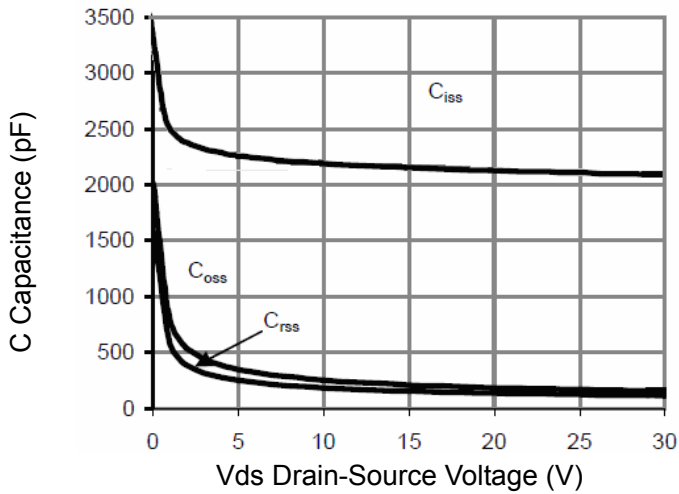


Figure 7 Capacitance vs Vds

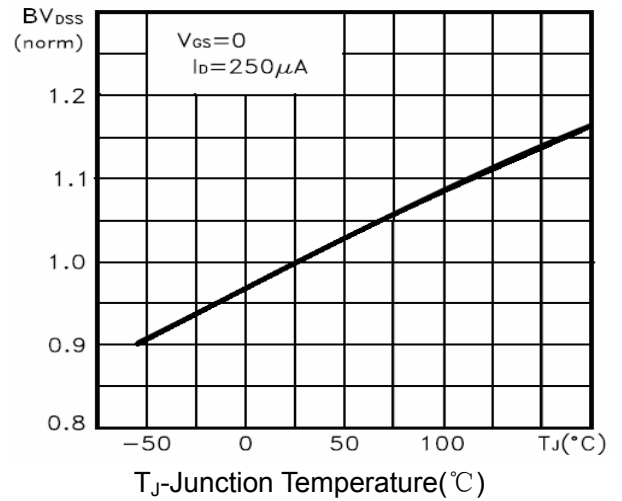


Figure 9  $BV_{DSS}$  vs Junction Temperature

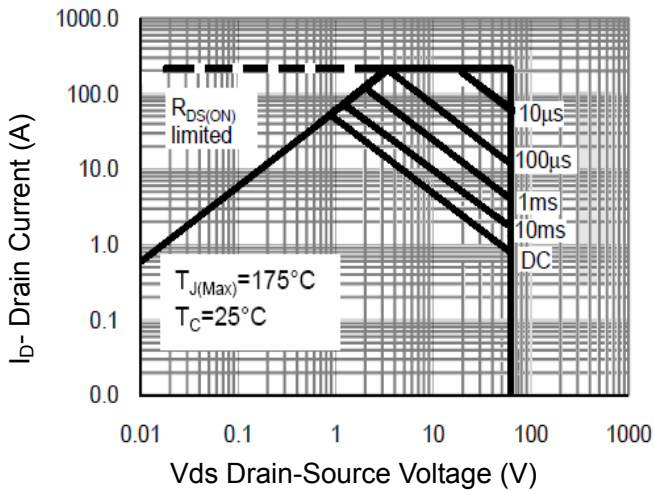


Figure 8 Safe Operation Area

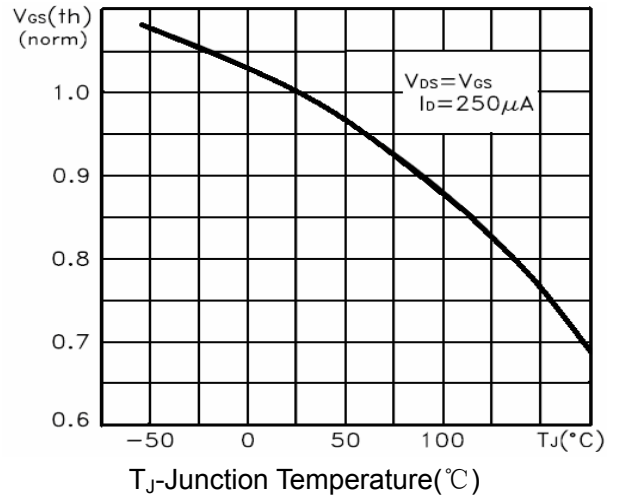


Figure 10  $V_{GS(th)}$  vs Junction Temperature

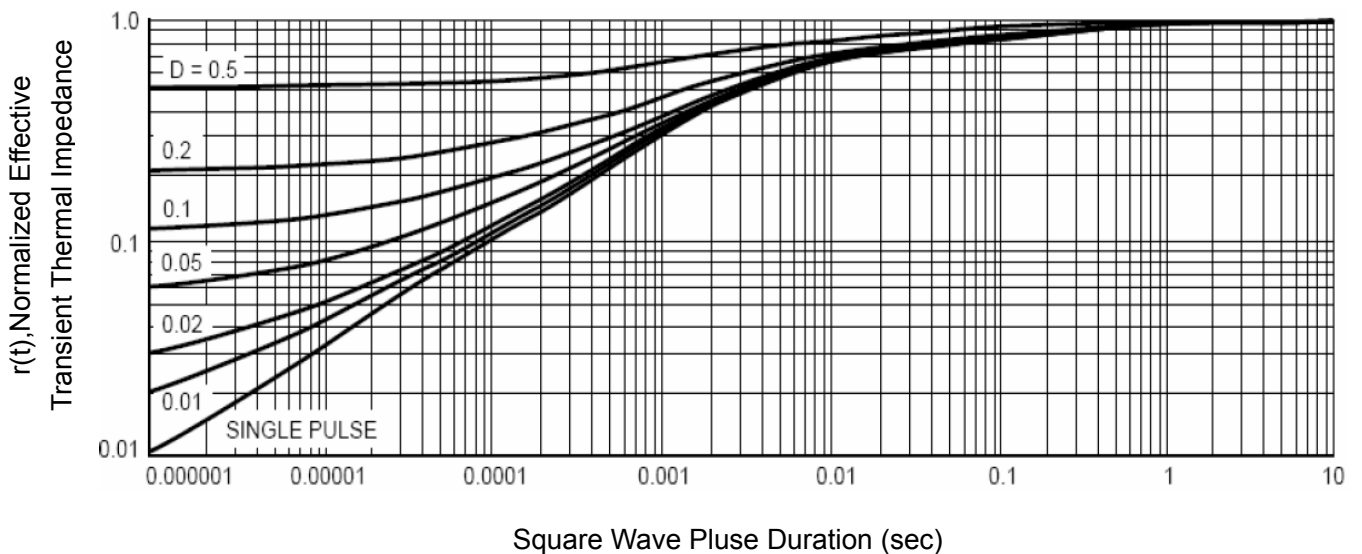


Figure 11 Normalized Maximum Transient Thermal Impedance