



Applications Note: SY5868

Dimming Interface Converter

Compatible With 0/1~10V Dimming Resistor Dimming And PWM Dimming

Adaptive LED Current Filter

General Description

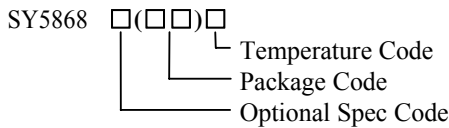
SY5868 integrate a dimming interface converter whose input signal can be a 0/1~10V dimming signal, resistor, or PWM signal. It recognizes the signal automatically. The final output of SY5868 is a PWM signal which is used to control a dimmable CC regulator or drive an opto-coupler to achieve isolated dimming. The frequency of output PWM signal and the source current to drive passive 0~10V dimmer/Resistor can be set by external capacitor and resistor.

SY5868 integrates an LED current remover to eliminate low frequency current ripple, which is compatible with dimming. It adopts adaptive control scheme and no additional electrical design is needed.

Features

- Compatible with 0/1~10V Dimming, Resistor Dimming and PWM Dimming.
- Recognize Different Dimming Signal Automatically.
- Integrate a 60V LDO Module to Simplify External Circuit.
- The Source Current for Passive 0~10V Dimmer Can Be Set.
- The Frequency of Output Can Be Set.
- Current Filter for Single Stage LED Driver to Eliminate Current Remover
- Current Remover Suitable for Dimming Application.
- External MOS for Different Output Specification.
- Compact Package: SO14

Ordering Information



Applications

- LED Lighting

Ordering Number	Package type	Note
SY5868FKC	SO14	----

Typical Applications

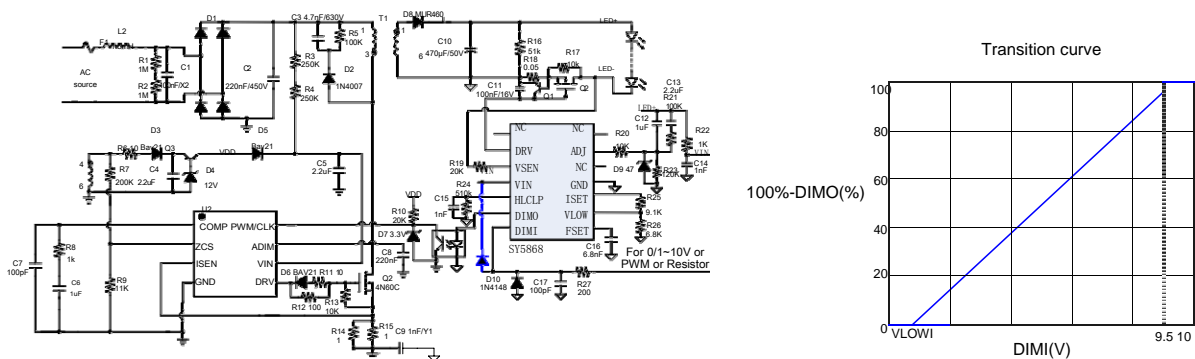
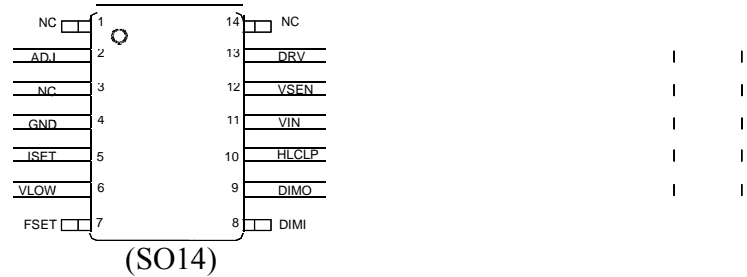


Fig.1 High clamp mode application Schematic

Pinout (top view)



Top Mark: **BPU**xyz, (Device code: BPU; x=year code, y=week code, z= lot number code)

Pin Name	Pin number	Pin Description
NC	1	No connect.
ADJ	2	Average Voltage of Drain setting pin. This pin receives ripple info to regulate the output.
NC	3	No connect.
GND	4	Ground pin.
ISET	5	Source current setting pin. V_{ISET} is a 1.5V voltage source. This pin is used to set the source current of DIMI pin for passive dimmer or resistor. $I_{DIMI} = \frac{5 \times 1.5}{R_{ISET}}$
VLOW	6	The lowest input setting pin. This pin is used to set the lowest input voltage which corresponds to 0% duty. The real minimum 0~10V input is $V_{LOWI} = 1.55 \cdot V_{LOW} - 0.726$
FSET	7	Dimming frequency setting pin. This pin is used to set the frequency of DIMO pin. $f_{DIM} = \frac{30\mu}{(6.6 - V_{LOW}) \cdot C_{FSET}}$
DIMI	8	Dimming input pin. Dimming signal is connected to this pin. It maybe is a 0/1~10 analog signal, resistor or a PWM signal.
DIMO	9	Dimming output pin. This pin will output a PWM signal to driver opto-coupler for separation dimming.
HLCLP	10	High clamp and low clamp setting pin. If the voltage of HLCLP pin is larger than 100mV during IC start-up, it enters into low clamp mode, else it works in high clamp mode. In low clamp mode, if V_{DIMI} is less than the setting value, it is clamped internally. $V_{LCLP} = \frac{9.3}{2} \cdot (V_{HLCLP} - 0.2) + 0.2$ In High clamp mode, the clamp voltage is 9.5V fixedly, and the resistor connected to HLCLP is used to adjust the max duty. $D_{MAX} = \frac{67.79 \cdot R_{HCLP}}{67.43 \cdot R_{HCLP} + 770.59}$ For Example $R_{HCLP} = 510k \text{ ohm}$

		$D_{MAX} = \frac{67.79 \cdot 510}{67.43 \cdot 510 + 770.59} = 98.3\%$
VIN	11	Power supply pin. This pin provides power supply for IC.
VSEN	12	LED negative sample pin. This pin receives negative node of LED waveform
DRV	13	Gate driver pin. Connect this pin to the gate of primary MOSFET.
NC	14	No connect.

Block Diagram

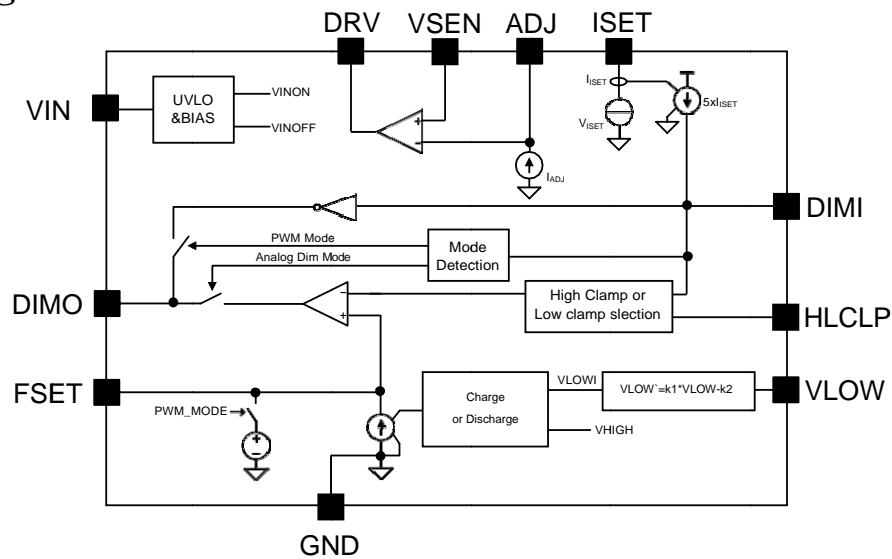


Fig.3 Block Diagram

Absolute Maximum Ratings (Note 1)

VIN	-----	-0.3V~60V
ADJ, VSEN, DRV	-----	-0.3V~20V
ISET, FSET, VLOW, HLCLP	-----	-0.3V~3.6V
DIMI, DIMO	-----	0.3V~20V
Power Dissipation, @ TA = 25°C SO 14	-----	1.3W
Package Thermal Resistance (Note 2)		
SO14, θ_{JA}	-----	94°C/W
SO14, θ_{JC}	-----	52°C/W
Maximum Junction Temperature	-----	125°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C

Recommended Operating Conditions

VIN	-----	V~55V
Junction Temperature Range	-----	40°C to 125°C



Electrical Characteristics

($V_{IN} = 15V$, $T_A = 25^\circ C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Voltage Range	V_{VIN}		V_{VIN_ON}		55	V
VIN Turn-on Threshold	V_{VIN_ON}		8.4	9.2	10.2	V
VIN Turn-off Threshold	V_{VIN_OFF}			$V_{VIN_ON}-1.3$		V
VIN Shunt Voltage	V_{VIN_SHUNT}		52	55	59	V
DIMI Section						
Range of Minimum Dimming Voltage	V_{LOW_Range}		0		V_{ISET}	V
Ref Voltage of ISET	V_{ISET}		1.44	1.5	1.56	V
MAX DIMI Source Current	I_{SR_MAX}	ISET=3.75K	1.85	2	2.15	mA
Maximum Dimming Voltage	V_{HIGH}		9.2	9.5	9.81	V
Max Duty of PWM	D_{PWM_MAX}			99(note 3)		%
PWM ON Voltage Threshold	V_{PWM_ON}		2.3			V
PWM OFF Voltage Threshold	V_{PWM_OFF}				0.8	V
PWM Frequency Range	F_{PWM}		400		10k	Hz
Current Remover Section						
ADJ Output Current	I_{ADJ}		9.5	10.5	11.5	μA
Thermal Section						
Thermal Shut Down Temperature	T_{SD}			145		$^\circ C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: If peak voltage of PWM signal is higher than 10V, It is no problem. But if the peak is 3.3V, 100% duty input may be recognized as 0~10V signal mistakenly.

Operation

SY5868 integrate a dimming interface converter whose input signal can be a 0/1~10V dimming signal, resistor, or PWM signal. It recognizes the signal automatically.

When input signal is 0/1~10V dimming signal, It will be converted into a PWM signal to driver opto-coupler or dimmable IC.

When input signal is a resistor, there is a current flowing out from DIMI pin to produce a voltage at the resistor. Then It works as same as 0/1~10V dimming input.

When input signal is a PWM signal, it is converted into a reverse PWM signal.

There are two working modes.

Low-clamp is used to clamp the minimum duty cycle.

High-clamp is used to clamp the maximum duty cycle.

More detail information is discussed below.

Also, it integrates a current remover for ripple-free application.

Applications Information

Start up

Supposing DIMI is floating.

DIMO follow VIN before VIN reach V_{IN_ON} . After reaching V_{IN_ON} , IC begin to work and DIMO is regulated by DIMI.

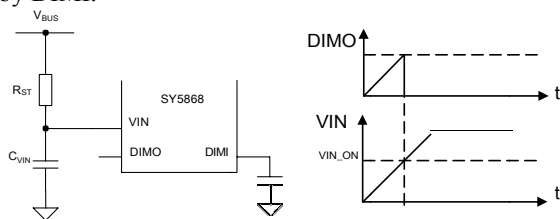


Fig.4 Start up

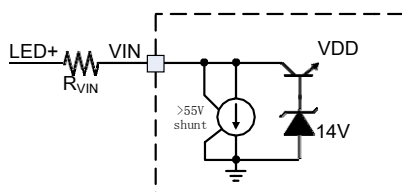


Fig.5 internal LDO

IC integrates a 60V LDO for simplifying peripheral device.

There is a shunt current if VIN voltage is larger than 55V which helps to protect IC when power voltage is high than 55V.

2. Dimming Input

(1) 0/1~10V Dimming

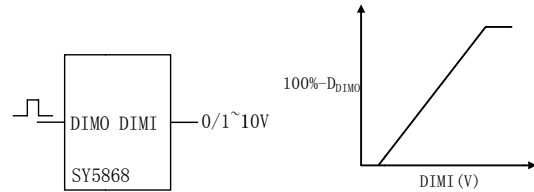


Fig.6 0/1~10V Dimming

If input signal of DIMI pin is 0/1~10V, it is converted into reversed duty signal.

(2) Resistor Dimming

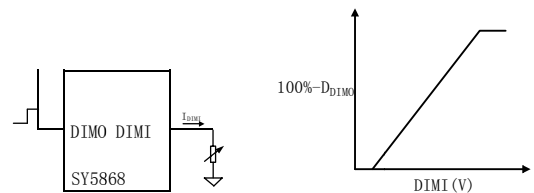


Fig.7 Resistor Dimming

If DIMI is connected with a variable resistor, there is a current flow from DIMI pin to drive the resistor and produce 0~10V signal. Also, the current exists in 0/1~10V dimming application.

(3) PWM Dimming

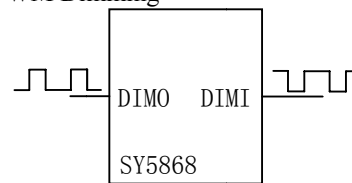


Fig.8 PWM Dimming

If input dimming signal is PWM signal, IC converts it into a reversed PWM signal.

3. Working Mode

(1) High clamp mode

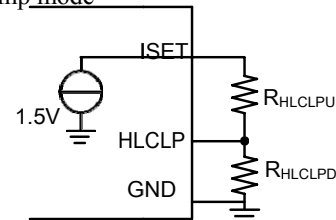


Fig.9 High clamp mode setting

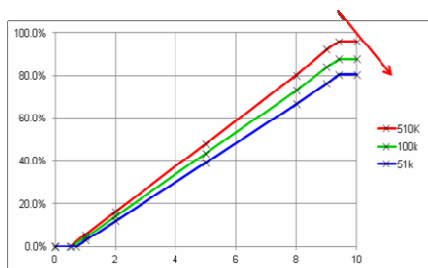


Fig.10 High clamp mode design result

As showed above, High clamp mode is used to set the maximum duty which can regulate the full load current in some special application.

If the voltage of HLCLP pin is less than $V_{HLCLP,MODE}$ when V_{IN} firstly reach V_{VIN_ON} , the high clamp mode is selected. To ensure IC enters into high clamp mode, R_{HLCLPU} should not be connected.

The turning point of DIMI is always 9.5V, and the maximum duty can be calculated by the following formula.

$$D_{MAX} = \frac{1}{2.2 - 0.2} \cdot \left(\frac{(9.5 - 0.2) \cdot \frac{14.58 \cdot R_{HLCLPD}}{14.58 + R_{HLCLPD}}}{14.58 + R_{HLCLPD}} + 52.85 \right)$$

Or

$$D_{MAX} = \frac{67.79 \cdot R_{HLCLPD}}{67.43 \cdot R_{HLCLPD} + 770.59}$$

With different R_{HLCLPD} , the maximum duty is changed. The design result is showed above.

(2) Low Clamp Mode

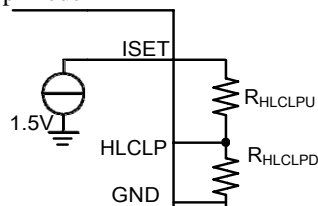


Fig.11 Low clamp mode setting

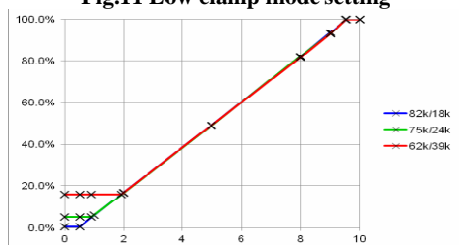


Fig.12 Low clamp mode design result

Low clamp mode is used to clamp the minimum duty as showed above.

If the voltage of HLCLP pin is larger than $V_{HLCLP,MODE}$ when V_{IN} reach V_{VIN_ON} , the low clamp mode is selected. To ensure IC enters into low clamp mode, please ensure:

$$\frac{V_{ISET} \cdot R_{HLCLPD}}{R_{HLCLPD} + R_{HLCLPU}} > V_{HLCLP,MODE} + 0.1$$

The turning point of DIMI pin is set by

$$V_{LCLP} = \frac{9.3}{2} \cdot (V_{HLCLP} - 0.2) + 0.2$$

$$= \frac{9.3}{2} \cdot \left(\frac{V_{ISET} \cdot R_{HLCLPD}}{R_{HLCLPU} + R_{HLCLPD}} - 0.2 \right) + 0.2$$

With different R_{HLCLPU} and R_{HLCLPD} , the minimum duty is set. The design result is showed above.

(3) Special low clamp mode

If there is no need to work in high clamp mode or low clamp mode, It can set by that:

$$V_{LCLP} = 0.2$$

It means that:

$$\frac{V_{ISET} \cdot R_{HLCLPD}}{R_{HLCLPU} + R_{HLCLPD}} = 0.2$$

4. Zero coordinate setting

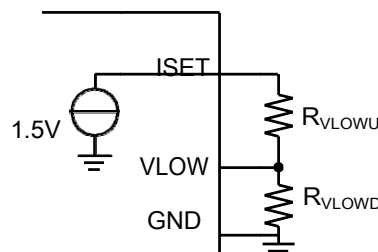


Fig.13 zero coordinate setting

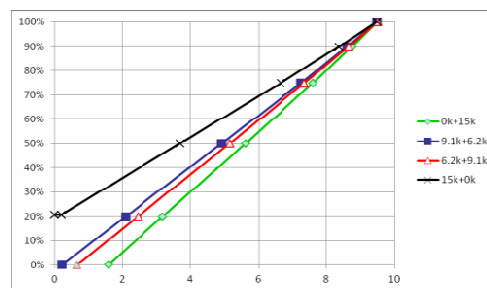


Fig.13 zero coordinate design result

Adjust the zero cross point of the curve by setting the voltage of VLOW. the formula is showed below.

$$V_{LOWI} = 1.55 \cdot k1 \cdot V_{LOW} - k1 \cdot 0.926 + 0.2$$

$k1$ is a compensation for high clamp mode.

$k1 = 1$; (Low clamp mode)

$$k1 = \frac{14.58}{52.85 + 14.58} \cdot \frac{52.85 + (14.58 // R_{HLCLPD})}{14.58 // R_{HLCLPD}} ; \text{(High clamp mode)}$$

If V_{LOWI} is less than 0.2V, the duty is clamped when $DIMI < 0.2V$.

And the V_{LOW} is set by:

$$V_{LOW} = \frac{V_{ISET} \cdot R_{VLOWD}}{R_{VLOWU} + R_{VLOWD}}$$

The design result is showed above.

5. Curve translation

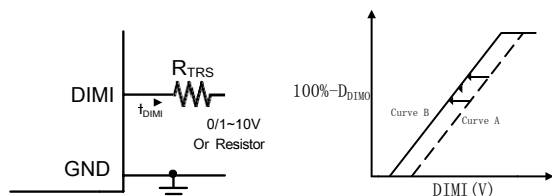


Fig.14 curve translation setting

To translate the converted curve, R_{TRS} is set. With greater R_{TRS} , converted curve is changed from A to B as showed above.

6. DIMI current set

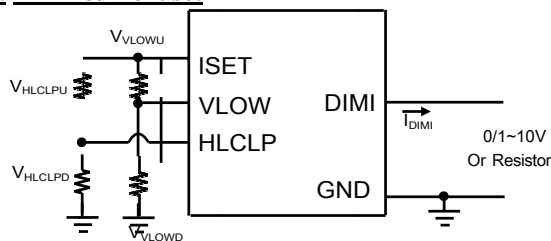


Fig.15 DIMI current setting

If the dimmer is passive device or a resistor, there should be a drive current to power the dimmer.

The current is set by:

$$I_{DIMI} = \frac{5 \times 1.5}{R_{ISET}}$$

$$R_{ISET} = (R_{HLCLPU} + R_{HLCLPD}) // (R_{VLOWU} + R_{VLOWD})$$

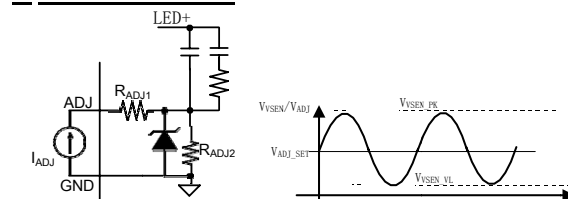
7. Frequency setting

There is a 20uA current charge or discharge FSET capacitor to produce a reference triangle wave.

The frequency is set by:

$$f_{DIM} = \frac{20\mu}{2 \cdot (2.2 - \frac{1}{3} \cdot V_{LOW}) \cdot C_{FSET}}$$

8. Current Remover



As showed above. V_{ADJ_SET} is set by R_{ADJ1} and R_{ADJ2} .

$$V_{ADJ_SET} = I_{ADJ} \cdot (R_{ADJ1} + R_{ADJ2})$$

It is recommended $V_{SEN_PK} < 4V$ and $V_{SEN_VL} > 0.3V$.

Design Example

A design example of typical application is shown below step by step.

Example A

#1. Identify design specification

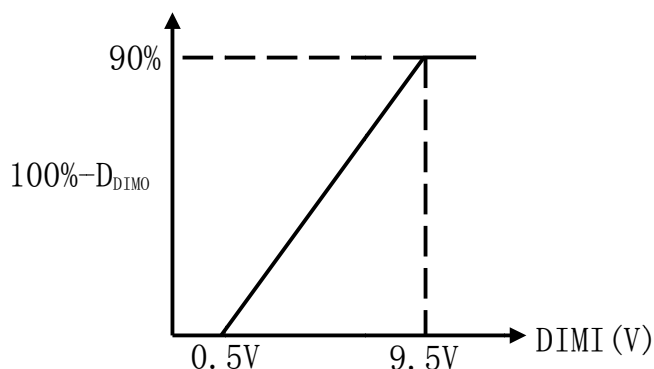


Fig.16 Target Curve

Target parameter			
I_{DIMI}	500uA	F_s	1kHz
V_{LOWI}	0.5	D_{MAX}	90%

(a). Mode Selection

As described above, high clamp mode is selected.

(b). D_{MAX} calculation

$$D_{MAX} = \frac{67.79 \cdot R_{HCLPD}}{67.43 \cdot R_{HCLPD} + 770.59} = 90\%$$

So,

$$R_{HCLPU} = NC$$

$$R_{HCLPD} = 97.6k \text{ ohm} \approx 100k \text{ ohm}$$

(c). V_{LOWI} calculation

$$k1 = \frac{14.58}{52.85 + 14.58} \cdot \frac{52.85 + (14.58 // R_{HLCLPD})}{14.58 // R_{HLCLPD}}$$

$$= 1.114$$

$$V_{LOWI} = 1.55 \cdot k1 \cdot V_{LOW} - k1 \cdot 0.926 + 0.2 = 0.5$$

$$V_{LOW} = \frac{V_{ISET} \cdot R_{VLOWD}}{R_{VLOWU} + R_{VLOWD}} = 0.771$$

So,

$$R_{VLOWD} = 1.06 \cdot R_{VLOWU}$$

(d). I_{DIMI} calculation



$$I_{DIM1} = \frac{5 \times 1.5}{R_{ISET}} = 500\mu A$$

$$R_{ISET} = (R_{HLCLPU} + R_{HLCLPD}) // (R_{VLOWU} + R_{VLOWD}) = 15\text{ kohm}$$

So,

$$R_{VLOWU} = 7.28\text{ kohm} \approx 7.2\text{ kohm}$$

$$R_{VLOWD} = 7.72\text{ kohm} \approx 7.8\text{ kohm}$$

(e). Fs calculation

$$f_{DIM} = \frac{1}{2 \cdot (2.2 - \frac{1}{3} \cdot V_{LOW}) \cdot C_{FSET}} = 1\text{kHz}$$

So,

$$C_{FSET} = 5.1\text{nF}$$

(f).ADJ parameter

Recommended parameters:

$$R_{ADJ1} = 10\text{k ohm}$$

$$R_{ADJ2} = 120\text{k ohm}$$

(g). The design Result

Conditions			
R _{HLCLPU}	NC	R _{HLCLPD}	100k ohm
R _{VLOWU}	7.2k ohm	R _{VLOWD}	7.8k ohm
C _{FSET}	5.1nF		

Example B

#1. Identify design specification

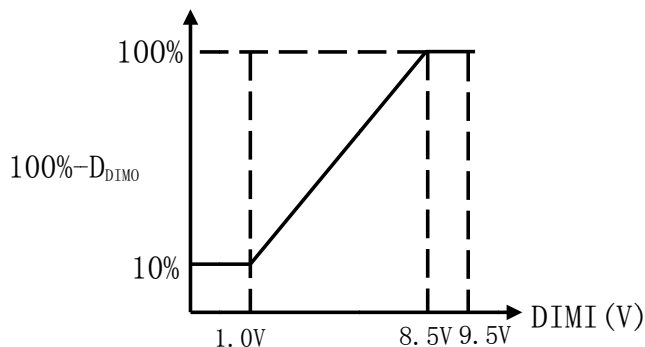


Fig.17 Target Curve

Target parameter			
I_{DIMI}	500uA	F_s	1kHz
V_{LCLP}	1.0	D_{MIN}	10%
V_{HCLP}	8.5	D_{MAX}	90%

(a). Mode Selection

As described above, Low clamp mode is selected.

(a). translation calculation

$$R_{TRS} = \frac{V_{HIGH} - V_{HCLP}}{I_{DIMI}} = \frac{9.5 - 8.5}{0.5} \text{ kohm} = 2 \text{ kohm}$$

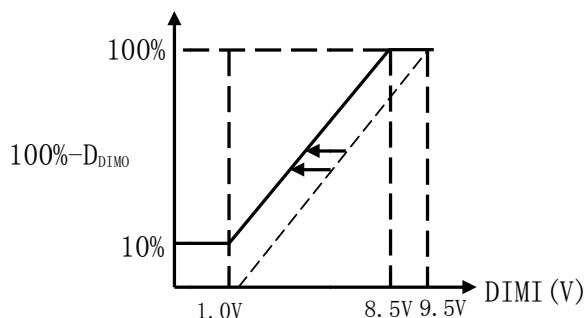


Fig.18 Curve translation

(b). VLOWI calculation

Zero Cross point:

$$V_{LOWI} = \frac{8.5 - 1.0}{100\% - 10\%} (0 - 10\%) + 1.0 + I_{DIMI} \cdot R_{TRS} = 1.167 \text{ V}$$

Due to,

$$V_{LOWI} = 1.55 \cdot V_{LOW} - 0.926 + 0.2 = 1.167$$

$$V_{LOW} = \frac{V_{ISET} \cdot R_{VLOWD}}{R_{VLOWU} + R_{VLOWD}} = 1.22$$

So,

$$R_{VLOWD} = 4.38 \cdot R_{VLOWU}$$

(c). Low clamp mode design

$$V_{LCLP} = \frac{9.3}{2} \cdot (V_{HLCLP} - 0.2) + 0.2$$

$$= \frac{9.3}{2} \cdot \left(\frac{V_{ISET} \cdot R_{HLCLPD}}{R_{HLCLPU} + R_{HLCLPD}} - 0.2 \right) + 0.2 = V_{LCLP} + I_{DIMI} \cdot R_{TRS}$$

So,

$$R_{HLCLPD} = 0.64 \cdot R_{HLCLPU}$$

If $R_{HLCLPU} + R_{HLCLPD} = 100 \text{ kohm}$

$$R_{HLCLPU} = 61.0 \text{ kohm} \approx 62 \text{ kohm}$$

$$R_{HLCLPD} = 39 \text{ kohm}$$

(d). I_{DIMI} calculation

$$I_{DIMI} = \frac{5 \times 1.5}{R_{ISET}} = 500 \text{ uA}$$

$$R_{ISET} = (R_{HLCLPU} + R_{HLCLPD}) / (R_{VLOWU} + R_{VLOWD}) = 15 \text{ kohm}$$

So,

$$R_{VLOWU} = 3.3 \text{ kohm}$$

$$R_{VLOWD} = 14.4 \text{ kohm} \approx 15 \text{ kohm}$$

(e). f_s calculation

$$f_{DIM} = \frac{20 \mu}{2 \cdot \left(2.2 - \frac{1}{3} \cdot V_{LOW} \right) \cdot C_{FSET}} = 1 \text{ kHz}$$

So,

$$C_{FSET} = 5.1 \text{ nF}$$

(f). ADJ parameter

Recommended parameters:

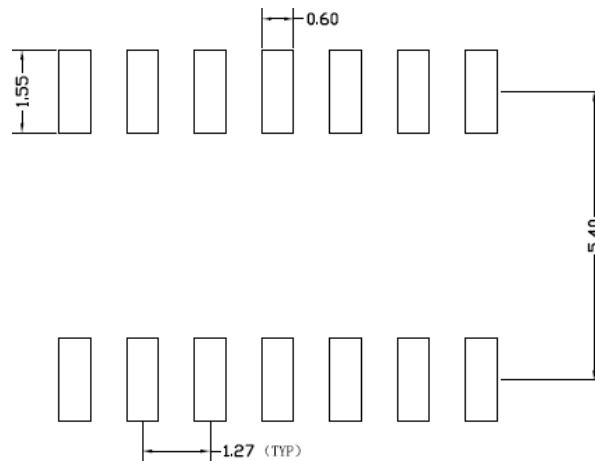
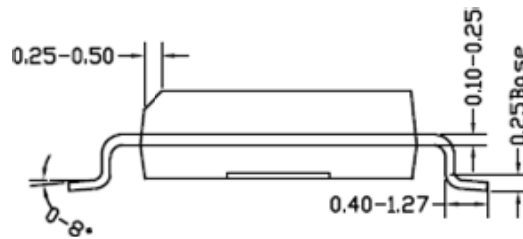
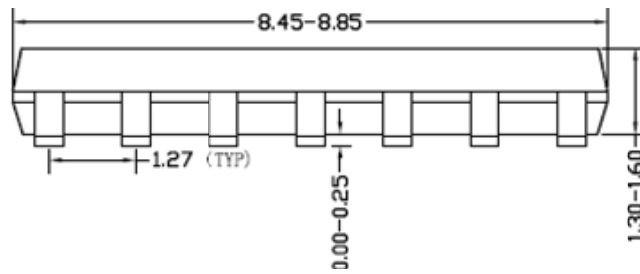
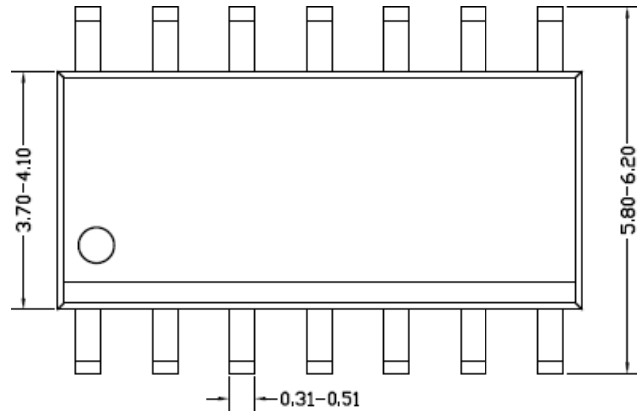
$$R_{ADJ1} = 10 \text{ k ohm}$$

$$R_{ADJ2} = 120 \text{ k ohm}$$

(g). The design Result

Conditions			
R_{HLCLPU}	62k ohm	R_{HLCLPD}	39k ohm
R_{VLOWU}	3.3k ohm	R_{VLOWD}	15k ohm
R_{TRS}	2.0k ohm	C_{FSET}	5.1nF

SOP14 Package Outline Drawing & PCB Layout



PCB layout (Recommended)

Notes: All dimension in MM and exclude mold flash & metal burr.



IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.
2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.
3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.
4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.
5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.
6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2018 Silergy Corp.

All Rights Reserved.