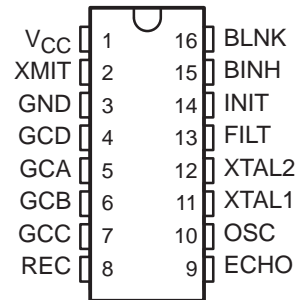- **Designed for Use With the TL852 in Sonar Ranging Modules Like the SN28827**
- **Operates With Single Supply**
- **Accurate Clock Output for External Use**
- **Synchronous 4-Bit Gain Control Output**
- **Internal 1.2-V Level Detector for Receive**
- **TTL-Compatible**
- **Interfaces to Electrostatic or Piezoelectric Transducers**

N PACKAGE
(TOP VIEW)

V_{CC}	1	16	BLNK
XMIT	2	15	BINH
GND	3	14	INIT
GCD	4	13	FILT
GCA	5	12	XTAL2
GCB	6	11	XTAL1
GCC	7	10	OSC
REC	8	9	ECHO

description

The TL851 is an economical digital I^2L ranging control integrated circuit designed for use with the Texas Instruments TL852 sonar ranging receiver integrated circuit.

The TL851 is designed for distance measurement from six inches to 35 feet. The device has an internal oscillator that uses a low-cost external ceramic resonator. With a simple interface and a 420-kHz ceramic resonator, the device will drive a 50-kHz electrostatic transducer.

The device cycle begins when Initiate (INIT) is taken to the high logic level. There must be at least 5 ms from initial power-up (V_{CC}) to the first initiate signal in order for all the device internal latches to reset and for the ceramic-resonator-controlled oscillator to stabilize. The device will transmit a burst of 16 pulses each time INIT is taken high.

The oscillator output (OSC) is enabled by INIT. The oscillator frequency is the ceramic resonator frequency divided by 8.5 for the first 16 cycles (during transmit) and then the oscillator frequency changes to the ceramic resonator frequency divided by 4.5 for the remainder of the device cycle.

When used with an external 420-kHz ceramic resonator, the device internal blanking disables the receive input (REC) for 3.8 ms after initiate to exclude false receive inputs that may be caused by transducer ringing. The internal blanking feature also eliminates echos from objects closer than 1.3 feet from the transducer. If it is necessary to detect objects closer than 1.3 feet, then the internal blanking may be shortened by taking the blanking inhibit (BINH) high, enabling the receive input. The blanking input (BLNK) may be used to disable the receive input and reset ECHO to a low logic level at any time during the device cycle for selective echo exclusion or for a multiple-echo mode of operation.

The device provides a synchronous 4-bit gain control output (12 steps) designed to control the gain of the TL852 sonar ranging receiver integrated circuit. The digital gain control waveforms are shown in Figure 2 with the nominal transition times from INIT listed in the Gain Control Output Table.

The threshold of the internal receive level detector is 1.2 V. The TL851 operates over a supply voltage range of 4.5 V to 6.8 V and is characterized for operation from 0°C to 40°C.

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TEXAS INSTRUMENTS

TL851
SONAR RANGING CONTROL

GAIN CONTROL OUTPUT TABLE

STEP NUMBER	GCD	GCC	GCB	GCA	TIME (ms) FROM INITIATE↑†
0	L	L	L	L	2.38 ms
1	L	L	L	H	5.12 ms
2	L	L	L	L	7.87 ms
3	L	L	H	H	10.61 ms
4	L	H	L	L	13.35 ms
5	L	H	L	H	16.09 ms
6	L	H	H	L	18.84 ms
7	L	H	H	H	21.58 ms
8	H	L	L	L	27.07 ms
9	H	L	L	H	32.55 ms
10	H	L	H	L	38.04 ms
11	H	L	H	H	INIT ↓

† This is the time to the end of the indicated step and assumes a nominal 420-kHz ceramic resonator.

functional block diagram
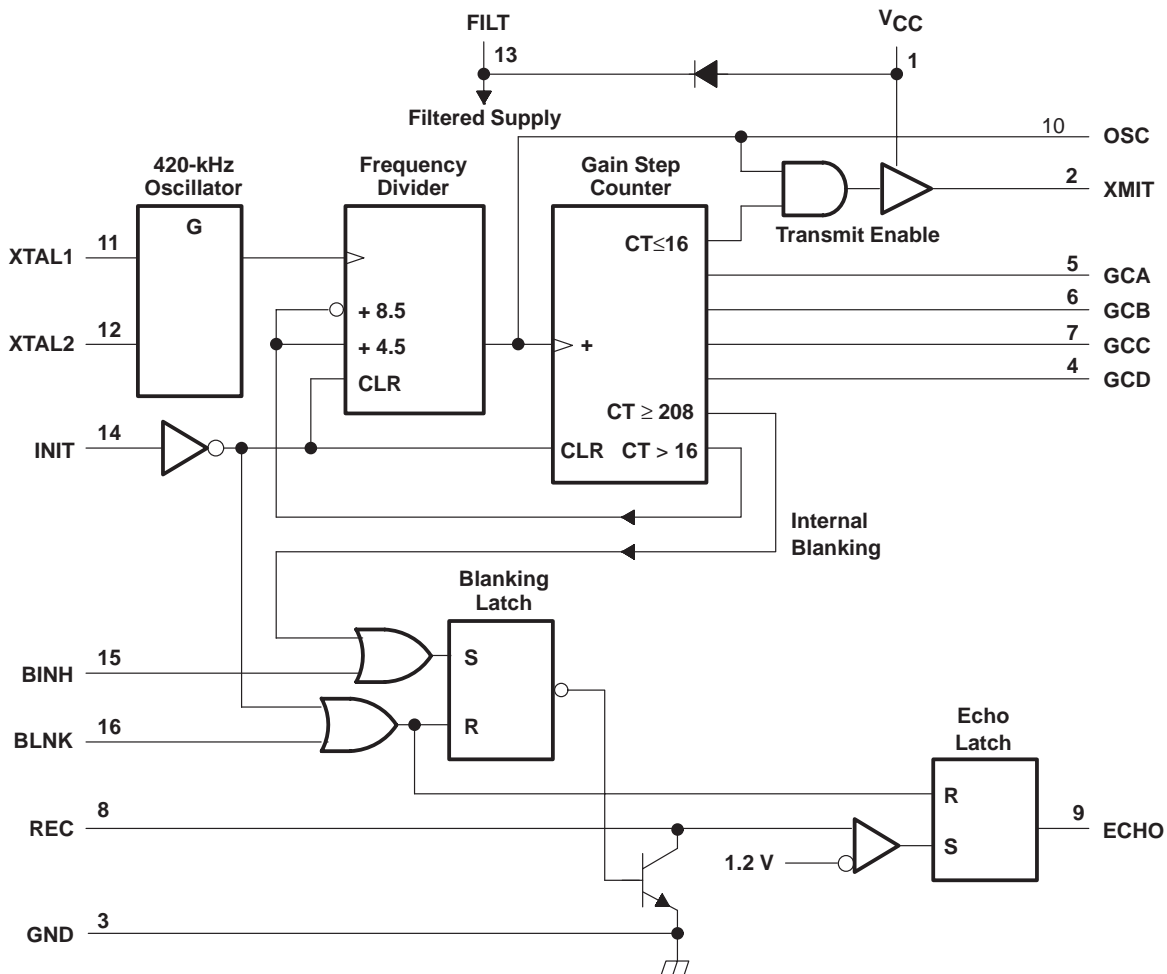
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range at any pin with respect to GND . . . . − 0.5 V to 7 V
Voltage range at any pin with respect to V_{CC} . . . . − 7 V to 0.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . 1150 mW
Operating free-air temperature range . . . . 0°C to 40°C
Storage temperature range . . . . − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
Delay time, power up to INIT high		5		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	ECHO, OSC, GCA, GCB, GCC, GCD	V_{OH} = 5.5 V			100	μA
Low-level output current, I_{OH}	ECHO, OSC, GCA, GCB, GCC, GCD	I_{OL} = 1.6 mA			0.4	V
On-state output current	SMIT output	V_O = 1 V		−140		mA
Internal blanking interval	REC input			2.38§		ms
Frequency during 16-pulse transmit period	OSC output			49.4§		kHz
Frequency during 16-pulse transmit period	XMIT output			49.4§		kHz
Frequency after 16-pulse transmit period	OSC output			93.3§		kHz
Frequency after 16-pulse transmit period	XMIT output			0		kHz
Supply current, I_{CC}	During transmit period				260	mA
Supply current, I_{CC}	After transmit period				55	mA

‡ Typical values are at V_{CC} = 5 V and T_A = 25°C.
§ These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs

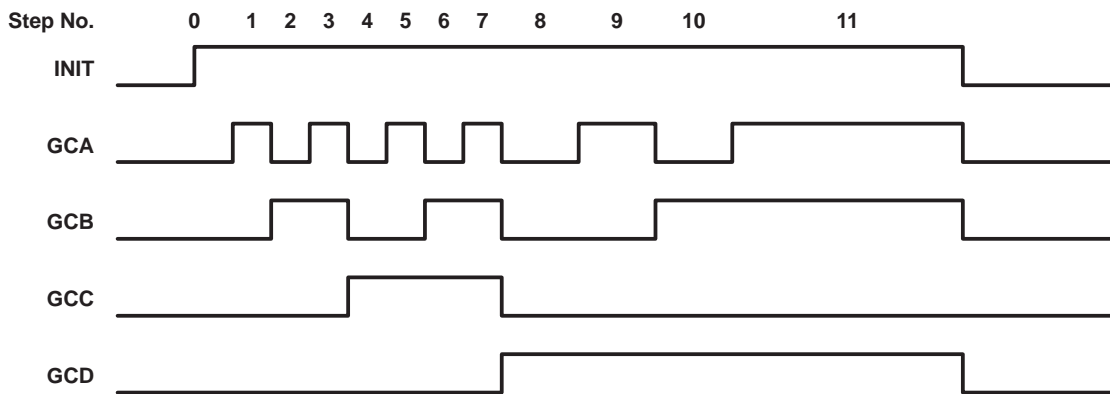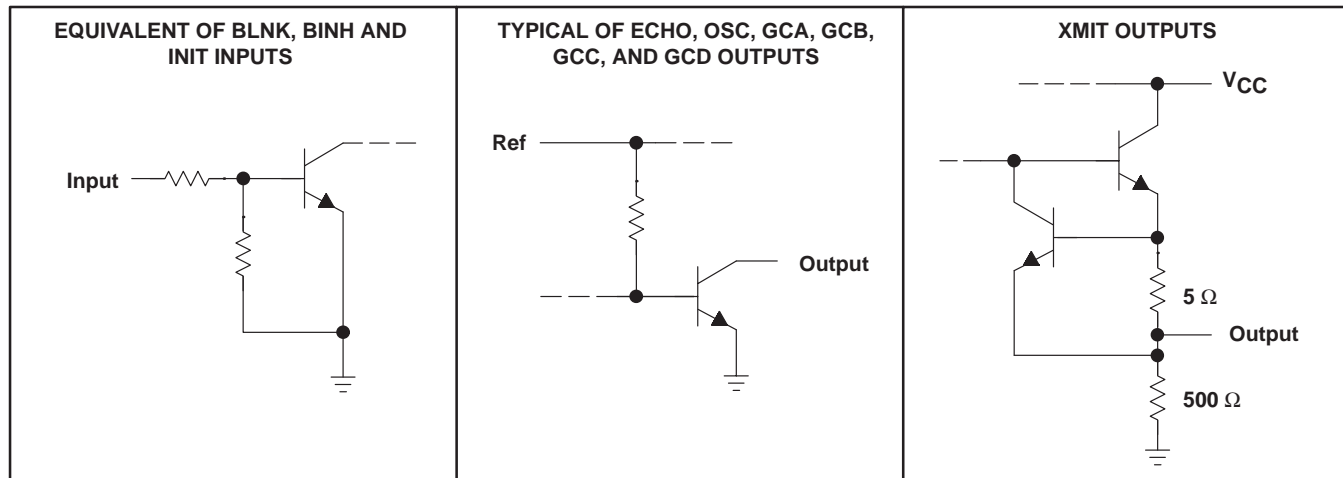| EQUIVALENT OF BLNK, BINH AND INIT INPUTS	TYPICAL OF ECHO, OSC, GCA, GCB, GCC, AND GCD OUTPUTS	XMIT OUTPUTS

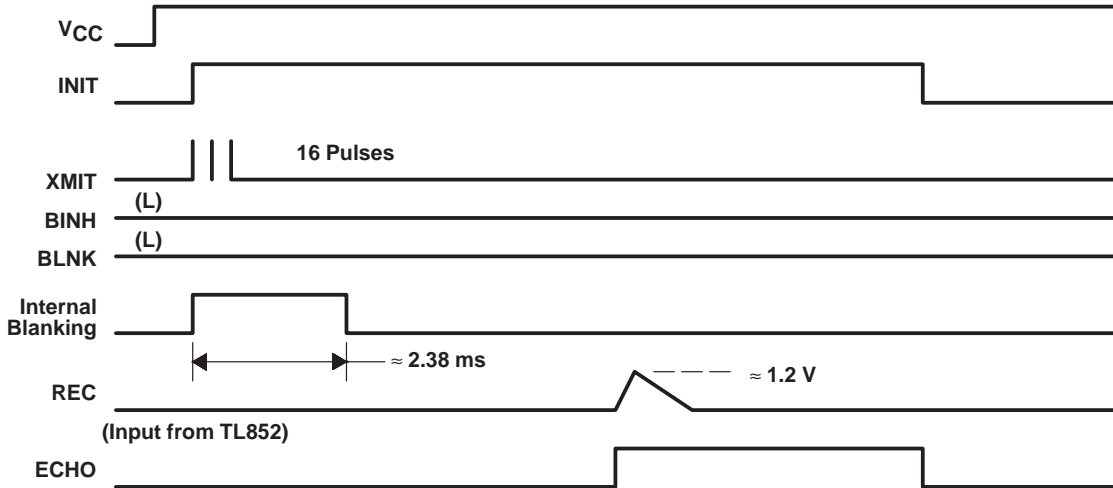**Figure 1. Digital Gain Control Waveforms**

Figure 2. Example of Single-Echo-Mode Cycle When Used With the TL852 Receiver and 420-kHz Ceramic Resonator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL851CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL851C	Samples
TL851CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL851C	Samples
TL851CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL851C	Samples
TL851CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL851C	Samples
TL851CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TL851CN	Samples
TL851CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TL851CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL851CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL851CDR	SOIC	D	16	2500	367.0	367.0	38.0

N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

$\frac{0.070\ (1,78)}{0.045\ (1,14)}$ /D\

$\frac{0.045\ (1,14)}{0.030\ (0,76)}$ /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

$\frac{0.021\ (0,53)}{0.015\ (0,38)}$

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
/C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
/D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16)　　　　　　　　　　　PLASTIC SMALL OUTLINE
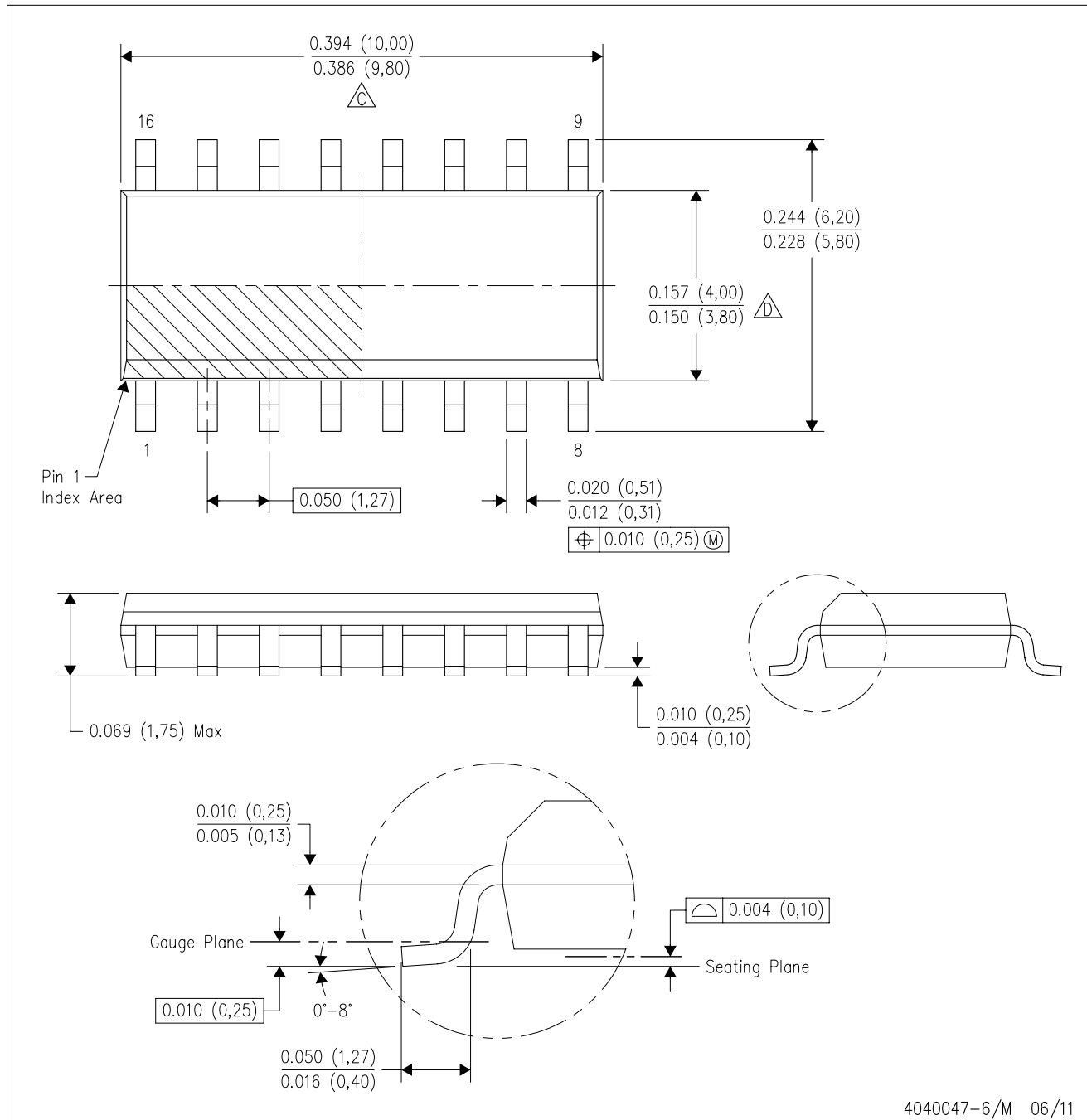
0.394 (10,00)
0.386 (9,80)
C

16　　　　　　　9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)　D

1　　　　　　　8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)　　0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M　06/11

NOTES:　A. All linear dimensions are in inches (millimeters).
　　　　B. This drawing is subject to change without notice.
　　　　C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
　　　　D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
　　　　E. Reference JEDEC MS−012 variation AC.

TEXAS
INSTRUMENTS
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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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