TPS54295 集成 FET 的 2A 双通道同步降压开关

1 特性

- D-CAP2™控制模式
  - 快速瞬态响应
  - 环路补偿无需外部部件
  - 与陶瓷输出电容兼容
- 宽输入电压范围：4.5V 至 18V
- 输出电压范围：0.76V 至 7V
- 高效集成场效应晶体管 (FET) 针对低占空比进行了优化 应用
  - 150mΩ（高侧）和 100mΩ（低侧）
- 高初始基准精度
- 低侧 $r_{DS(ON)}$ 无损耗电流感测
- 可调节软启动
- 非灌电流预偏置软启动
- 700kHz 开关频率
- 逐周期过流限制控制
- 过流限制 (OCL)、过压保护 (OVP)、欠压保护 (UVP)、欠压锁定 (UVLO) 和热关断 (TSD) 保护
- 集成升压 P 沟道金属氧化物半导体 (PMOS) 开关的自适应栅极驱动
- 凭借温漂为 4000ppm/℃ 的热补偿 $r_{DS(ON)}$，OCP 恒定不变
- 16 引脚散热薄型小外形尺寸 (HTSSOP) 封装，16 引脚超薄四方扁平无引线封装 (VQFN)
- 自动跳跃 Eco-mode™模式，以在轻负载时实现高效率

2 应用范围

- 低功耗系统中的负载点调节，广泛适用于各种 应用
  - 数字电视电源
  - 网络家庭终端设备
  - 数字机顶盒 (STB)
  - DVD 播放器和录像机
  - 游戏控制台和其他设备

3 说明

TPS54295 是一款双路自适应导通时间 D-CAP2 模式同步降压转换器。TPS54295 有助于系统设计人员通过具备成本效益、所用组件较少并且待机电流较低的解决方案完成各种终端设备的电源总线调节器集。TPS54295 的主控制回路采用 D-CAP2 模式控制，无需外部补偿元件即可实现快速瞬态响应。自适应接通时间控制可在更高负载状态下的脉宽调制 (PWM) 模式与轻负载下的 Eco-mode 工作之间实现无缝转换。Eco-mode 使 TPS54295 能够在轻载状况下保持高效率。TPS54295 既能够适应诸如高分子有机半导体固体电容 (POSCAP) 或高分子聚合物电容 (SP-CAP) 的低等效串联电阻 (ESR) 输出电容，也能够适应超低等效串联电阻 (ESR) 的陶瓷电容。该器件在输入电压介于 4.5V 至 18V 范围内时实现便捷高效的运行。

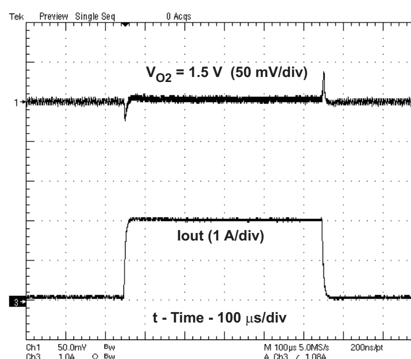
TPS54295 采用 4.4mm × 5mm 16 引脚 HTSSOP (PWP) 封装以及 4mm x 4mm 16 引脚 VQFN (RSA) 封装，设计为在 –40°C 至 85°C 的环境温度范围内运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS54295	HTSSOP (16)	5.00mm x 4.40mm
	VQFN (16)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

负载瞬态响应



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

1 特性 1
2 应用范围 1
3 说明 1
4 修订历史记录 2
5 Pin Configuration and Functions 3
6 Specifications 4
 6.1 Absolute Maximum Ratings 4
 6.2 ESD Ratings 4
 6.3 Recommended Operating Conditions 4
 6.4 Thermal Information 5
 6.5 Electrical Characteristics 5
 6.6 Typical Characteristics 7
7 Detailed Description 10
 7.1 Overview 10
 7.2 Functional Block Diagram 11
 7.3 Feature Description 12
 7.4 Device Functional Modes 13
8 Application and Implementation 14
 8.1 Application Information 14
 8.2 Typical Application 14
9 Power Supply Recommendations 18
10 Layout 18
 10.1 Layout Guidelines 18
 10.2 Layout Example 19
 10.3 Thermal Considerations 21
11 器件和文档支持 22
 11.1 器件支持 22
 11.2 文档支持 22
 11.3 接收文档更新通知 22
 11.4 社区资源 22
 11.5 商标 22
 11.6 静电放电警告 22
 11.7 Glossary 22
12 机械、封装和可订购信息 22

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (April 2013) to Revision D **Page**

- 已添加 *器件信息表，规范部分，ESD 额定值表，详细 说明部分，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* 1
- 已删除 *订购信息表*；请参见数据表末尾的 POA 1
- Deleted Operating ambient temperature from *Absolute Maximum Ratings* table 4
- Deleted Operating ambient temperature from *Recommended Operating Conditions* table 4
- Changed Operating junction temperature maximum value from 150 to 125 in *Recommended Operating Conditions* table 4

Changes from Revision B (December 2011) to Revision C **Page**

- 已添加"RSA-16 引脚封装"至*订购信息表* 1
- 已更改 说明部分的 文本，以包含 RSA 封装 1
- Added the RSA-16 Pin package pin out 3
- Added Figure 26 20

Changes from Revision A (October 2011) to Revision B **Page**

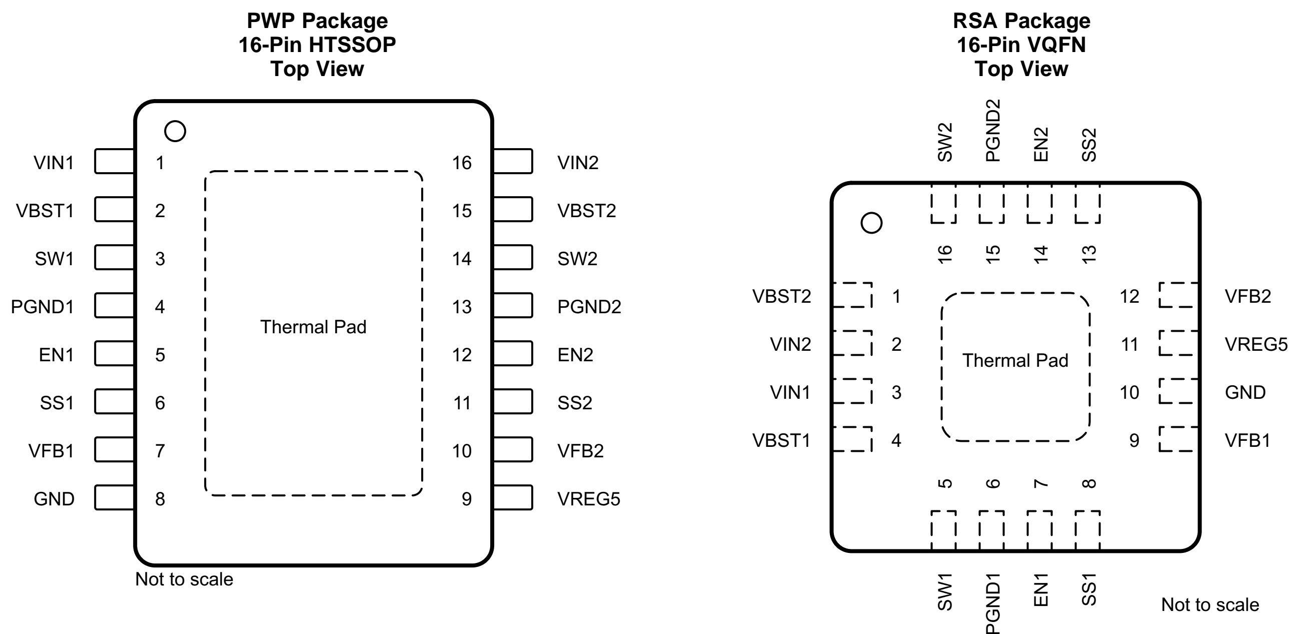
- Deleted MIN and MAX values from V_{VREG5} specification 5
- Deleted Line and Load regulation specs from V_{REG5} specification 5
- Added "Ensured by design. Not production tested" annotation to specifications for MOSFETs, ON-TIME TIMER CONTROl, and SOFT START. 5
- Deleted MIN and MAX values from V_{UVREG5} specification 5
- Added "VIN = 12 V, T_A = 25°C (unless otherwise noted)" to Typical Characteristics conditions statement. 7

Copyright © 2011–2016, Texas Instruments Incorporated

Changes from Original (October 2011) to Revision A **Page**

- Added indication for not production tested parameters. 5
- Added Over/Under Voltage Protection Description 13

5 Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	HTSSOP	VQFN		
EN1	5	7	I	Enable. Pull high to enable the corresponding (1 or 2) converter.
EN2	12	14		
GND	8	10	I/O	Signal GND. Connect sensitive SSx and VFBx returns to GND at a single point.
PGND1	4	6	I/O	Ground returns for low-side MOSFETs. Input of current comparator.
PGND2	13	15		
SS1	6	8	O	Soft-start programming pin. Connect capacitor from SSx pin to GND to program soft-start time.
SS2	11	13		
SW1	3	5	I/O	Switch node connections for both the high-side NFETs and low-side NFETs. Input of current comparator.
SW2	14	16		
VBST1	2	14	I	Supply input for high-side NFET gate drive circuit. Connect a 0.1-µF ceramic capacitor between VBSTx and SWx pins. An internal diode is connected between VREG5 and VBSTx.
VBST2	15	1		
VFB1	7	9	I	D-CAP2 feedback inputs. Connect to output voltage with resistor divider.
VFB2	10	12		
VIN1	1	3	I	Power inputs and connects to both high-side NFET drains. Supply Input for 5.5-V linear regulator.
VIN2	16	2		
VREG5	9	11	O	Output of 5.5-V linear regulator. Bypass to GND with a high-quality ceramic capacitor of at least 1 µF. VREG5 is active when VIN1 is added.
Thermal Pad	—	—	—	Thermal pad of the package. Must be soldered to ground to achieve appropriate dissipation. Must be connected to GND.

Copyright © 2011–2016, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

		MIN	MAX	UNIT
Input voltage	VIN1, VIN2, EN1, EN2	–0.3	20	V
	VBST1, VBST2	–0.3	26	
	VBST1, VBST2 (10-ns transient)	–0.3	28	
	VBST1 – SW1 , VBST2 – SW2	–0.3	6.5	
	VFB1, VFB2	–0.3	6.5	
	SW1, SW2	–2	20	
	SW1, SW2 (10-ns transient)	–3	22	
Output voltage	VREG5, SS1, SS2	–0.3	6.5	V
	PGND1, PGND2	–0.3	0.3	
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to IC GND terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Supply input voltage	VIN1, VIN2	4.5	18	V
	Input voltage	VBST1, VBST2	–0.1	24	V
		VBST1, VBST2 (10-ns transient)	–0.1	27	
		VBST1 – SW1, VBST2 – SW2	–0.1	5.7	
		VFB1, VFB2	–0.1	5.7	
		EN1, EN2	–0.1	18	
		SW1, SW2	–1	18	
		SW1, SW2 (10-ns transient)	–3	21	
	Output voltage	VREG5, SS1, SS2	–0.1	5.7	V
		PGND1, PGND2	–0.1	0.1	
		VO1, VO2	0.76	7	
T_J	Operating Junction Temperature		–40	125	°C

Copyright © 2011–2016, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC(1)		TPS54295 PWP (HTSSOP) 16 PINS	TPS54295 RSA (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.5	34.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.1	40	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.8	11.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VINx supply current	T_A = 25°C, V_{EN1} = V_{EN2} = 5 V, V_{VFB1} = V_{VFB2} = 0.8 V		1300	2000	μA
I_{VINSDN}	VINx shutdown current	T_A = 25°C, V_{EN1} = V_{EN2} = 0 V		80	150	μA
FEEDBACK VOLTAGE						
$V_{VFBTHLx}$	VFBx threshold voltage	T_A = 25°C, V_{CH1} = 3.3 V, V_{CH2} = 1.5 V	758	765	773	mV
TC_{VFBx}	Temperature coefficient	On the basis of 25°C(1)	–115		115	ppm/°C
I_{VFBx}	VFBx Input Current	V_{VFBx} = 0.8 V, T_A = 25°C	–0.35	0.2	0.35	μA
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 6 V < V_{IN}1 < 18 V, I_{VREG5} = 5 mA		5.5		V
I_{VREG5}	Output current	V_{IN}1 = 6 V, V_{VREG5} = 4 V, T_A = 25°C(1)		75		mA
MOSFETs						
$r_{DS(ON)H}$	High-side switch resistance	T_A = 25°C, V_{VBSTx} – V_{SWx} = 5.5 V (1)		150		mΩ
$r_{DS(ON)L}$	Low-side switch resistance	T_A = 25°C (1)		100		mΩ
ON-TIME TIMER CONTROL						
T_{ON1}	SW1 ON time	V_{SW1} = 12 V, V_{OUT}1 = 1.2 V		165		ns
T_{ON2}	SW2 ON time	V_{SW2} = 12 V, V_{OUT}2 = 1.2 V		165		ns
T_{OFF1}	SW1 minimum OFF time	T_A = 25°C, V_{VFB1} = 0.7 V(1)		220		ns
T_{OFF2}	SW2 minimum OFF time	T_A = 25°C, V_{VFB2} = 0.7 V(1)		220		ns
SOFT START						
I_{SSC}	SSx charge current	V_{SSx} = 0.5 V, T_A = 25°C	–8.4	–8	–7.6	μA
TC_{ISSC}	I_{SSC} temperature coefficient	On the basis of 25°C(1) (PWP)	–4		3	nA/°C
		On the basis of 25°C(1) (RSA)	–4		5	
I_{SSD}	SSx discharge current	V_{SSx} = 0.5 V	3	7	10	mA
UVLO						
V_{UVREG5}	VREG5 UVLO threshold	VREG5 rising		3.83		V
		Hysteresis		0.6		
LOGIC THRESHOLDS						
V_{ENxH}	ENx H-level threshold voltage		2			V
V_{ENxL}	ENx L-level threshold voltage				0.4	V
R_{ENx_IN}	ENx input resistance	V_{ENx} = 12 V	225	450	900	kΩ
CURRENT LIMITS						
I_{OCL}	Current limit	L_{OUT} = 2.2 μH(1)	2.7	3.9	4.5	A

(1) Ensured by design. Not production tested.

Copyright © 2011–2016, Texas Instruments Incorporated

Electrical Characteristics (continued)

over recommended free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION (UVP, OVP)						
V_{OVP}	Output OVP trip threshold	measured on VFBx	115%	120%	125%	
T_{OVPDEL}	Output OVP prop delay			3	10	µs
V_{UVP}	Output UVP trip threshold	measured on VFBx	63%	68%	73%	
T_{UVPDEL}	Output UVP delay time			1.5		ms
T_{UVPEN}	Output UVP enable delay	UVP enable delay and soft-start time	× 1.4	× 1.7	× 2	
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	Shutdown temperature [(1)]		155		°C
		Hysteresis [(1)]		25		

6.6 Typical Characteristics

One output is enabled unless otherwise noted. $V_I = V_{IN}1$ or $V_{IN}2$. V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

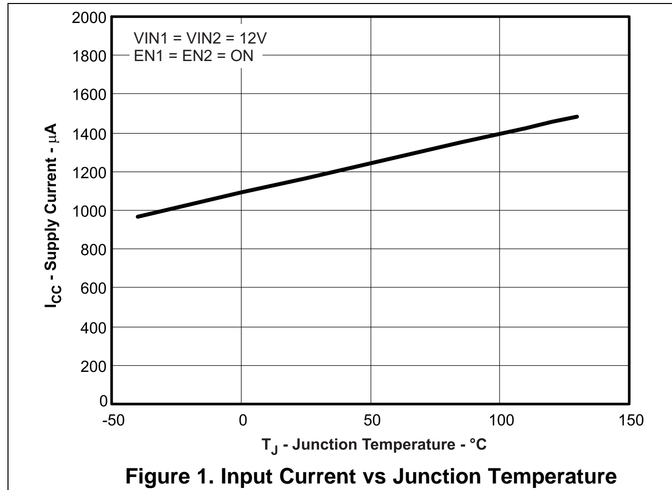


Figure 1. Input Current vs Junction Temperature

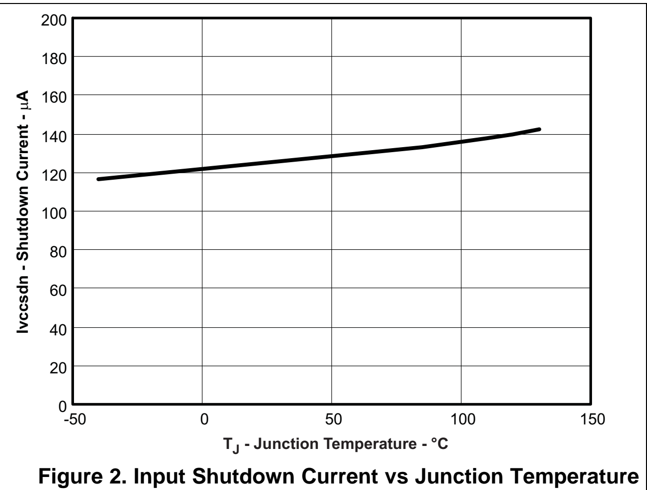
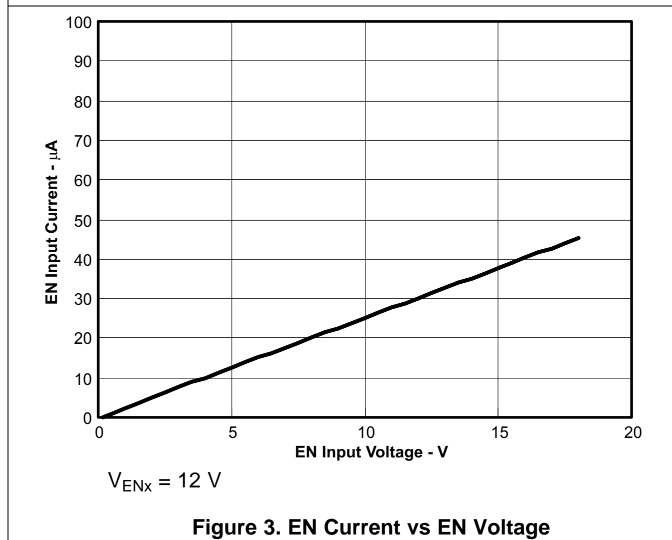
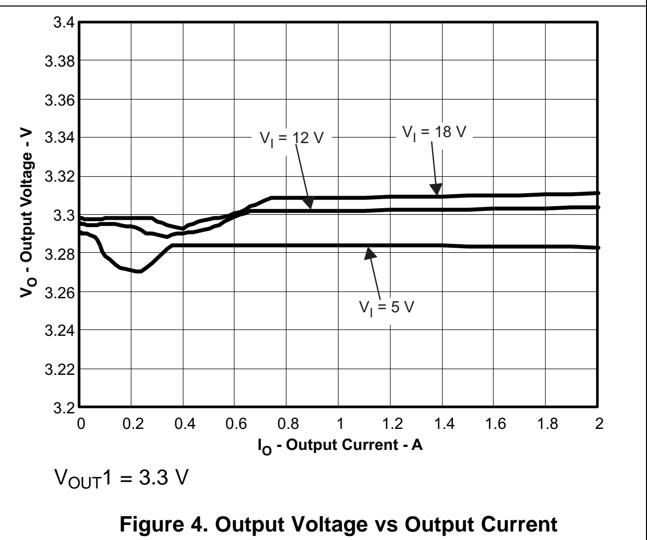


Figure 2. Input Shutdown Current vs Junction Temperature



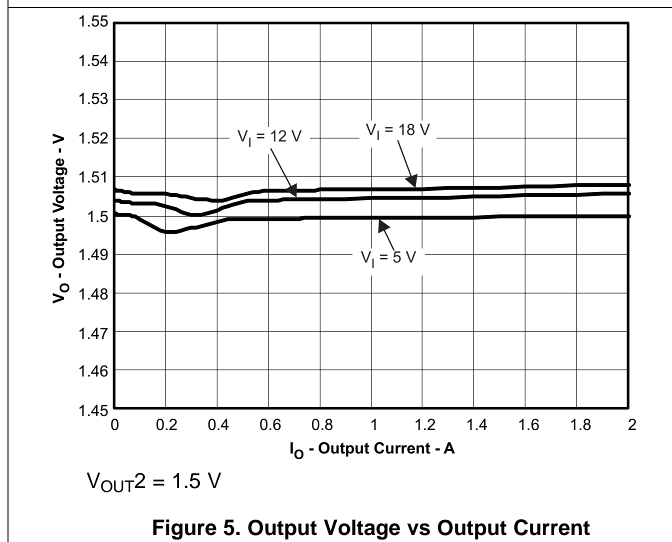
V_{ENx} = 12 V

Figure 3. EN Current vs EN Voltage



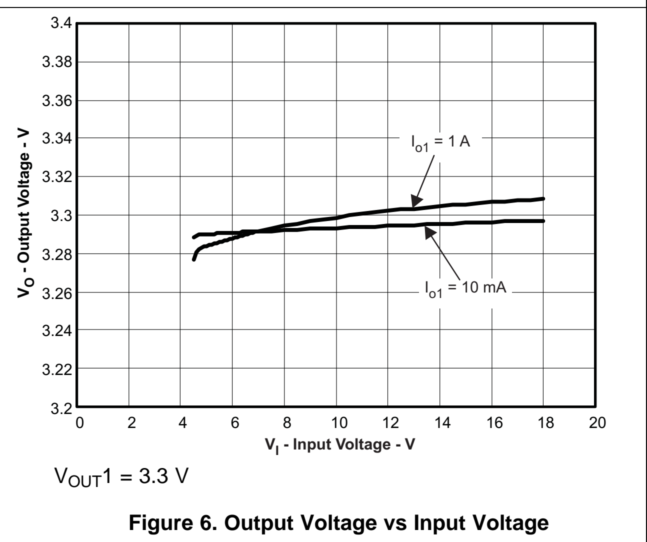
$V_{OUT}1$ = 3.3 V

Figure 4. Output Voltage vs Output Current



$V_{OUT}2$ = 1.5 V

Figure 5. Output Voltage vs Output Current



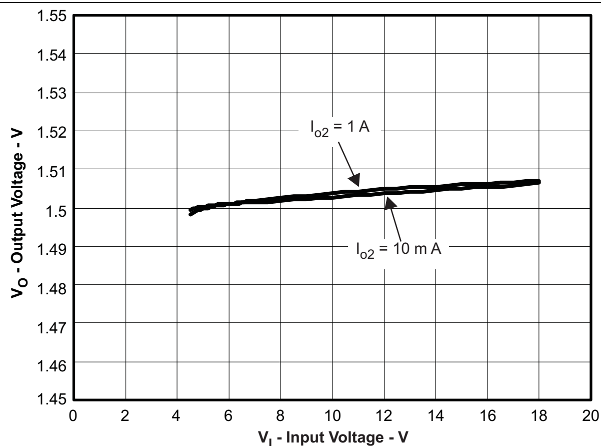
$V_{OUT}1$ = 3.3 V

Figure 6. Output Voltage vs Input Voltage

Copyright © 2011–2016, Texas Instruments Incorporated

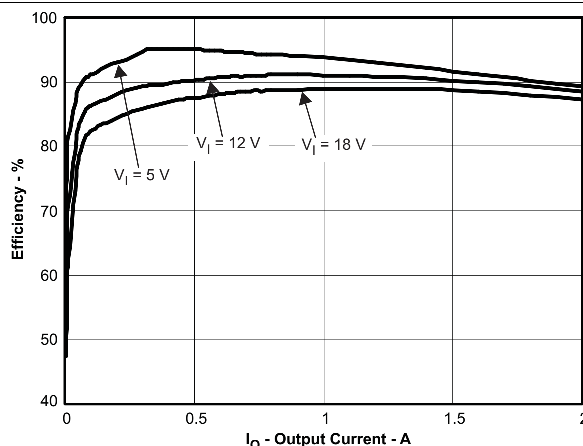
Typical Characteristics (continued)

One output is enabled unless otherwise noted. V_I = V_{IN}1 or V_{IN}2. V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).



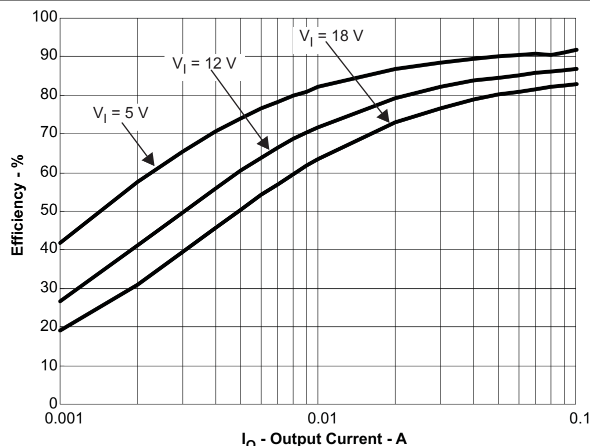
V_{OUT}2 = 1.5 V

Figure 7. Output Voltage vs Input Voltage



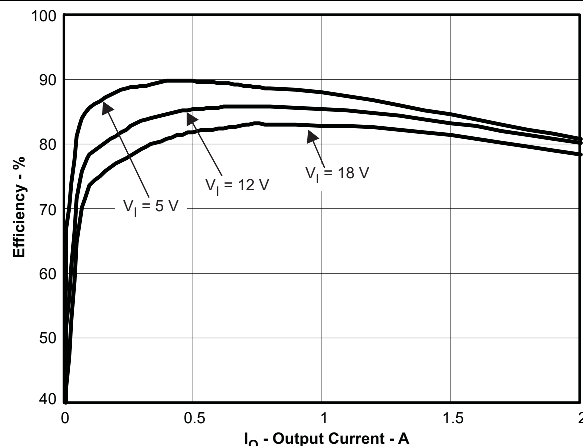
V_{OUT}1 = 3.3 V

Figure 8. Efficiency vs Output Current



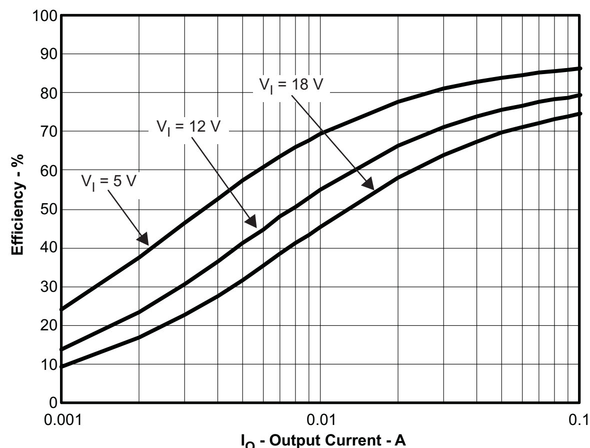
V_{OUT}1 = 3.3 V

Figure 9. Efficiency vs Output Current



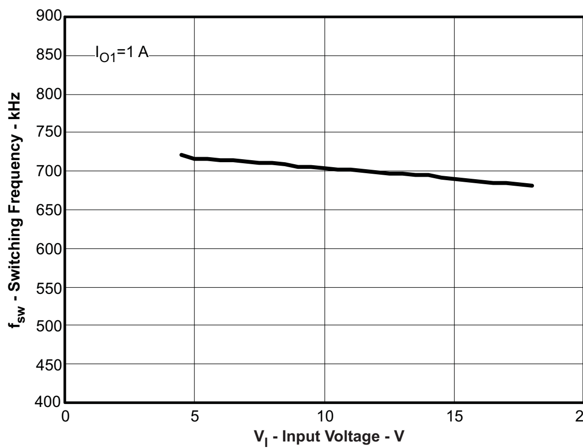
V_{OUT}1 = 1.5 V

Figure 10. Efficiency vs Output Current



V_{OUT}2 = 1.5 V

Figure 11. Efficiency vs Output Current

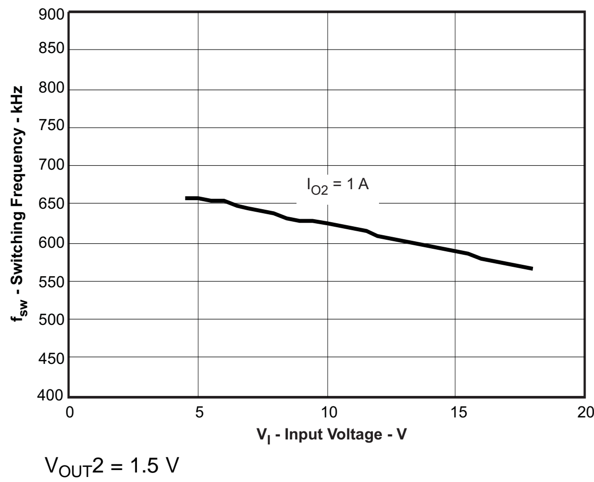


V_{OUT}1 = 3.3 V

Figure 12. Switching Frequency vs Input Voltage

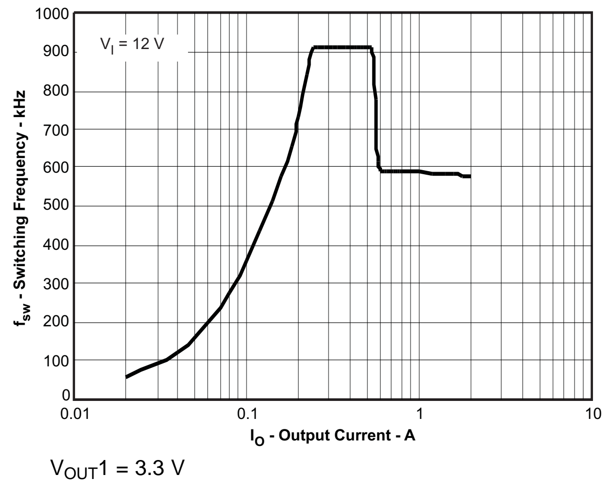
Typical Characteristics (continued)

One output is enabled unless otherwise noted. $V_I = V_{IN}1$ or $V_{IN}2$. V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).



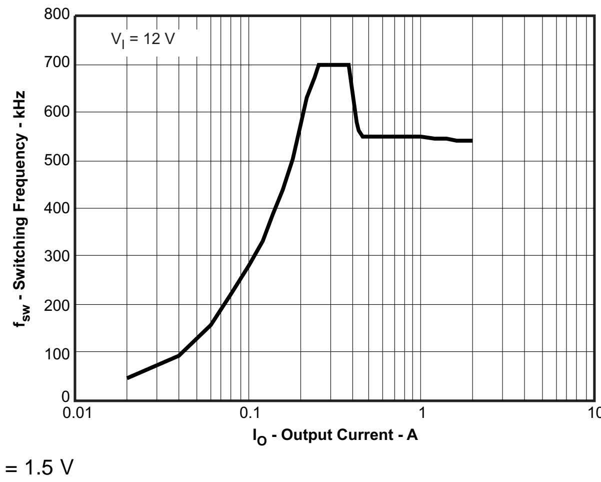
$V_{OUT}2$ = 1.5 V

Figure 13. Switching Frequency vs Input Voltage



$V_{OUT}1$ = 3.3 V

Figure 14. Switching Frequency vs Output Current



$V_{OUT}2$ = 1.5 V

Figure 15. Switching Frequency vs Output Current

Copyright © 2011–2016, Texas Instruments Incorporated

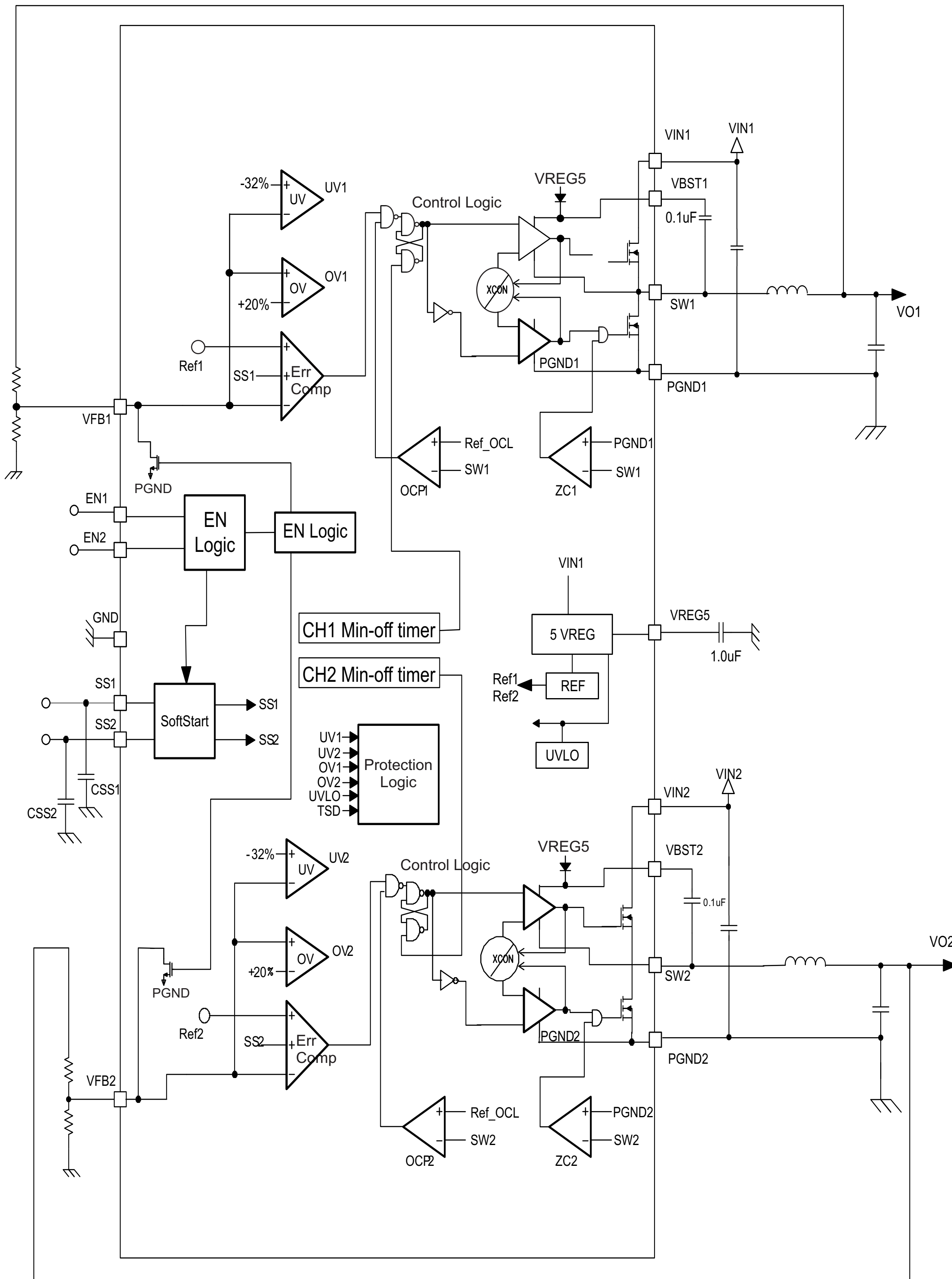
7 Detailed Description

7.1 Overview

The TPS54295 is a 2-A and 2-A, dual synchronous step-down (buck) converter with two integrated N-channel MOSFETs for each channel. It operates using D-CAP2 control mode. The fast transient response of D-CAP2 control reduces the required output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

Copyright © 2011–2016, Texas Instruments Incorporated

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

Copyright © 2011–2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS54295 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 control mode. D-CAP2 control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off when the internal timer expires. This timer is set by the converter's input voltage (V_{IN}x) and the output voltage (V_{OUT}x) to maintain a pseudo-fixed frequency over the input voltage range hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output voltage ripple, eliminating the need for ESR induced output ripple from D-CAP control.

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS54295 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54295 runs with a pseudo-fixed frequency of 700 kHz by using the input voltage and output voltage to set the on-time timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is V_{OUT}x / V_{IN}x, the frequency is constant.

7.3.3 Auto-Skip Eco-Mode Control

The TPS54295 is designed with auto-skip Eco-mode to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current also reduces and eventually comes to the point where its ripple valley touches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost half as it was in the continuous conduction mode because it takes longer to discharge the output capacitor with smaller load current to the nominal output voltage. The transition point to the light load operation current ($I_{OUT(LL)}$x) can be estimated with Equation 1 with 700 kHz used as f_{SW}.

$$I_{OUT(LL)}x = \frac{1}{2 \times L1x \times f_{SW}} \times \frac{\left(V_{IN}x - V_{OUT}x\right) \times V_{OUT}x}{V_{IN}x} \quad (1)$$

7.3.4 Soft Start and Prebiased Soft Start

The soft-start time is adjustable. When the ENx pin becomes high, 8-µA current begins charging the capacitor which is connected from the SSx pin to GND. Smooth control of the output voltage is maintained during start-up. Calculate the slow-start time with Equation 2. VFBx voltage is 0.765 V and SSx pin source current is 8 µA.

$$T_{SS}(ms) = \frac{C4x(nF) \times VFBx(V)}{I_{SS}(\mu A)} = \frac{C4x(nF) \times 0.765\ V}{8\ \mu A} \quad (2)$$

The TPS54295 contains a unique circuit to prevent current from being pulled from the output during start-up if the output is prebiased. When the soft start commands a voltage higher than the prebias level (internal soft start becomes greater than internal feedback voltage), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by 1 – D, where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebiased output, and ensures that the output voltage starts and ramps up smoothly into regulation from prebiased start-up to normal mode operation.

7.3.5 Overcurrent Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detection control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SWx and PGNDx pins. This voltage is proportional to the switch current and the on-resistance of the FET. To improve the measurement accuracy, the voltage sensing is temperature compensated.

Copyright © 2011–2016, Texas Instruments Incorporated

Feature Description (continued)

During the ON time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}x$, $V_{OUT}x$, the ON time, and the output inductor value. During the ON time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current (I_{OUTx}). If the sensed voltage on the low-side FET is above the voltage proportional to the current limit, the converter keeps the low-side switch on until the measured voltage falls below the voltage corresponding to the current limit and a new switching cycle begins. In subsequent switching cycles, the on-time is set to the value determined for CCM and the current is monitored in the same manner.

Following are some important considerations for this type of overcurrent protection. The load current is one half of the peak-to-peak inductor current higher than the overcurrent threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. When the overcurrent condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

7.3.6 Overvoltage and Undervoltage Protection

TPS54295 monitors the resistor divided feedback voltage to detect overvoltage and undervoltage. If the feedback voltage is higher than 120% of the reference voltage, the OVP comparator output goes high and the circuit latches both the high-side MOSFET driver and the low-side MOSFET driver off. When the feedback voltage is lower than 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1.5 ms, TPS54295 latches OFF both the high-side MOSFET and the low-side MOSFET drivers. This function is enabled approximately 1.7 times the soft-start time after power on. The OVP and UVP latch off is reset when EN is toggled.

7.3.7 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than the UVLO threshold, the TPS54295 shuts down. As soon as the voltage increases above the UVLO threshold, the converter starts again.

7.3.8 Thermal Shutdown

TPS54295 monitors its temperature. If the temperature exceeds the threshold value (typically 155°C), the device shuts down. When the temperature falls below the threshold, the IC starts again.

When VIN1 starts up and VREG5 output voltage is below its nominal value, the thermal shutdown threshold is lower than 155°C. As long as VIN1 rises, T_J must be kept below 110°C.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS54295 can operate in the normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS54295 operates at a quasi-fixed frequency of 700 kHz while $V_{OUT}1 = V_{OUT}2 = 3.3$ V.

7.4.2 Eco-Mode Operation

When the TPS54295 is in the normal CCM operating mode and the switch current falls to 0 A, the TPS54295 begins operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

7.4.3 Standby Operation

When the TPS54295 is operating in either normal CCM or Eco-mode, it may be placed in standby mode by asserting the EN pin low.

Copyright © 2011–2016, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54295 is a typical step-down DC-DC converter. The device typically is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A.

8.2 Typical Application

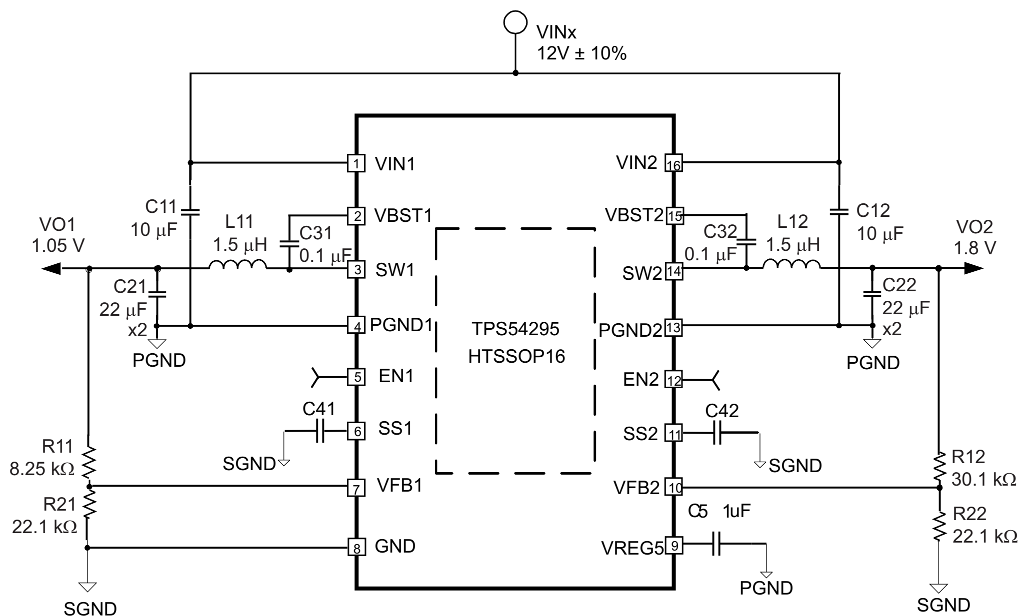


Figure 16. Schematic Diagram for the Design Example

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	4.5 V to 18 V
Output voltage	1.05 V and 1.8 V
Transient response (1.5-A load step)	ΔV_{OUT} = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	2 A
Operating frequency	700 kHz

8.2.2 Detailed Design Procedure

This section presents a simplified design process and guidelines for component selection. Alternatively the WEBENCH® software may be used to generate a complete design. WEBENCH uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

To begin the design process, determine the following application parameters:

- Input voltage
- Output voltage
- Output current

In all formulas *x* is used to indicate that they are valid for both converters. For the calculations the estimated switching frequency of 700 kHz is used.

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFBx pin. TI recommends 1% tolerance or better divider resistors. Start by using Equation 3 to calculate $V_{OUT}x$.

To improve the efficiency at very light loads consider using larger value resistors, but resistance values that are too high make the device susceptible to noise and voltage errors due to the VFBx input current being more noticeable.

$$V_{OUT}x = 0.765\ V \times \left(1 + \frac{R1x}{R2x}\right) \tag{3}$$

8.2.2.2 Output Filter Selection

The output filter used with the TPS54295 is an LC circuit. This LC filter has a double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L1x \times C1x}} \tag{4}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS545295. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1x (kΩ)	R2x (kΩ)	$C_{FF}x$ (pF)(1)	L1x (µH)	C2x (µF)
1	6.81	22.1	—	1 to 1.5	22 to 68
1.05	8.25	22.1	—	1 to 1.5	22 to 68
1.2	12.7	22.1	—	1 to 1.5	22 to 68
1.5	21.5	22.1	—	1.5	22 to 68
1.8	30.1	22.1	5 to 22	1.5	22 to 68
2.5	49.9	22.1	5 to 22	2.2	22 to 68
3.3	73.2	22.1	5 to 22	2.2	22 to 68
5	124	22.1	5 to 22	3.3	22 to 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C_{FF}) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6, and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Copyright © 2011–2016, Texas Instruments Incorporated

For the calculations, use 700 kHz as the switching frequency (f_{SW}). Make sure the chosen inductor is rated for the peak current of Equation 6 and the RMS current of Equation 7.

$$\Delta I_{L1x} = \frac{V_{OUT}x}{V_{IN(MAX)}x} \times \frac{V_{IN(MAX)}x - V_{OUT}x}{L1x \times f_{SW}} \tag{5}$$

$$I_{L1xpeak} = I_{OUT}x + \frac{\Delta I_{L1x}}{2} \tag{6}$$

$$I_{L1x(RMS)} = \sqrt{I_{OUT}x^2 + \frac{1}{12}\Delta I_{L1x}^2} \tag{7}$$

For this design example, the calculated peak current is 2.46 A and the calculated RMS current is 2.02 A for $V_{OUT}1$. The inductor used has a rated current of 7.3 A based on the inductance change and of 4.9 A based on the temperature rise.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54295 is intended for use with ceramic or other low ESR capacitors. TI recommends a value from 22 µF to 68 µF. Use Equation 8 to determine the required RMS current rating for the output capacitors.

$$I_{C2x(RMS)} = \frac{V_{OUT}x \times (V_{IN}x - V_{OUT}x)}{\sqrt{12} \times V_{IN}x \times L1x \times f_{SW}} \tag{8}$$

For this design two 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.19 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS54295 requires an input decoupling capacitor and a bulk capacitor may be required depending on the application. TI recommends a ceramic capacitor of at least 10 µF for the decoupling capacitor. Additionally, TI recommends 0.1-µF ceramic capacitors from VIN1 and VIN2 to ground to improve the stability and reduce the SWx node overshoots. The capacitors' voltage rating must be greater than the maximum input voltage.

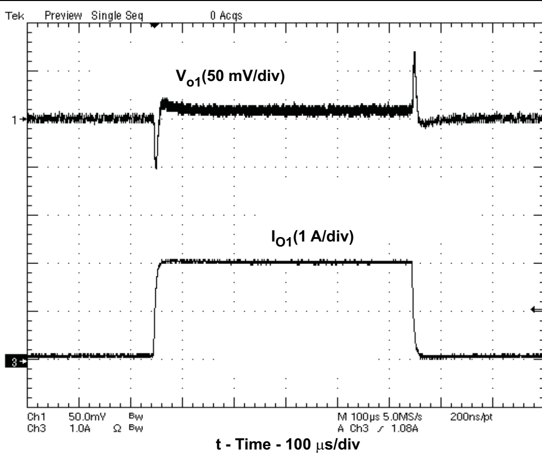
8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBSTx and SWx pins for proper operation. TI recommends ceramic capacitors with a dielectric of X5R or better.

8.2.2.5 VREG5 Capacitor Selection

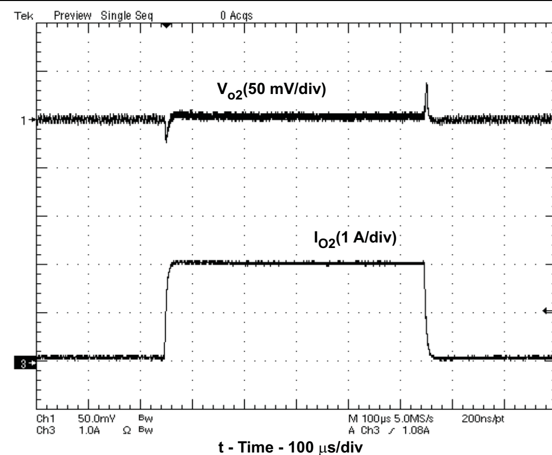
A 1-µF ceramic capacitor must be connected between the VREG5 and GND pins for proper operation. TI recommends a ceramic capacitor with a dielectric of X5R or better.

8.2.3 Application Curves



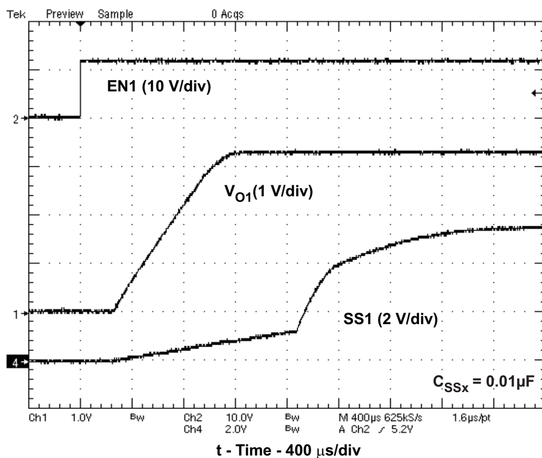
$V_{OUT}1 = 3.3$ V

Figure 17. 0-A to 2-A Load Transient Response



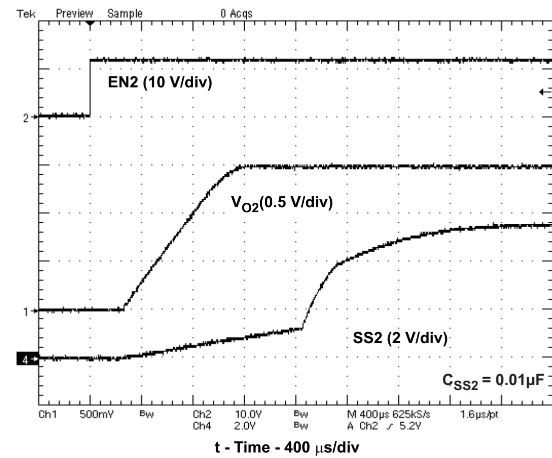
$V_{OUT}2 = 1.5$ V

Figure 18. 0-A to 2-A Load Transient Response



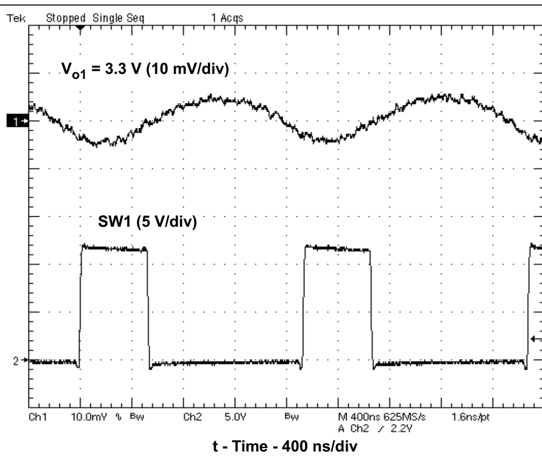
$V_{OUT}1 = 3.3$ V

Figure 19. Soft Start



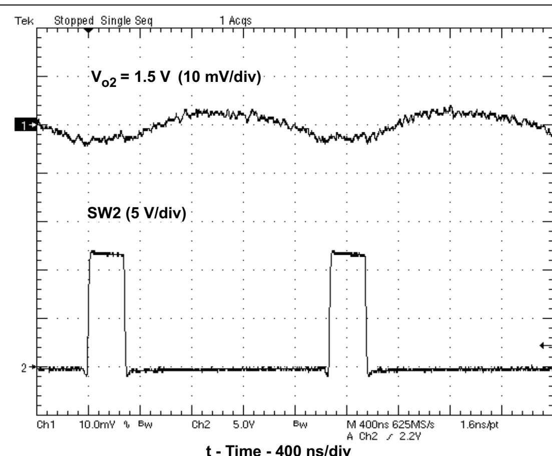
$V_{OUT}2 = 1.5$ V

Figure 20. Soft Start



$V_{OUT}1 = 3.3$ V $I_{OUT}1 = 2$ A

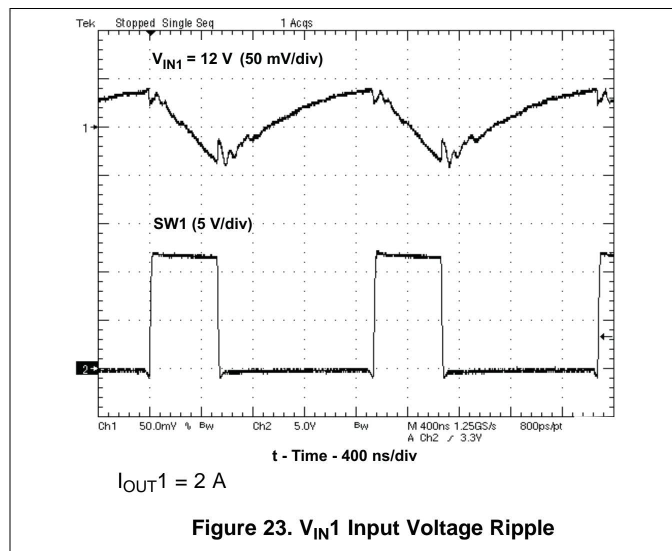
Figure 21. $V_{OUT}1$ Ripple Voltage



$V_{OUT}2 = 1.5$ V $I_{OUT}2 = 2$ A

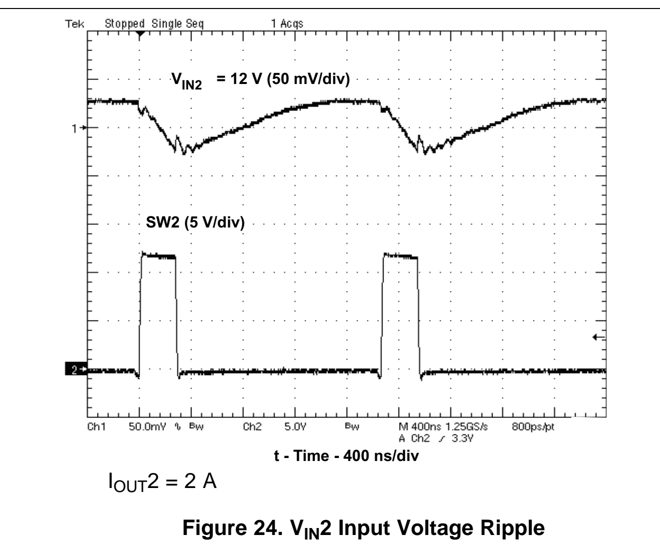
Figure 22. $V_{OUT}2$ Ripple Voltage

Copyright © 2011–2016, Texas Instruments Incorporated



$I_{OUT}1$ = 2 A

Figure 23. $V_{IN}1$ Input Voltage Ripple



$I_{OUT}2$ = 2 A

Figure 24. $V_{IN}2$ Input Voltage Ripple

9 Power Supply Recommendations

The TPS54295 is designed to operate with an input voltage supply from 4.5 V to 18 V. This input power supply must be well regulated. Bulk capacitance may be required in addition to the ceramic bypass capacitors if the input supply is placed more than a few inches from the device. A 47-μF electrolytic capacitor is a typical choice.

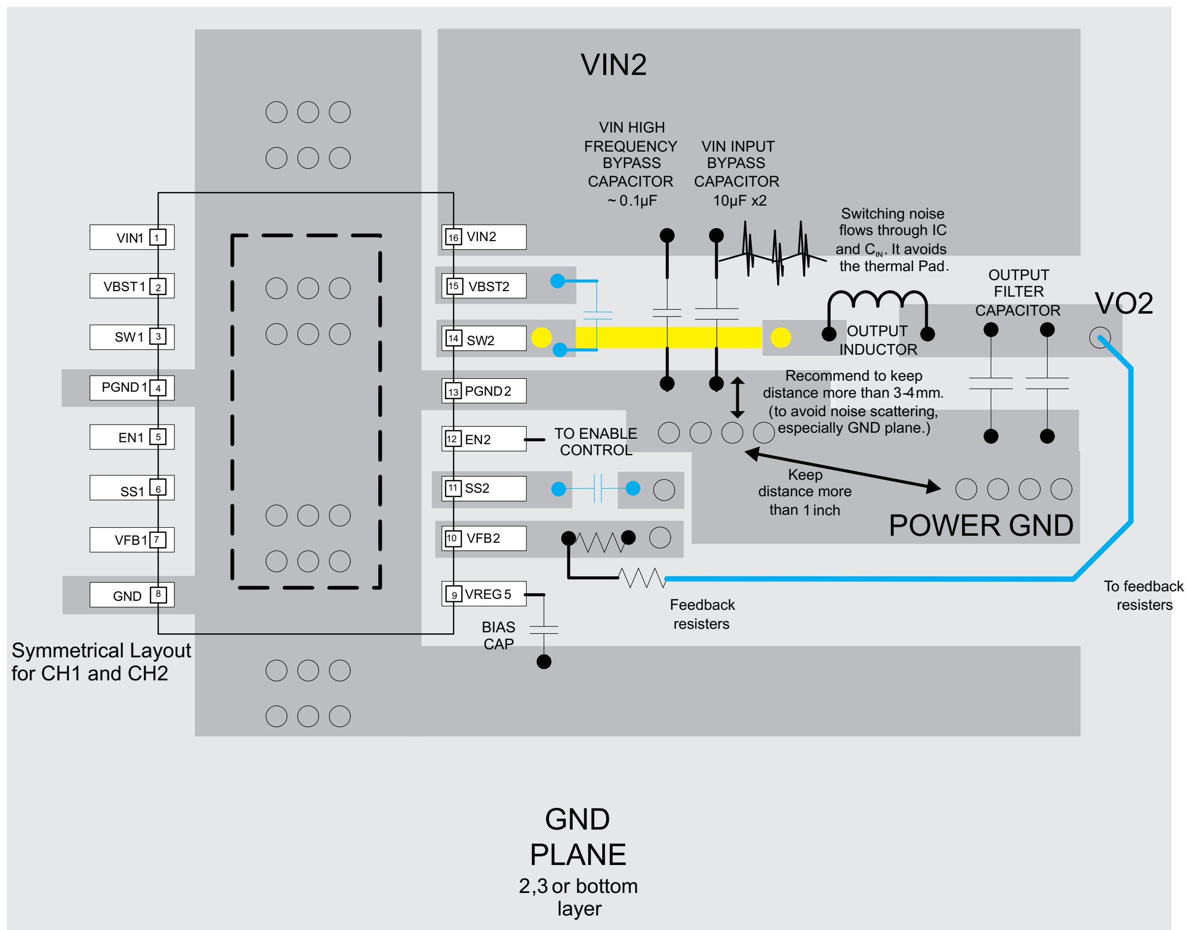
10 Layout

10.1 Layout Guidelines

1. Keep the input current loop as small as possible. And avoid the input switching current through the thermal pad.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching currents to flow under the device.
6. Keep the pattern lines for VINx and PGNDx broad.
7. Exposed pad of device must be soldered to PGND.
8. VREG5 capacitor must be placed near the device, and connected to GND.
9. Output capacitors must be connected with a broad pattern to the PGND.
10. Voltage feedback loops must be as short as possible, and preferably with ground shields.
11. Kelvin connections must be brought from the output to the feedback pin of the device.
12. Providing sufficient vias is preferable for VIN, SW, and PGND connections.
13. PCB pattern for VIN, SW, and PGND must be as broad as possible.
14. VIN capacitor must be placed as near as possible to the device.

Copyright © 2011–2016, Texas Instruments Incorporated

10.2 Layout Example



○ Via to GND Plane

- Blue parts can be placed on the bottom side
- Connect the SWx pins through another layer with the indcutor (yellow line)

Figure 25. TPS54295 PWP Package Layout

Copyright © 2011–2016, Texas Instruments Incorporated

Layout Example (continued)

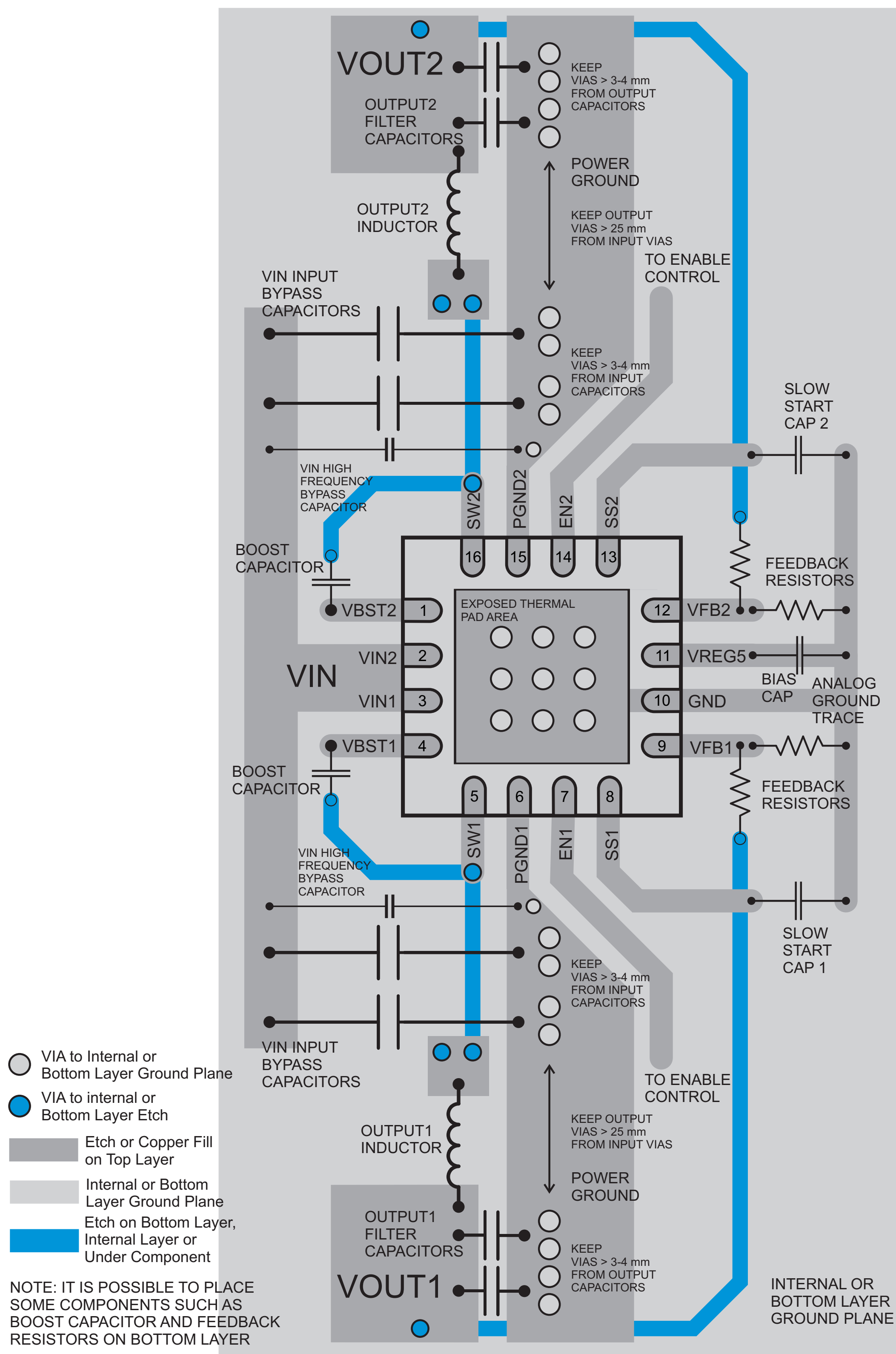


Figure 26. TPS54295 RSA Package Layout

Copyright © 2011–2016, Texas Instruments Incorporated

10.3 Thermal Considerations

This 16-pin PWP package incorporates an exposed thermal pad. The thermal pad must be soldered directly to the printed-circuit board (PCB). After soldering, the PCB is used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see *PowerPAD Thermally Enhanced Package* and *PowerPAD Made Easy*.

The exposed thermal pad dimensions for this package are shown in Figure 27.

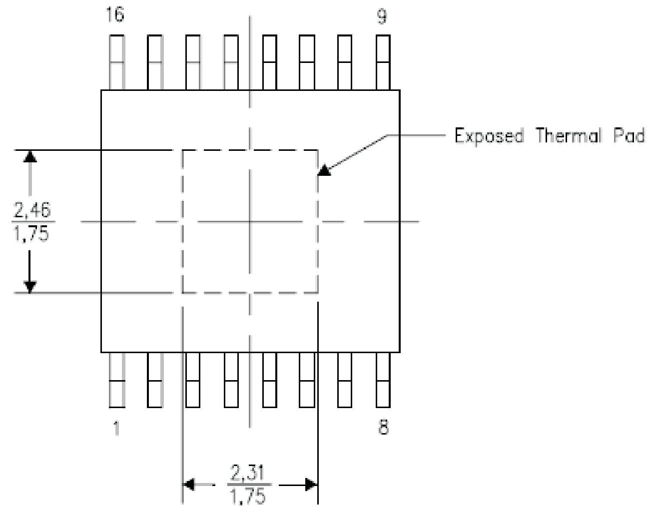


Figure 27. Thermal Pad Dimensions

版权 © 2011–2016, Texas Instruments Incorporated

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

WEBENCH 工具http://www.ti.com/lsds/ti/analog/webench/overview.page

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *《PowerPAD 耐热增强型封装》*（文献编号：SLMA002）
- *《PowerPAD 速成》*（文献编号：SLMA004）

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

D-CAP2, Eco-mode, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122
Copyright © 2016, 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54295PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54295	Samples
TPS54295PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54295	Samples
TPS54295RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 54295	Samples
TPS54295RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 54295	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

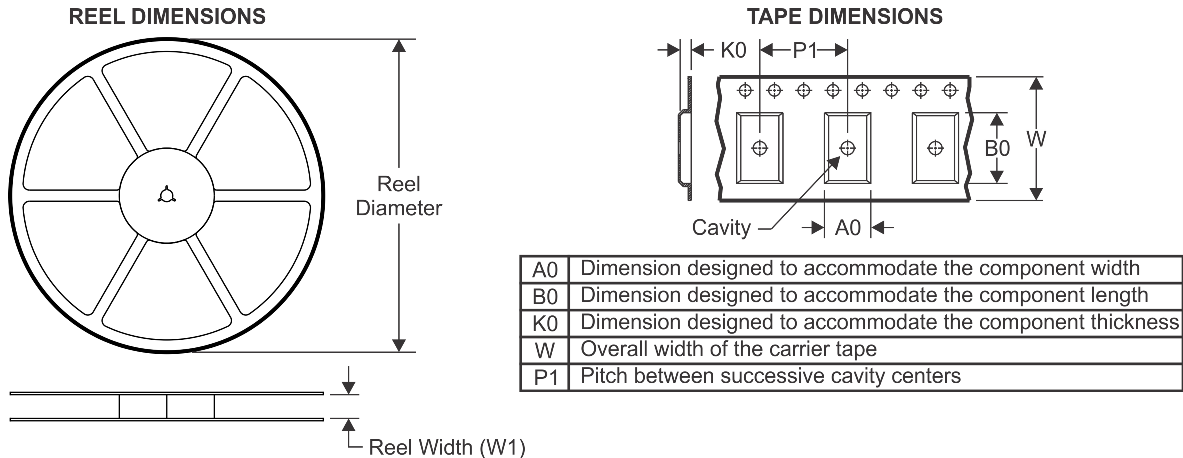
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

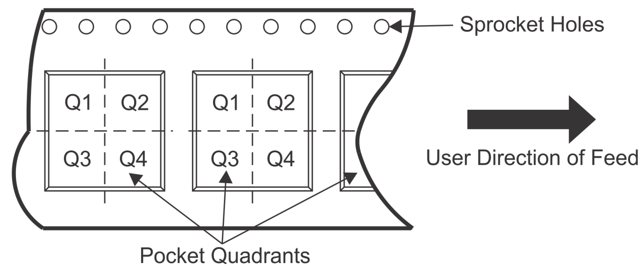
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

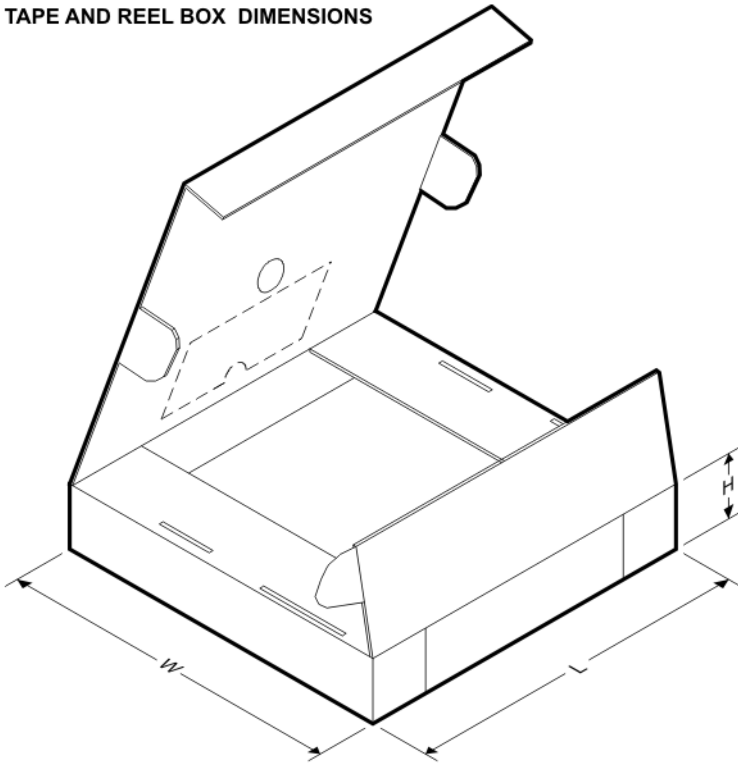




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54295PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54295PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54295RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54295RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

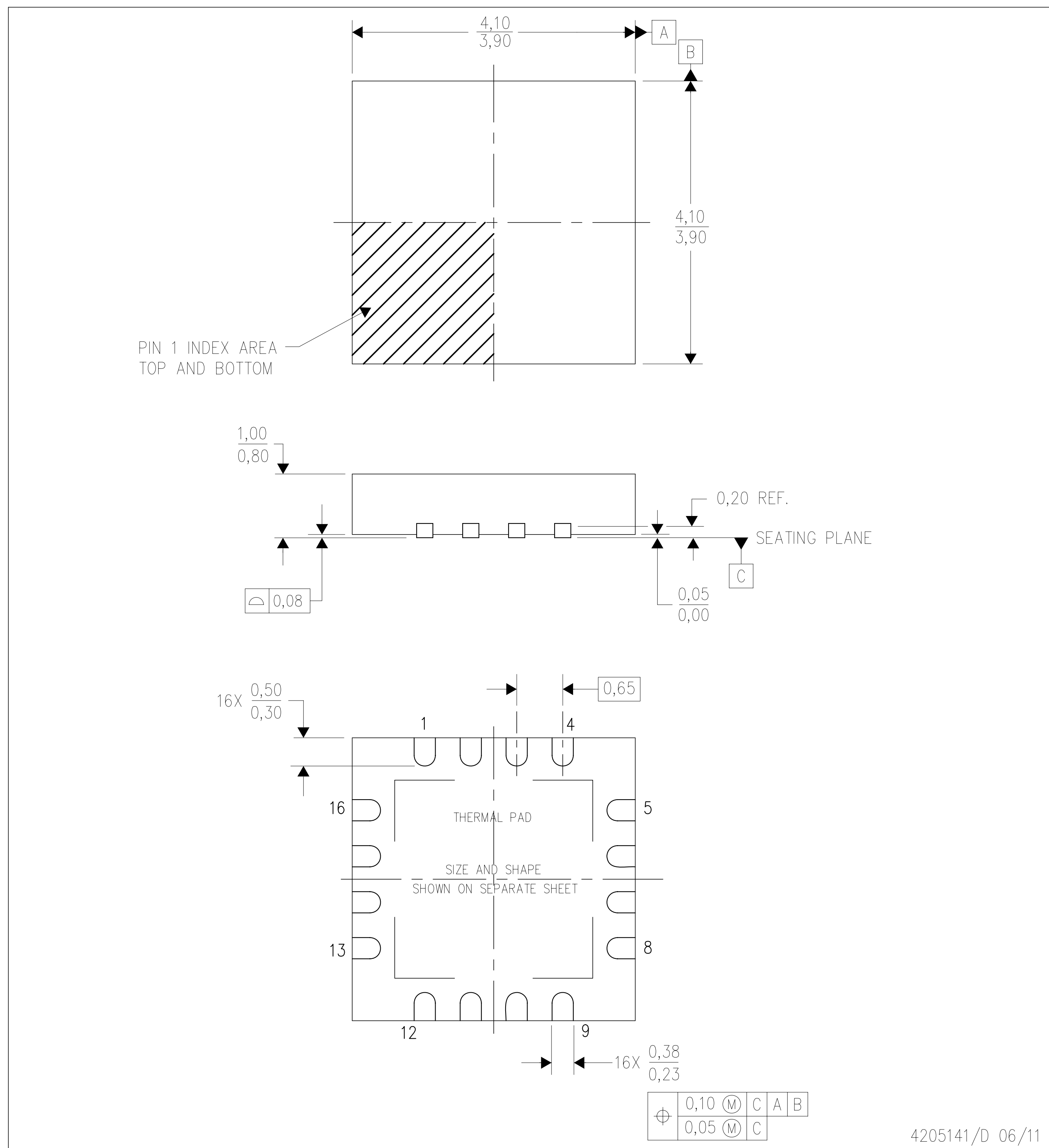
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54295PWPR	HTSSOP	PWP	16	2000	367.0	367.0	38.0
TPS54295PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
TPS54295RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
TPS54295RSAT	QFN	RSA	16	250	210.0	185.0	35.0

RSA (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

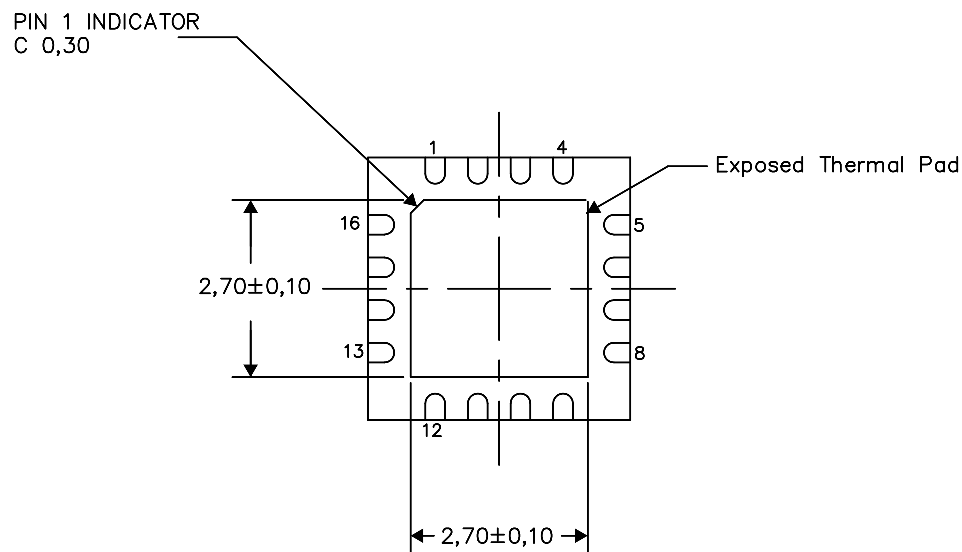
RSA (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

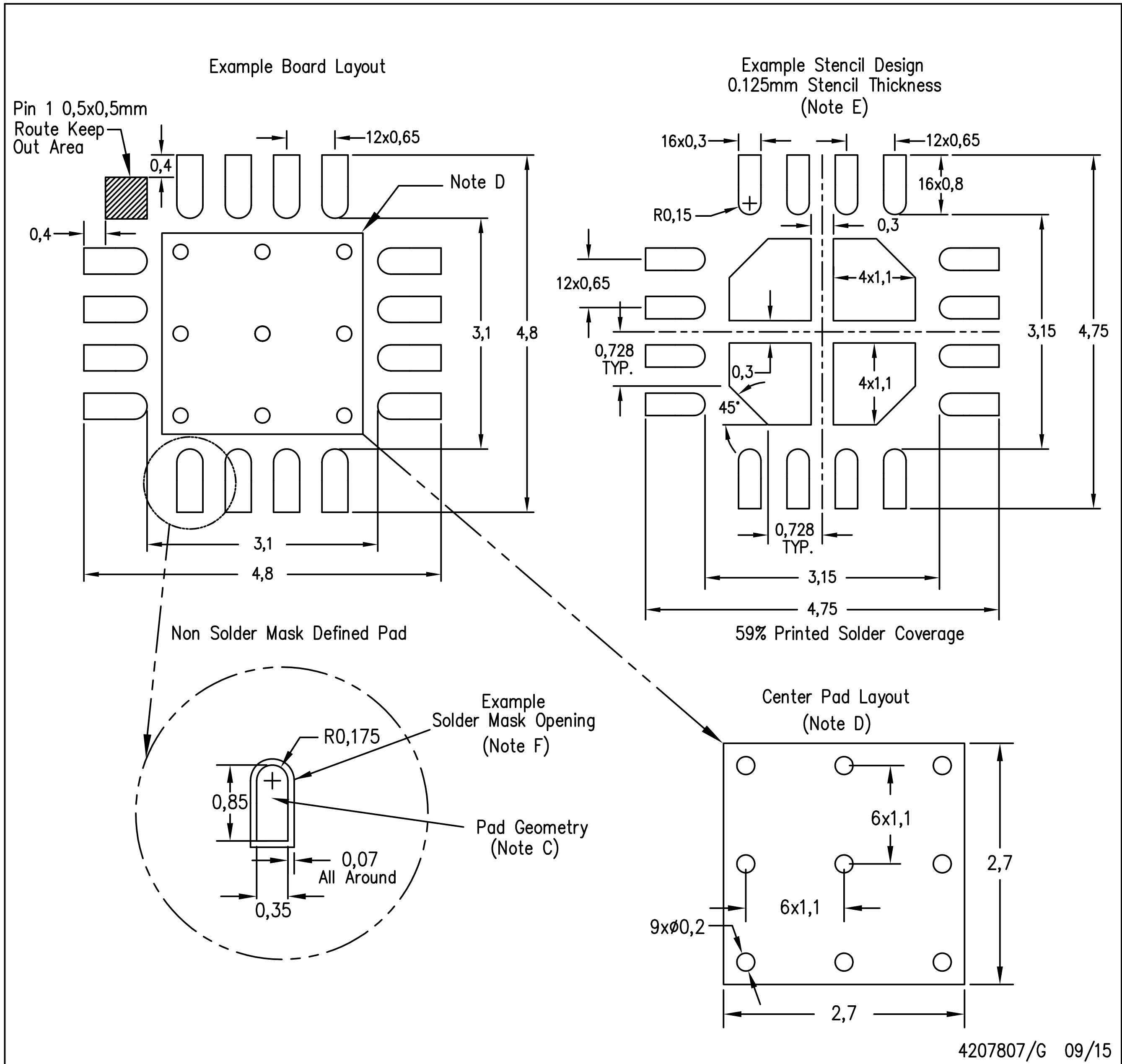


Exposed Thermal Pad Dimensions

4206364-2/O 09/15

NOTES:
A. All linear dimensions are in millimeters

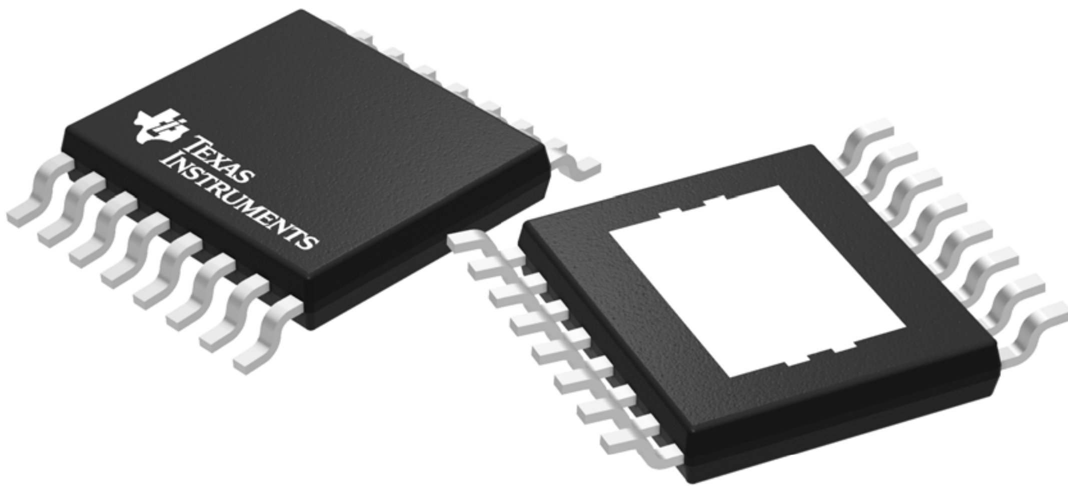
RSA (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

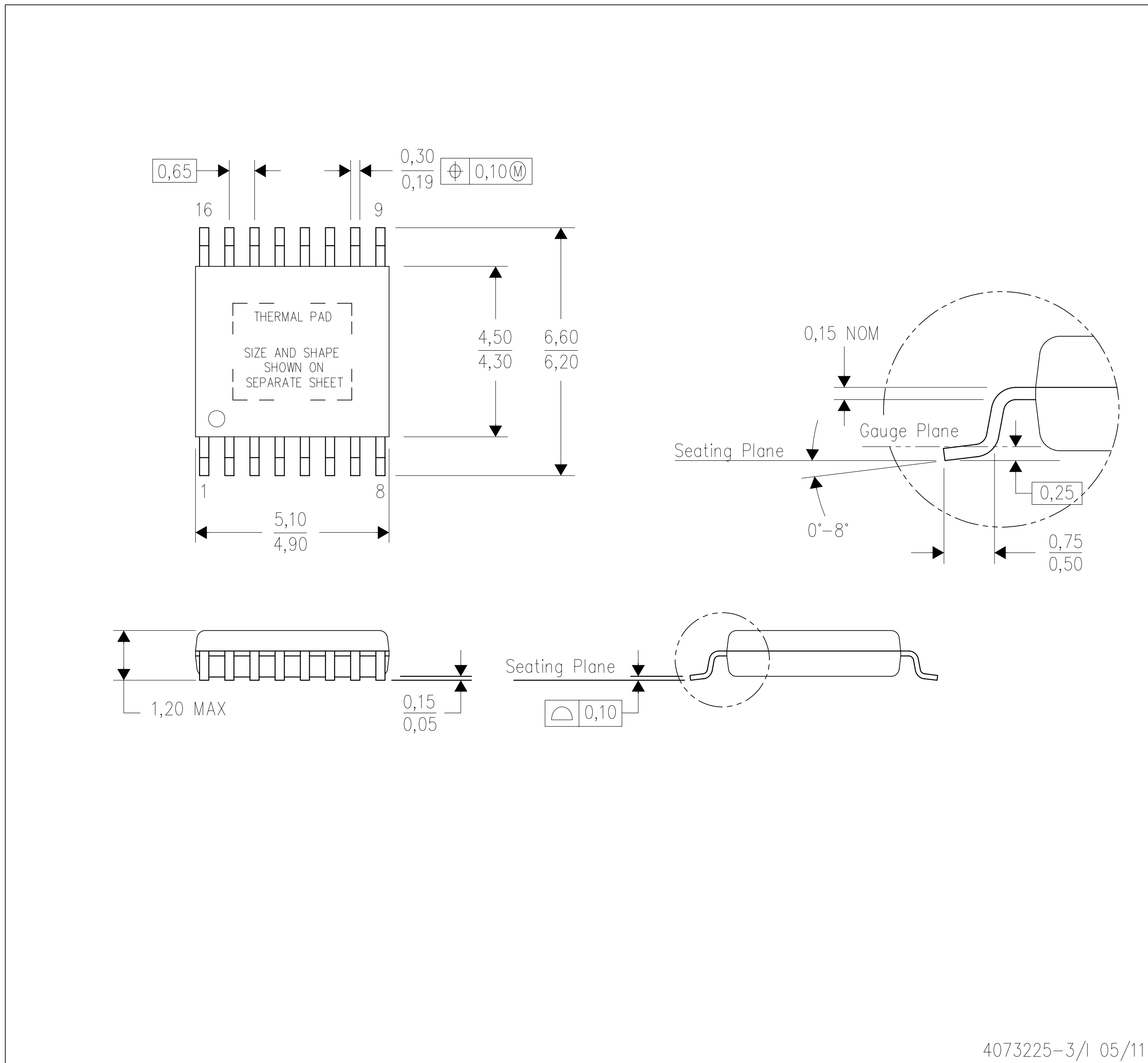
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073225-3/J

PWP (R-PDSO-G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

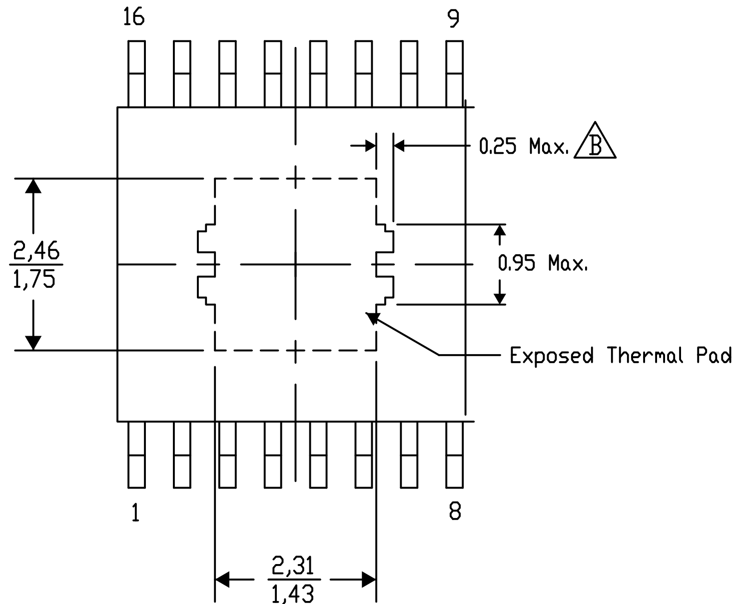
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

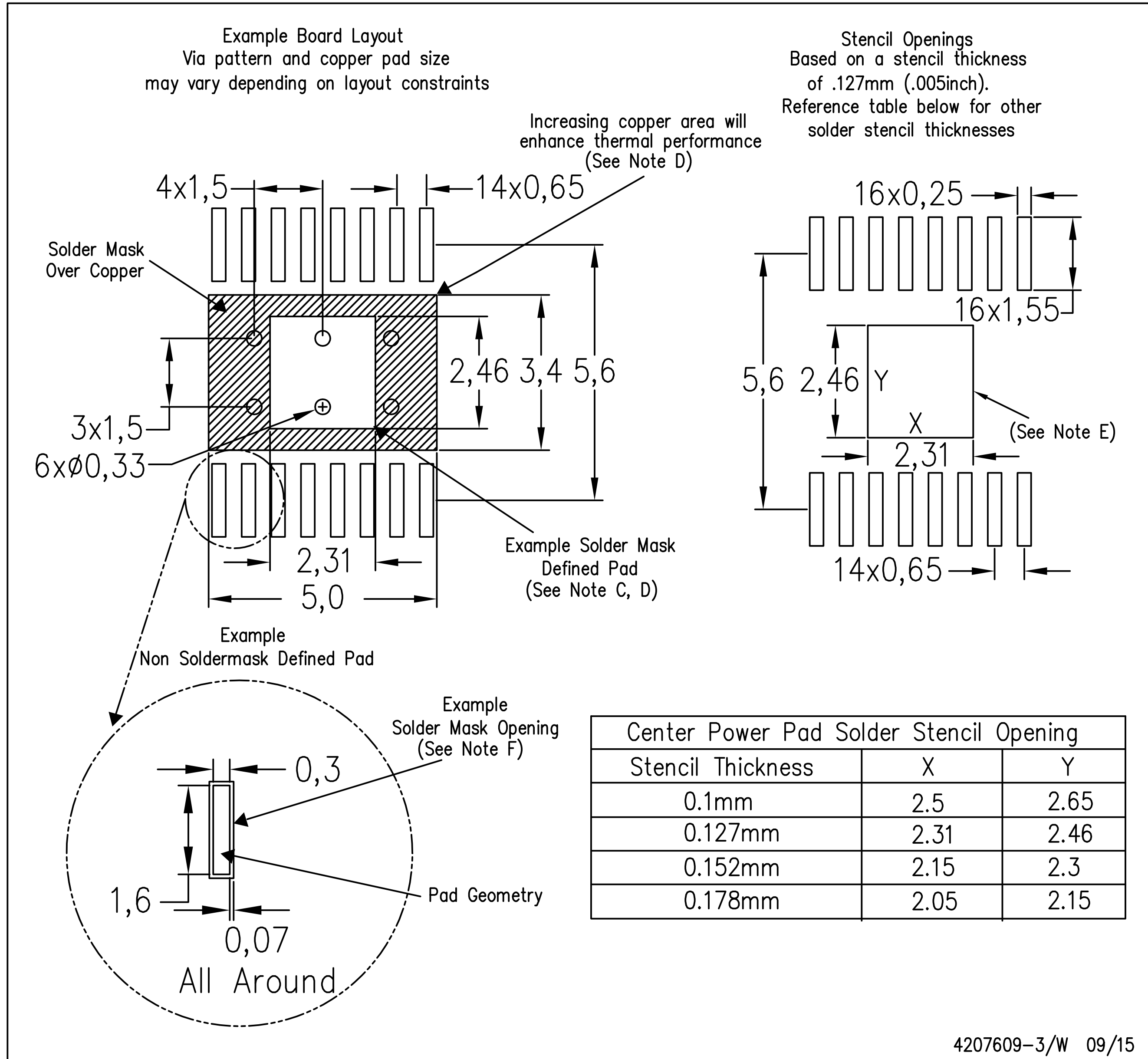
4206332-6/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE

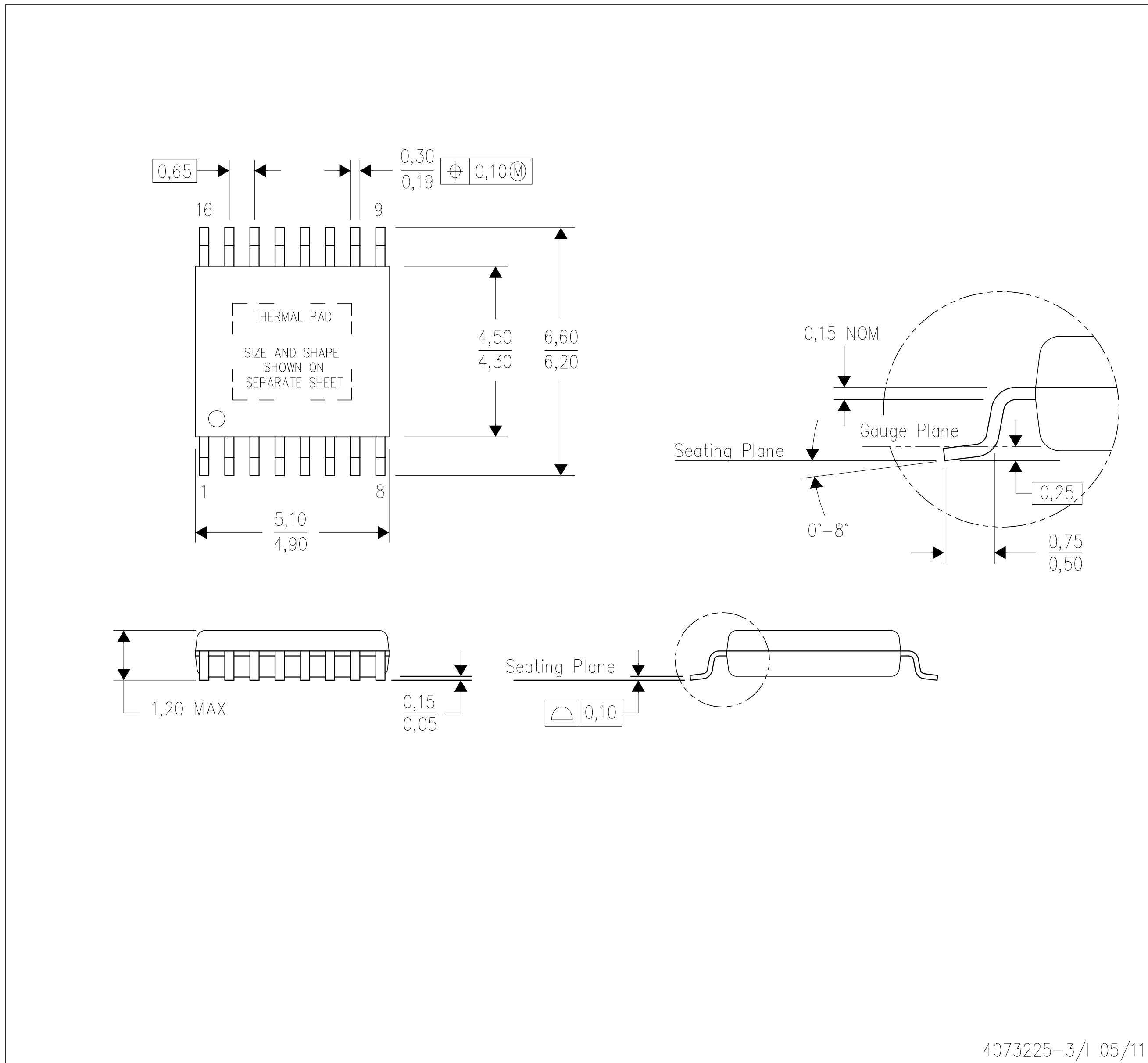


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

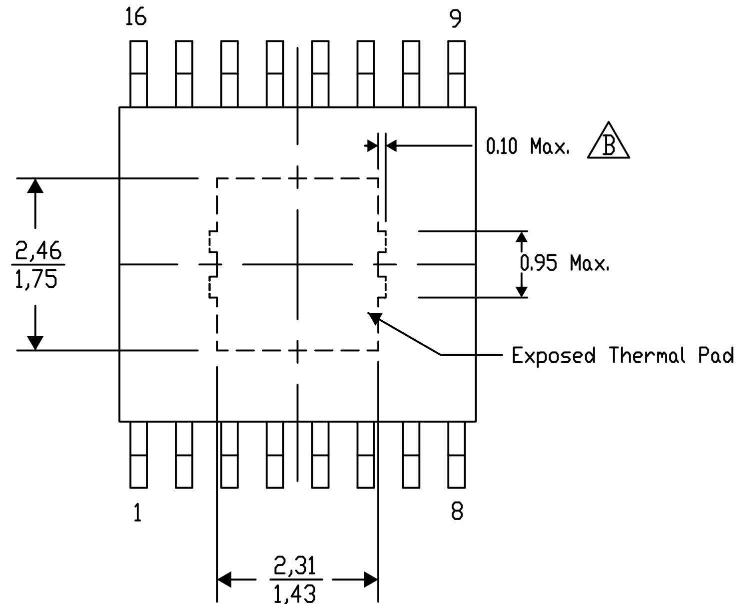
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-45/A0 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (http://www.ti.com/sc/docs/stdterms.htm) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权 负责并确保 应用的安全性， 及设计人员的 应用 （包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的 应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何 应用前， 将彻底测试该等 应用和 该等应用中所用 TI 产品的 功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用， 如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司