TEXAS INSTRUMENTS

TPS62180, TPS62182

SLVSBB8B –AUGUST 2014–REVISED MAY 2017

TPS6218x 4-V to 15-V, 6-A, 2-Phase Step-Down Converters with AEE™

1 Features

- Dual Phase Balanced Peak Current Mode
- Input Voltage Range: 4 V to 15 V
- Output Voltage Range: 0.9 V to 6 V
- Output Current up to 6 A
- Typical Quiescent Current of 28 µA
- Output Voltage Accuracy of ±1% (PWM Mode)
- Automatic Efficiency Enhancement (AEE™)
- Phase Shifted Operation
- Automatic Power Save Mode
- Adjustable Soft Start
- Power Good Output
- Undervoltage Lockout
- HICCUP Over Current Protection
- Pin-to-Pin Compatible with TPS62184
- Over Temperature Protection
- NanoFree™ 2.10 mm x 3.10 mm DSBGA Package
- Create a Custom Design Using the TPS62180 With the WEBENCH® Power Designer

2 Applications

- Low Profile POL Supply
- NVDC Powered Systems
- Dual/Triple Cell Li-ion Battery
- Ultra Portable/Embedded/Tablet PC
- Computing Network Solutions
- Micro Server, SSD

3 Description

The TPS6218x is a synchronous dual-phase step-down DC-DC converter for low profile power rails. It operates with two identical, current balanced phases that are peak current controlled enabling use in height limited applications.

With a wide operating input voltage range of 4 V to 15 V, the device is ideally suited for systems powered from multi-cell Li-Ion batteries or 12-V rails. The output current of 6 A is continuously provided by two phases of 3 A each, allowing the use of low profile external components. The phases operate out of phase, reducing switching noise significantly.

The TPS6218x automatically enters Power Save Mode to maintain high efficiency down to very light loads. It also incorporates an *Automatic Efficiency Enhancement (AEE™)* for the entire duty cycle range.

The device features a Power Good signal, as well as an adjustable soft start. The quiescent current is typically 28 µA, it is able to run in 100% mode, and it has no duty cycle limitation even at lowest output voltage.
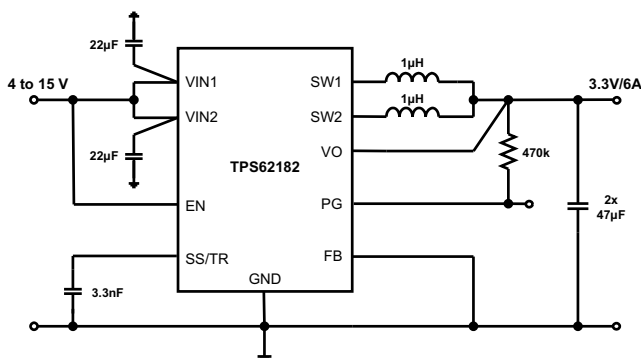
The TPS6218x, available in adjustable and fixed output voltage options, is packaged in a small 24-bump, 0.5 mm pitch DSBGA package.

Device Information[(1)]

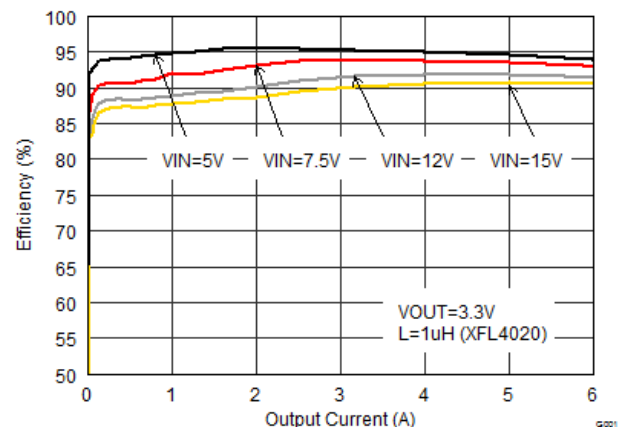| PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62180	DSBGA (24)	2.10 mm x 3.10 mm
TPS62182	DSBGA (24)	2.10 mm x 3.10 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

Copyright © 2017, Texas Instruments Incorporated

Efficiency vs Output Current

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2014) to Revision B   **Page**

Changes from Original (August 2014) to Revision A   **Page**

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	T$_J$
TPS62180	Adjustable	-40°C to 125°C
TPS62182	3.3 V	-40°C to 125°C

6 Pin Configuration and Functions

24-Pin DSBGA
YZF Package
(Top View - Left, Bottom View - Right)
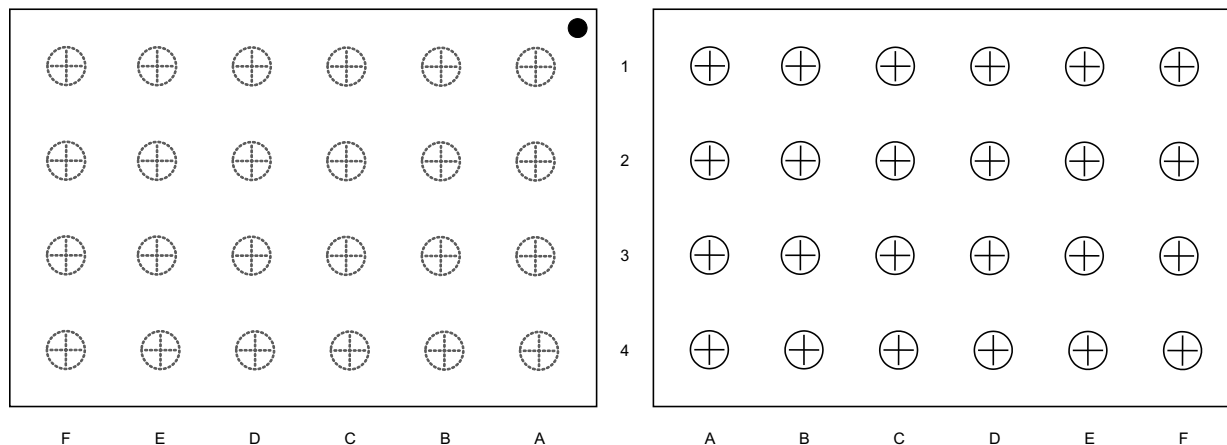
Pin Functions

PIN[1]		DESCRIPTION
NAME	**NUMBER**	
AGND	C4	Analog Ground. Connect on PCB directly with PGND.
EN	E4	Enable input (High = enabled, Low = disabled)
FB	B4	Output voltage feedback. Connect resistive voltage divider to this pin and AGND. On TPS62182, connect to AGND.
PG	F4	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor)
PGND	A3, B3, C3, D3, E3, F3	Common power ground.
SS/TR	D4	Soft-Start and Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time.
SW1	A2, B2, C2	Switch node for Phase 1 (master), connected to the internal MOSFET switches. Connect inductor 1 between SW1 and output capacitor.
SW2	D2, E2, F2	Switch node for Phase 2 (follower), connected to the internal MOSFET switches. Connect inductor 2 between SW2 and output capacitor.
VIN1	A1, B1, C1	Supply voltage for Phase 1.
VIN2	D1, E1, F1	Supply voltage for Phase 2.
VO	A4	Output Voltage Connection

(1)   For more information about connecting pins, see *Detailed Description* and *Application Information* sections.

7 Specifications

7.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
Pin voltage range[2]	VIN1, VIN2	−0.3	17	V
	EN, PG	−0.3	V_{IN} + 0.3	V
	SW1, SW2, (DC)	−0.3	V_{IN} + 0.3	V
	SW1, SW2, (AC, less than 10ns)[3]	−2	24.5	
	SS/TR	−0.3	V_{IN} + 0.3, but ≤ 7	V
	FB, VO	−0.3	7	V
Power good sink current	PG		10	mA
Operating junction temperature range	T_J	−40	150	°C
Storage Temperature Range	T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground pin.
(3) While switching.

7.2 ESD Ratings

		MIN	MAX	UNIT
V_{ESD}[1]	Human Body Model (HBM) ESD stress voltage[2]	−1	1	kV
	Charge device model (CDM) ESD stress voltage	−0.5	0.5	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Supply voltage range, V_{IN}		4		15	V
Output voltage range, V_{OUT}		0.9		6	V
Maximum Output current, $I_{OUT(max)}$	0.9V ≤ V_{OUT} ≤ 3.3V	6			A
	3.3V < V_{OUT}		6		
Operating junction temperature, T_J		−40		125	°C

7.4 Thermal Information

	THERMAL METRIC[1]	TPS6218x YZF (24 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.5	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.1	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over operating junction temperature range (T_J = −40°C to +125°C) and V_{IN} = 4 V to 15 V.
Typical values at V_{IN} = 12 V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			4		15	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, Device not switching, (T_J = −40°C to +85°C)			28	55	µA
I_{SD}	Shutdown current	EN = Low (≤ 0.3 V), (T_J = −40°C to +85°C)			2.8	15	µA
V_{UVLO}	Undervoltage lockout threshold [1]	Falling input voltage		3.5	3.6	3.7	V
		Hysteresis			300		mV
T_{SD}	Thermal shutdown	Rising junction temperature			160		°C
		Hysteresis			20		
CONTROL (EN, SS/TR, PG)							
V_{H_EN}	High-level input threshold voltage (EN)			0.97	1	1.03	V
V_{L_EN}	Low-level input threshold voltage (EN)			0.87	0.9	0.93	V
I_{LKG_EN}	Input leakage current (EN)	EN = V_{IN} or GND			0.01	1.2	µA
$I_{SS/TR}$	SS/TR pin source current			4.5	5	5.5	µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})		94%	96%	98%	
		Falling (%V_{OUT})		90%	92%	94%	
V_{OL_PG}	Power good output low voltage	I_{PG}= -2 mA				0.3	V
I_{LKG_PG}	Input leakage current (PG)				1	100	nA
POWER SWITCH							
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} = 7.5 V	Phase 1		27	65	mΩ
			Phase 2				
	Low-side MOSFET ON-resistance		Phase 1		21	45	mΩ
			Phase 2				
I_{LIM}	High-side MOSFET current limit	Each phase, V_{IN} = 7.5 V		4.0	4.7	5.5	A
T_{PSD}	Phase shift delay time	Phase 2 after Phase 1, PWM mode			250		ns
OUTPUT							
V_{REF}	Internal reference voltage			0.792	0.8	0.808	V
I_{LKG_FB}	Input leakage current (FB)	V_{FB} = 0.8 V			1	100	nA
$R_{DISCHARGE}$	Output discharge resistance	EN = Low			60		Ω
V_{OUT}	Output voltage range (TPS62180)	V_{IN} ≥ V_{OUT}		0.9		6	V
	Output voltage (TPS62182)				3.3		V
	Feedback voltage accuracy (TPS62180) [2]	PWM Mode, V_{IN} ≥ V_{OUT} + 1 V		−1%		1%	
		Power Save Mode, V_{OUT} = 3.3 V, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 2 x 47 µF, (T_J = −40°C to +85°C)		−1%		2%	
		Power Save Mode, V_{OUT} = 1.8 V, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 4 x 47 µF, (T_J = −40°C to +85°C)					
		Power Save Mode, V_{OUT} = 0.9 V, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 4 x 47 µF, (T_J = −40°C to +85°C)		−1%		3%	
	Output voltage accuracy (TPS62182) [2]	PWM Mode, V_{IN} ≥ V_{OUT} + 1 V		−1%		1%	
		Power Save Mode, I_{load} ≥ 1 mA, L = 1 µH, C_{OUT} = 2 x 47 µF, (T_J = −40°C to +85°C)		−1%		2%	
	Load regulation	V_{OUT} = 3.3 V, PWM Mode operation			0.04		%/A
	Line regulation	4 V ≤ V_{IN} ≤ 15 V, V_{OUT} = 3.3 V, I_{OUT} = 4 A			0.01		%/V
t_{HICCUP}	Hiccup on time				0.9		ms
	Hiccup off time				5		

(1) The minimum V_{IN} value of 4 V is not violated by UVLO threshold and hysteresis variations.
(2) The accuracy in Power Save Mode can be improved by increasing the output capacitor value, reducing the output voltage ripple.
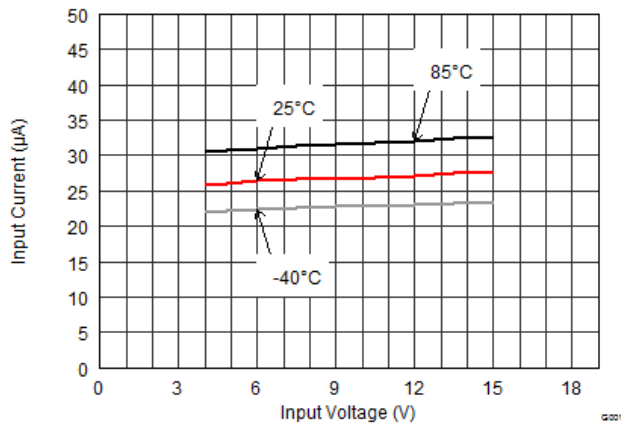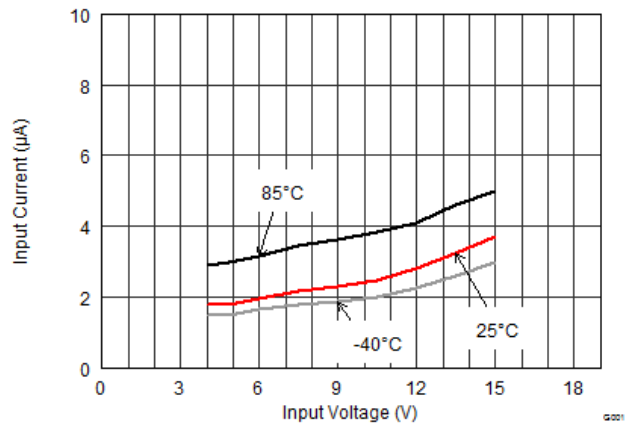
7.6 Typical Characteristics
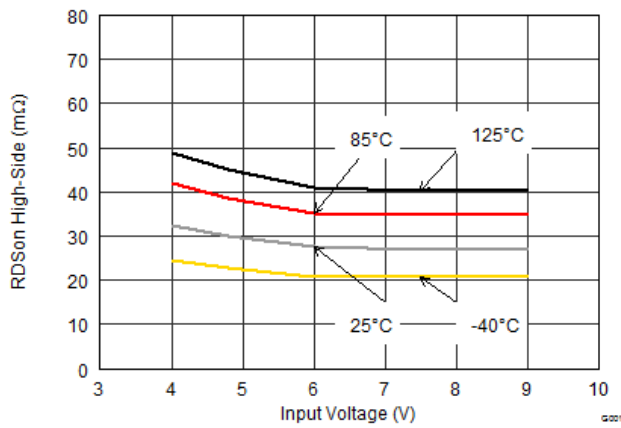

Figure 1. Quiescent Current

Figure 2. Shutdown Current

Figure 3. High-Side Switch Resistance

Figure 4. Low-Side Switch Resistance

Product Folder Links: *TPS62180 TPS62182*
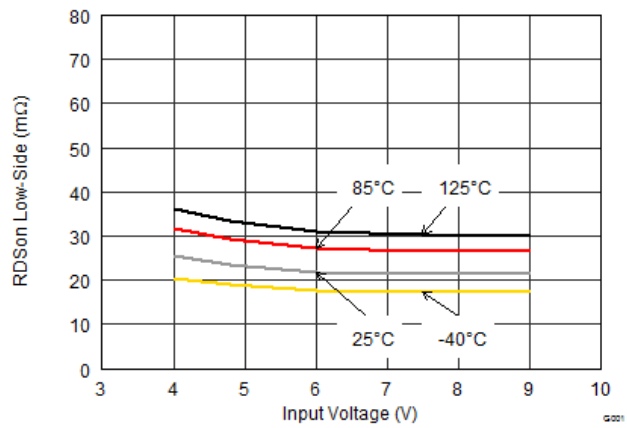
8 Detailed Description

8.1 Overview

The TPS6218x is a high efficiency synchronous switched mode step-down converter based on a peak current control topology. It is designed for smallest solution size low-profile applications, converting multi-cell Li-Ion supply voltages to output voltages of 0.9 V to 6 V. While an outer voltage loop sets the regulation threshold for the current loop based on the actual V_{OUT} level, the inner current loop adapts the peak inductor current for every switching cycle. The regulation network is internally compensated. The switching frequency is set by an OFF-time control and features Power Save Mode (PSM) and AEE™ (Automatic Efficiency Enhancement) to keep the efficiency high over the whole load current and duty cycle range. The switching frequency is set depending on V_{IN} and V_{OUT} and remains unchanged for steady state operating conditions.

The TPS6218x is a dual phase converter, sharing the load current among the phases. Identical in construction, the follower control loop is connected with a fixed delay to the master control loop. Both the phases use the same regulation threshold and cycle-by-cycle peak current setpoint. This ensures a phase-shifted as well as current-balanced operation. Using the advantages of the dual phase topology, a 6-A continuous output current is provided with high performance and smallest system solution size.

While the TPS62180 offers an adjustable output voltage, the TPS62182 supports a fixed 3.3-V output voltage, saving external components.

8.2 Functional Block Diagram
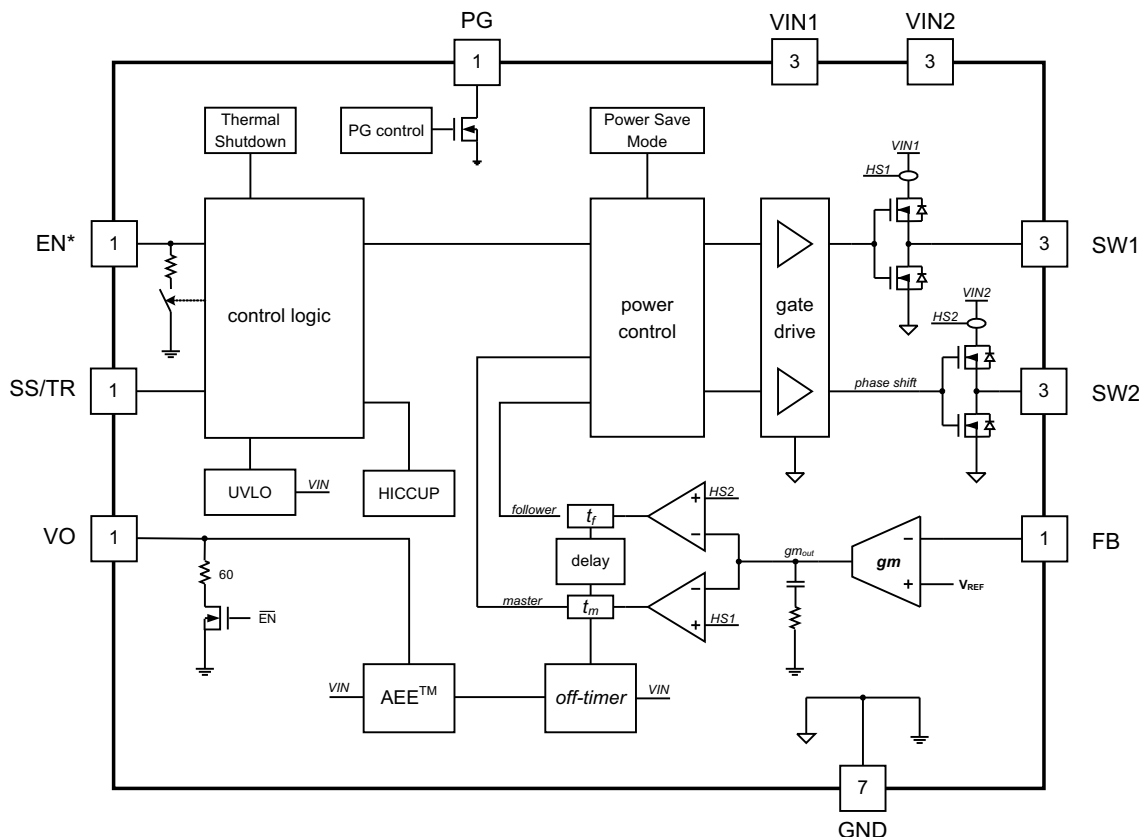
*Pin is connected to a pull down resistor internally
(see Feature Description section)

Copyright © 2017, Texas Instruments Incorporated

Figure 5. TPS62180 (Adjustable output voltage)

Functional Block Diagram (continued)

*Pin is connected to a pull down resistor internally
(see Feature Description section)

Copyright © 2017, Texas Instruments Incorporated
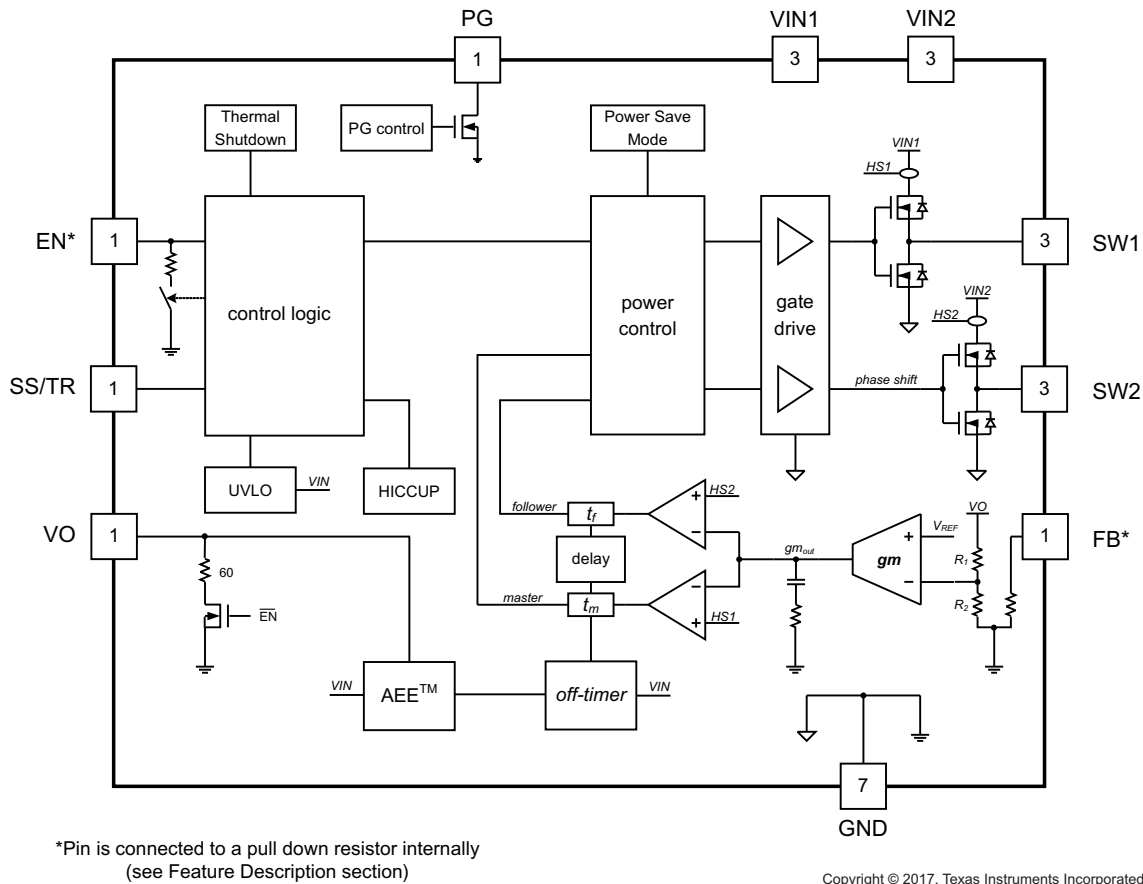
Figure 6. TPS62182 (Fixed output voltage)

8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

The device starts operation, when V_{IN} is present and Enable (EN) is set High. The EN threshold is 1 V for rising and 0.9 V for falling voltages, providing a threshold accuracy of ±3%. That makes it suitable for precise switching on and off in accurate power sequencing arrangements as well as for slowly rising EN control voltage signals (see Using the Accurate EN Threshold for more details).

The device is disabled by pulling EN Low. A discharge resistor of about 60 Ω is then connected to the output. At the EN pin, an internal pull down resistor of about 350 kΩ keeps the Low state, if EN gets high impedance or floating afterwards.

The EN pin can be connected to V_{IN} to always enable the device. A delay of 1 ms, after V_{IN} exceeds V_{UVLO}, ensures safe operating conditions before the device starts switching. If V_{IN} is already present, a soft start sequence is initiated about 100 µs after EN is pulled High.

8.3.2 Soft Start / Tracking (SS/TR)

The soft start circuit controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drop from high impedance power sources or batteries. When EN is set to start device operation, the device starts switching and V_{OUT} rises with a slope, controlled by the external capacitor connected to the SS/TR pin. There is no theoretical limit for the longest startup time. It is not recommended to leave the SS/TR pin floating, because V_{OUT} may overshoot. Typical startup operation is shown in Application Performance Curves.

Feature Description (continued)

The device can track an external voltage (see Tracking). The device can monotonically start into a pre-biased output.

8.3.3 Power Good (PG)

The TPS6218x has a built in power good (PG) function. The PG pin goes High, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low. The PG pin is an open drain output that requires a pull-up resistor and can sink typically 2 mA. If not used, the PG pin can be left floating or grounded.

Table 1. Power Good Pin Logic Table

Device Information		PG Logic Status	
		High Z	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7V$	√	

8.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) prevents misoperation of the device, if the input voltage drops below the UVLO threshold. It is set to 3.6 V typically with a hysteresis of typically 300mV. (See also Device Functional Modes).

8.3.5 Thermal Shutdown

The junction temperature T_J of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. Both the power FETs are turned off, the discharge resistor is connected to the output and the PG pin goes Low. Once T_J has decreased enough, the device resumes normal operation with Soft Start.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPS6218x is based on a predictive OFF-time peak current control topology, operating with PWM in continuous conduction mode for heavier loads. Since the OFF-time is automatically adjusted according to the actual V_{IN} and V_{OUT}, it provides highest efficiency over the entire input and output voltage range. The OFF-time is calculated as:

$$t_{OFF} = \left[\frac{V_{IN}}{5V_{OUT}} 500ns \right] + 50ns \tag{1}$$

While the OFF-time is predicted, the ON-time is set depending on the converter's duty cycle and calculated as:

$$t_{ON} = \frac{t_{OFF} \cdot V_{OUT}}{V_{IN} - V_{OUT}} \tag{2}$$

Device Functional Modes (continued)

Thereby the switching frequency is fixed for a given input and output voltage and is calculated as:

$$f_{SW} = \frac{1-D}{t_{OFF}} = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

(3)

Both the master and follower phases regulate to the same level of V_{OUT} with separate current loops, using the same peak current setpoint, cycle by cycle. This provides excellent peak current balancing, independent of inductor dc resistance matching. Since the follower phase operates with a fixed delay to the master phase, also cycle by cycle, phase shifted operation is obtained.

The device features an automatic transition into Power Save Mode, entered at light loads, running in discontinuous conduction mode (DCM).

8.4.2 Power Save Mode (PSM) Operation

As the load current decreases, the converter enters Power Save Mode operation. During PSM, the converter operates with a reduced switching frequency maintaining highest efficiency due to minimum quiescent current. Power Save Mode is based on a fixed peak current architecture, where the peak current (I_{PEAK}) is set depending on V_{IN}, V_{OUT}, and L. After each single pulse, a pause time until the internal V_{OUT_Low} level threshold is reached completes the switching cycle in PSM.

The switching frequency for PSM in one phase operation is calculated as :

$$f_{PSM} = \frac{2 I_{OUT} \cdot V_{OUT}\left(V_{IN} - V_{OUT}\right)}{L \cdot I_{PEAK}^2 \cdot V_{IN}}$$

(4)

Equation 4 shows the linear relationship of output current and switching frequency. Typical values of the fixed peak current are shown in Figure 7.
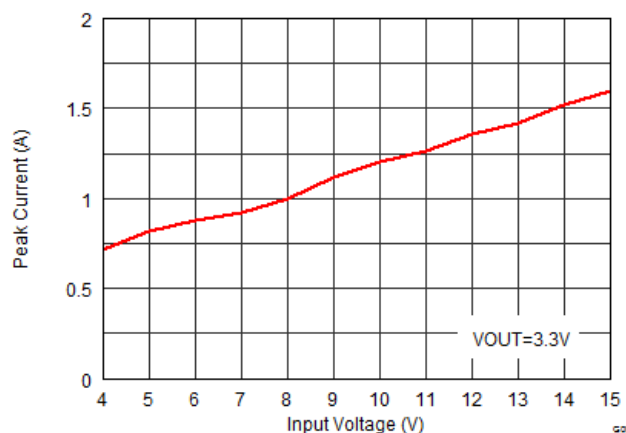

Figure 7. Typical Fixed Peak Current (I_{PEAK}) in Power Save Mode

If the load decreases to very light loads and only one phase is needed, either phase (master or follower) might be active. The load current level at which Power Save Mode is entered is calculated as follows:

Product Folder Links: *TPS62180 TPS62182*

Device Functional Modes (continued)

$$I_{load(PSM)} = \Delta I_L \tag{5}$$

Equation 7 is used to calculate ΔI_L.

8.4.3 Minimum Duty Cycle and 100% Mode Operation

When the input voltage comes close to the output voltage, the device enters 100% mode and both high-side FETs are continuously switched on as long as V_{OUT} remains below its setpoint. The minimum V_{IN} to maintain output voltage regulation is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left[\frac{R_{DS(ON)}}{2} + DCR_{L1} // DCR_{L2}\right] \tag{6}$$

This allows the conversion of small input to output voltage differences, for example for the longest operation time in battery powered applications. In 100% duty cycle mode, the low-side FET is switched off.

While the maximum ON-time is not limited, the AEE feature, explained in the next section, secures a minimum ON-time of about 100 ns.

8.4.4 Automatic Efficiency Enhancement (AEE™)

AEE™ provides highest efficiency over the entire input voltage and output voltage range by automatically adjusting the converter's switching frequency. This is achieved by setting the predictive off-time of the converter.

The efficiency of a switched mode converter is determined by the power losses during the conversion. The efficiency decreases, if V_{OUT} decreases and/or V_{IN} increases. In order to keep the efficiency high over the entire duty cycle range (V_{OUT}/V_{IN} ratio), the switching frequency is adjusted while maintaining the ripple current. The following equation shows the relation between the inductor ripple current, switching frequency and duty cycle.

$$\Delta I_L = V_{OUT} \cdot \left(\frac{1-D}{L \cdot f_{SW}}\right) = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \cdot f_{SW}}\right) \tag{7}$$

Efficiency increases by decreasing switching losses, preserving high efficiency for varying duty cycles, while the ripple current amplitude remains low enough to deliver the full output current without reaching current limit. The AEE™ feature provides an efficiency enhancement for various duty cycles, especially for lower Vout values, where fixed frequency converters suffer from a significant efficiency drop. Furthermore, this feature compensates for the very small duty cycles of high V_{IN} to low V_{OUT} conversion, which limits the control range in other topologies.

Figure 8 shows the typical switching frequency over the input voltage range.
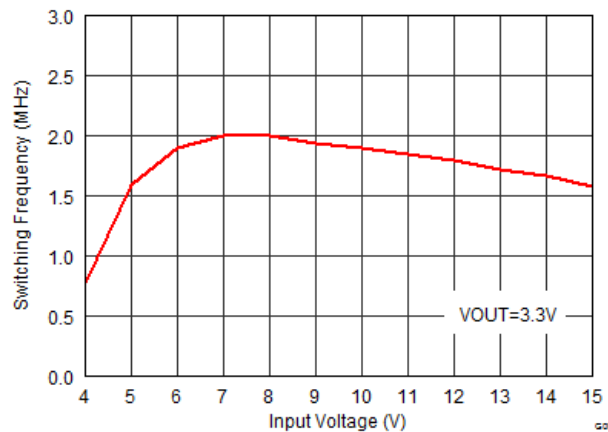
Device Functional Modes (continued)

Figure 8. Typical Switching Frequency vs Input Voltage

8.4.5 Phase-Shifted Operation

While, for a buck converter, the input current source provides the average current that is needed to support the output current, an input capacitance is needed to support pulse currents. One of the natural benefits of a two- (or multi-) phase converter is the possibility to operate out of phase, which decreases the pulse currents and switching noise. In PWM mode, the TPS6218x devices run with a fixed delay of typically 250 ns between the phases. This ensures that the phases run phase-delayed, limiting input RMS current and corresponding noise. If in PSM, both phases run, the phase delay is about 100 ns.

8.4.6 Current Limit, Current Balancing, and Short Circuit Protection

Each phase has a separate integrated peak current limit. While its minimum value limits the output current of the phase, the maximum number gives the current that must be considered to flow in any operating case. If the current limit of a phase is reached, the peak current setpoint is unable to increase further. The device provides its maximum output current. Detecting this heavy load or short circuit condition for about 0.9 ms, the device switches off for about 5 ms and then restarts again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

The two phases are peak current balanced with a variation within about ±10% at 6-A output current (see Figure 9). Since the control topology does not depend on inductor or output current measurements, the current balancing accuracy is independent of inductor matching (binning) and does not need matched power routing.
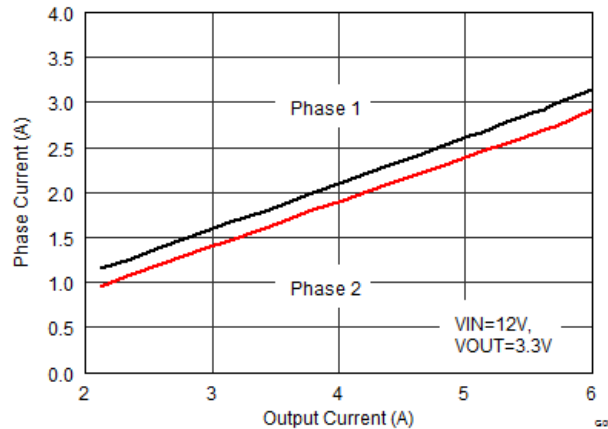
Device Functional Modes (continued)

Figure 9. Typical Current Balancing vs Load Current

8.4.7 Tracking

V_{OUT} can track a voltage that is applied at the SS/TR pin. The tracking range at the SS/TR pin is 50 mV to 1.2 V and the FB pin voltage tracks this as given in Equation 8:

$$V_{FB} \approx 0.64 \cdot V_{SS/TR}$$

(8)

Due to the factor of about 0.64, the minimum output voltage for tracking is 1.25 V. Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and the device goes to normal regulation. This works for falling tracking voltage as well. If, in this case, the SS/TR voltage decreases, the device does not sink current from the output. Thus, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN}+0.3 V.

Note: If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

8.4.8 Operation with Fixed V_{OUT}

The TPS62182 provides a fixed output voltage of 3.3 V (±1%). In this case, the feedback divider is integrated and the FB pin is internally connected to GND with a resistor of about 350 kΩ. It is recommended to connect the FB pin to PCB ground to improve thermal behavior.

# 9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS62180/2 are switched mode step-down converters, able to convert a 4-V to 15-V input voltage into a lower 0.9-V to 6-V output voltage, providing up to 6 A. It needs a minimum amount of external components. Apart from the LC output filter and the input capacitors only an optional pull-up resistor for Power Good (PG) and a small capacitor for adjustable soft start are used. The TPS62180 with an adjustable output voltage needs an additional resistive divider to set the output voltage level.

9.2 Typical Applications

9.2.1 Typical TPS62180 Application
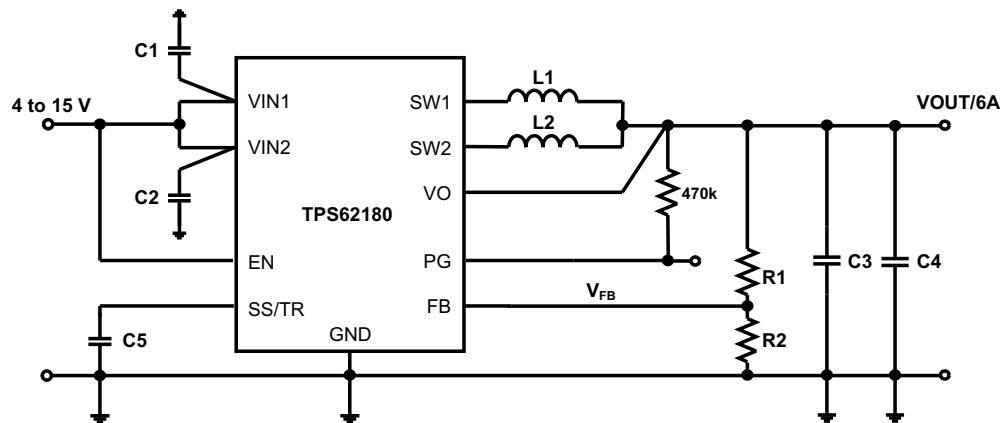
Figure 10. Typical 4-V to 15-V Input, 6A Converter

9.2.1.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. The component selection is given in Table 2 and gives a total solution size of about 99 mm^2 with a maximum height of 2.1 mm:

Table 2. Components Used for Application Characteristics

REFERENCE NAME	DESCRIPTION / VALUE	MANUFACTURER
TPS62180YZF	2 phase step down converter, 2 x 3 mm WCSP	Texas Instruments
L1, L2	Inductor XFL4020-102ME, 1 µH ±20%, 4 x 4 x 2.1 mm	Coilcraft
C1, C2	Ceramic capacitor GRM21BR61E226ME44, 2 x 22 µF, 25 V, X5R, 0805	muRata
C3, C4	Ceramic capacitor GRM21BR60J476ME15, 2 x 47 µF, 6.3 V, X5R, 0805	muRata
C5	Ceramic capacitor, 3.3 nF	Standard
R1	Chip resistor, value depending on V_{OUT}	Standard
R2	Chip resistor, value depending on V_{OUT}	Standard
R3	Chip resistor, 470 kΩ, 0603, 1/16 W, 1%	Standard

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62180 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:
- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Programming the Output Voltage

The output voltage of the TPS62180 is programmed using an external resistive divider. While the voltage at the FB pin is regulated to 0.8 V, the output voltage range is specified from 0.9 up to 6 V. The value of the output voltage is set by selection of the resistive divider (from VOUT to FB to AGND) from Equation 9.

$$\frac{R_1}{R_2} = \frac{V_{OUT}}{V_{FB}} - 1$$

(9)

The current through those resistors contributes to the light load efficiency, which makes larger resistor values beneficial. However, to get sufficient noise immunity these values should not be oversized. Using this, the resistor values are calculated by converting Equation 9 as follows:

$$R_2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8V}{5\mu A} = 160k\Omega$$

(10)

Inserting the R_2 value in Equation 11, R_1 can be obtained.

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

(11)

Calculating for V_{OUT} = 3.3 V gives R_1 = 500 kΩ. Using standard resistor values R_1 = 470 kΩ and R_2 = 150 kΩ are chosen.

For applications requiring lowest current consumption, the use of fixed output voltage options is recommended. Using the TPS62182, the FB pin can be left floating, but it is recommended to connect it to AGND which decreases thermal resistance.

In case the FB pin of the adjustable output voltage version gets opened or an over voltage appears at the output, an internal clamp limits the output voltage to about 7.4 V.

9.2.1.2.3 Output Filter Selection

Since the TPS6218x is compensated internally, it is optimized for a range of external component values, which is specified below. Table 3 and Table 4 are used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

Table 3. Recommended LC Output Filter Combinations for $V_{OUT} \geq 1.8$ V[1]

	2 x 47 µF	4 x 47 µF	6 x 47 µF	8 x 47 µF
0.47 µH				
1.0 µH	√	√	√	√
1.5 µH				

(1) The values in the table are the nominal values of inductors and ceramic capacitors. The effective capacitance can vary by +20 and −60%.

Table 4. Recommended LC Output Filter Combinations for $V_{OUT} < 1.8$ V[1]

	2 x 47 µF	4 x 47 µF	6 x 47 µF	8 x 47 µF
0.68 µH				
1.0 µH		√	√	
1.5 µH				

(1) The values in the table are nominal values of inductors and ceramic capacitors. The effective capacitance can vary by +20 and −40%.

For the output capacitors, a voltage rating of 6.3 V and an X5R dielectric are chosen. If space allows for higher voltage rated capacitors in larger case sizes, the dc bias effect is lowered and the effective capacitance value increases.

9.2.1.2.4 Inductor Selection

The TPS6218x is designed to work with two inductors of 1 µH nominal. They have to be selected for adequate saturation current and a low dc resistance (DCR). The minimum inductor current rating $I_{L(min)}$ that is needed under static load conditions is calculated using Equation 12 and Equation 13. A current imbalance of 10% at most is incorporated.

$$I_{peak(max)} = I_{L(min)} = \frac{1.1 \cdot I_{OUT(max)}}{2} + \frac{\Delta I_{L(max)}}{2}$$

(12)

$$\Delta I_{L(max)} = V_{OUT} \cdot \left(\frac{1 - \dfrac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \cdot f_{SW}} \right)$$

(13)

This calculation gives the minimum saturation current of the inductor needed and an additional margin of about 20% is recommended to cover dynamic overshoot due to load transients. For low profile solutions, the physical inductor size and the power losses have to be traded off. Smallest solution size (for example with chip inductors) are less efficient than bigger inductors with lower losses due to lower DCR and/or core losses. The following inductors have been tested with the TPS6218x:

Product Folder Links: *TPS62180 TPS62182*

Table 5. List of Inductors

TYPE	INDUCTANCE [µH]	CURRENT RATING MIN/TYP [A] [1]	DCR MAX [mΩ]	DIMENSIONS (LxBxH) [mm]	MANUFACTURER
DFE201612E-1R0M	1 ±20%	4.0/4.4	48	2.0 x 1.6 x 1.2	TOKO
DFE252012F-1R0M	1 ±20%	4.7/5.3	40	2.5 x 2.0 x 1.2	TOKO
DFE252012P-1R0M	1 ±20%	3.8/4.5	42	2.5 x 2.0 x 1.2	TOKO
PIFE32251B-1R0MS	1 ±20%	4.2/4.7	42	3.2 x 2.5 x 1.2	CYNTEC
PIME031B-1R0MS	1 ±20%	4.5/5.4	55	3.7 x 3.3 x 1.2	CYNTEC
PISB25201T-1R0MS	1 ±20%	3.6/3.9	62	2.5 x 2.0 x 1.0	CYNTEC
IHLP1212AB-11	1 ±20%	/5.0	37.5	3.6 x 3.0 x 1.2	VISHAY
IHLP1212AE-11	1 ±20%	/5.3	33	3.6 x 3.0 x 1.5	VISHAY
XFL4015-122ME_	1.2±20%	/4.5	20.7	4.0 x 4.0 x 1.5	COILCRAFT
XFL4020-102ME_	1 ±20%	/5.4	11.9	4.0 x 4.0 x 2.1	COILCRAFT
TFM201610-GHM	1 ±20%	3.6/3.8	60	2.0 x 1.6 x 1.0	TDK
TFM252010-GHM	1 ±20%	3.5/4.0	56	2.5 x 2.0 x 1.0	TDK

(1) I_{SAT} at 30% drop of inductance ($\Delta I_L / I_L$).

The TPS6218x is not designed to operate with only one inductor.

9.2.1.2.5   Output Capacitor Selection

The TPS6218x provides a wide output voltage range of 0.9 V to 6 V. While stability is a critical criteria for the output filter selection, the output capacitor value also determines transient response behavior, ripple and accuracy of V_{OUT}. Table 6 gives recommendations to achieve various transient design targets using 1-µH inductors and small sized output capacitors (see Table 2).

Table 6. Recommended Output Capacitor Values

OUTPUT VOLTAGE [V]	LOAD STEP [A]	(NOMINAL) CAPACITOR VALUE[1]	TYPICAL TRANSIENT RESPONSE ACCURACY	
			±mV	±%
0.9[2]	2-6-2[3]	4 x 47 µF	90	10
		6 x 47 µF	70	8
1.8	2-6-2[3]	2 x 47 µF	150	8
		4 x 47 µF	120	7
		8 x 47 µF	90	5
3.3	2-6-2[3]	2 x 47 µF	170	5
		4 x 47 µF	135	4
		8 x 47 µF	100	3

(1)   Ceramic capacitors have a dc bias effect where the effective capacitance differs significantly from the nominal value, depending on package size, voltage rating and dielectric material.
(2)   For output voltages < 1.8V an additional feedforward capacitor of 82pF, parallel to R_1 is recommended to increase stability margin at heavy load steps.
(3)   The transient load step is tested with 1-µs/step rising/falling slopes.

The architecture of the TPS6218x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectrics. Using even higher values than demanded for stability and transient response has further advantages like smaller voltage ripple and tighter dc output accuracy in Power Save Mode.

Product Folder Links: *TPS62180 TPS62182*

9.2.1.2.6 Input Capacitor Selection

The input current of a buck converter is pulsating. Therefore, a low ESR input capacitor is required to prevent large voltage transients and provide peak currents. The recommended value for most applications is 2 x 22 µF, split between the VIN1 and VIN2 inputs and placed as close as possible to these pins and PGND pins. If additional capacitance is needed, it can be added as bulk capacitance. To ensure proper operation, the effective capacitance at the VIN pins must not fall below 2 x 2 µF (close) + 10 µF bulk (effective capacitances).

Low ESR multilayer ceramic capacitors are recommended for best filtering. Increasing with input voltage, the dc bias effect reduces the nominal capacitance value significantly. To decrease input ripple current further, larger values of input capacitors can be used.

9.2.1.2.7 Soft Start Capacitor Selection

The TPS6218x provides a user programmable soft start time. A constant current source of 5 µA, internally connected to the SS/TR pin, allows control of the startup slope by connecting a capacitor to this pin. The current source charges the capacitor and the soft start time is given by:

$$C_{SS} = t_{SS} \cdot \frac{5 \mu A}{1.25 V}$$

(14)

where C_{SS} is the soft-start capacitance required at the SS/TR pin and t_{ss} is the resulting soft-start ramp time.

The SS/TR pin should not be left floating and a minimum capacitance of 220 pF is recommended. Using Equation 14, and inserting t_{SS} = 750 µs, a value of 3 nF is calculated. 3.3 nF is chosen as a standard value for this example.

Product Folder Links: *TPS62180 TPS62182*

9.2.1.3 Application Performance Curves

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

V_{OUT} = 6 V
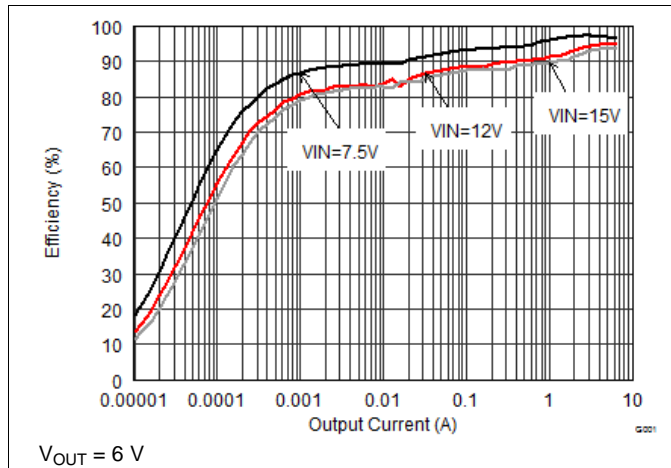
Figure 11. Efficiency vs Load Current

V_{OUT} = 6 V
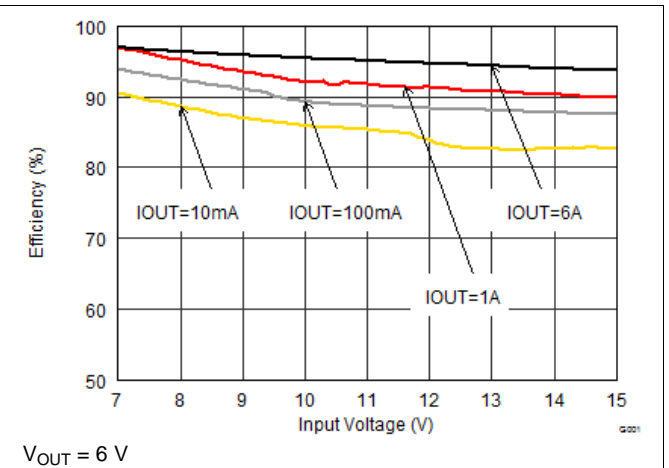
Figure 12. Efficiency vs Input Voltage

V_{OUT} = 3.3 V
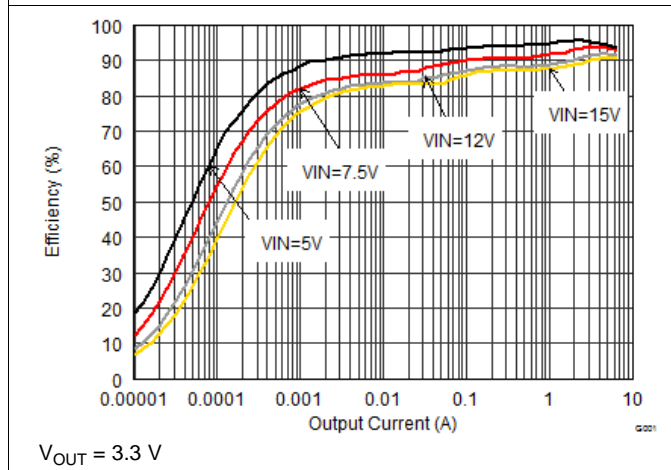
Figure 13. Efficiency vs Load Current

V_{OUT} = 3.3 V
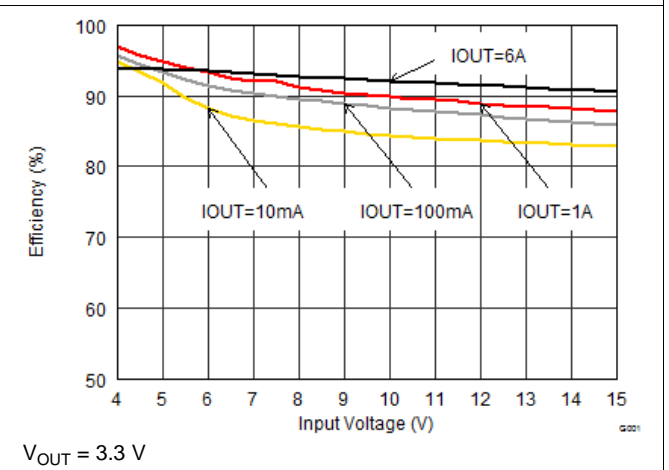
Figure 14. Efficiency vs Input Voltage

V_{OUT} = 1.8 V
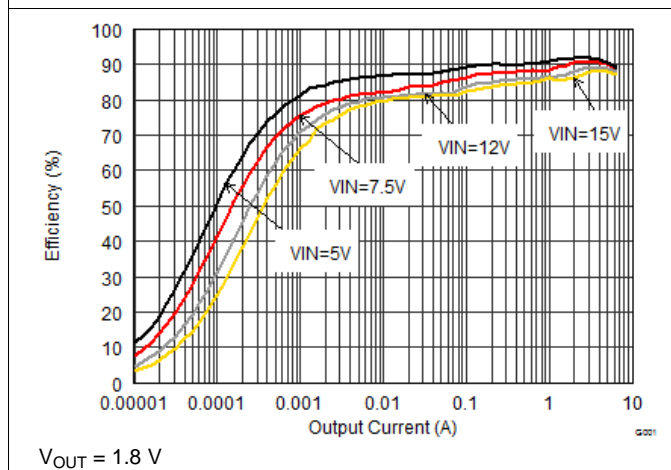
Figure 15. Efficiency vs Load Current

V_{OUT} = 1.8 V
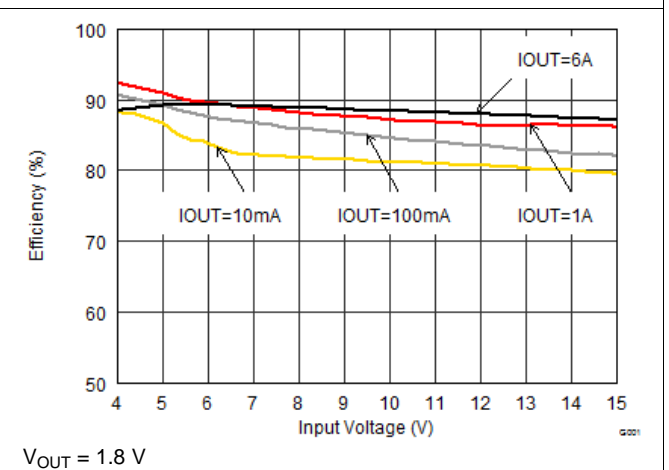
Figure 16. Efficiency vs Input Voltage

V_{OUT} = 0.9 V
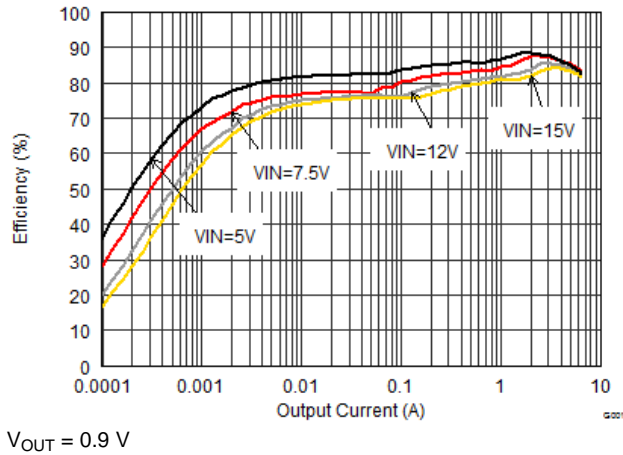
Figure 17. Efficiency vs Load Current

V_{OUT} = 0.9 V
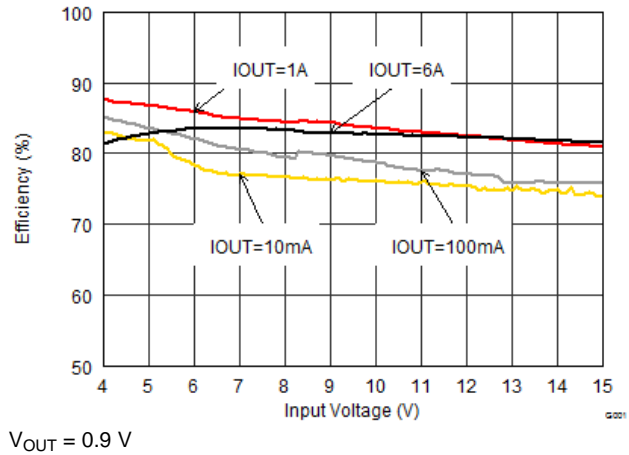
Figure 18. Efficiency vs Input Voltage
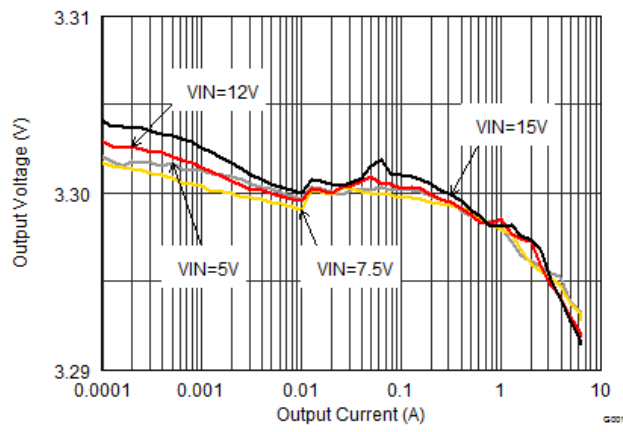
Figure 19. Output Voltage vs Output Current (Load regulation)
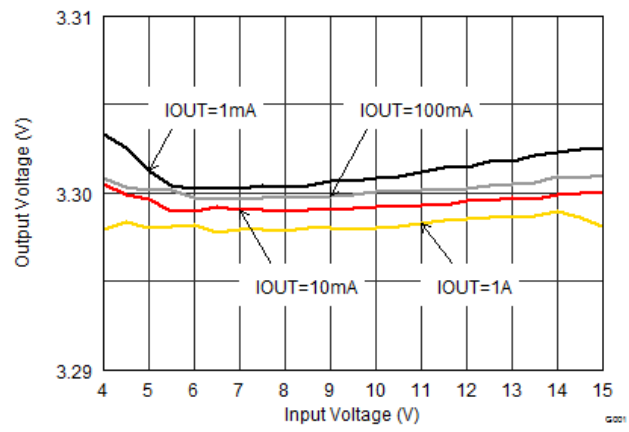
Figure 20. Output Voltage vs Input Voltage (Line regulation)
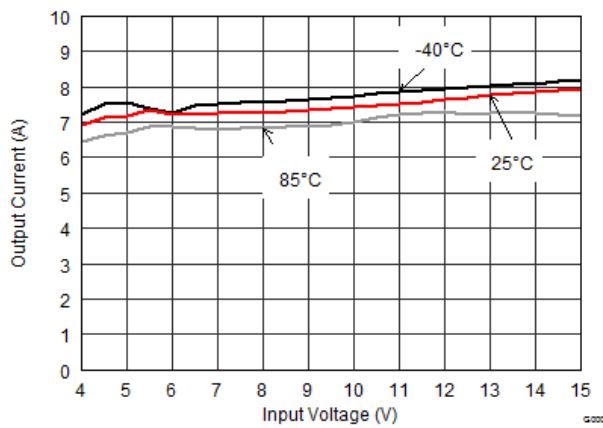
Figure 21. Maximum Output Current vs Input Voltage
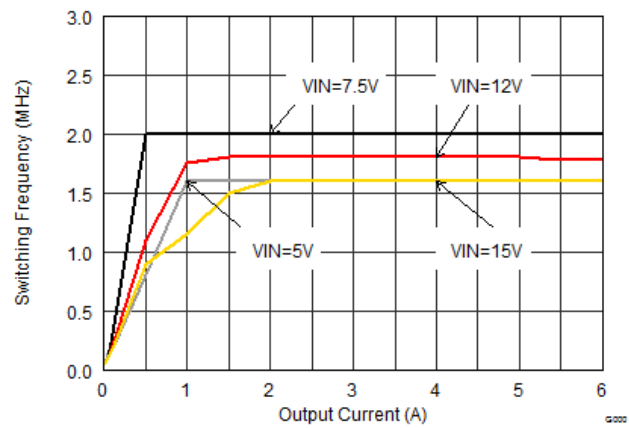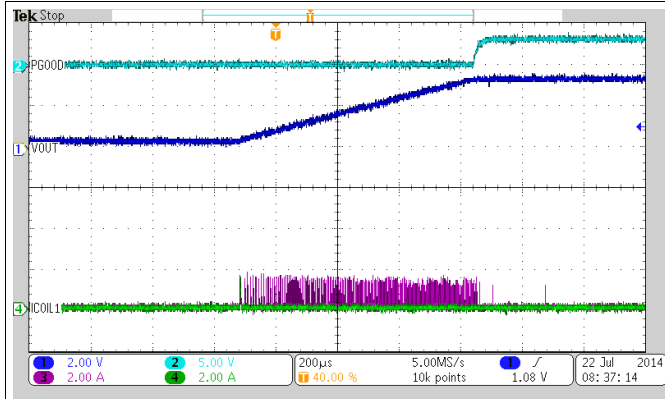
Figure 22. Switching Frequency vs Output Current

Product Folder Links: *TPS62180 TPS62182*

Figure 23. Startup into 33 Ω (100 mA)
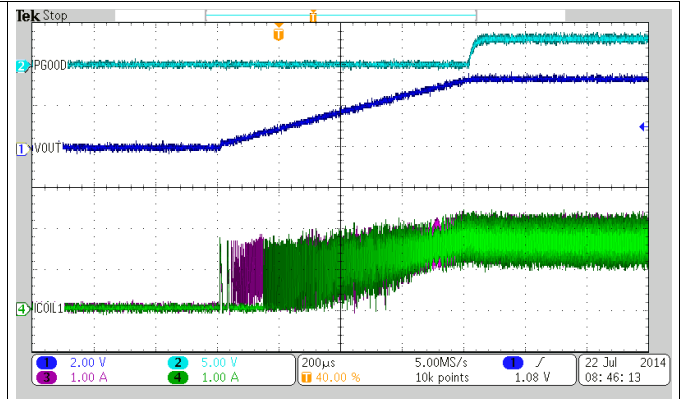
Figure 24. Startup into 1 Ω (3.3 A)
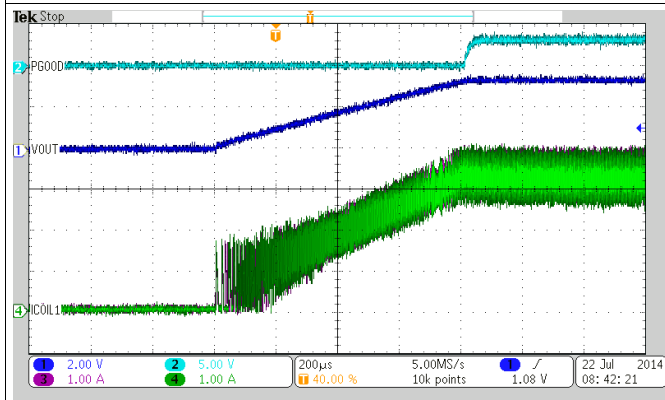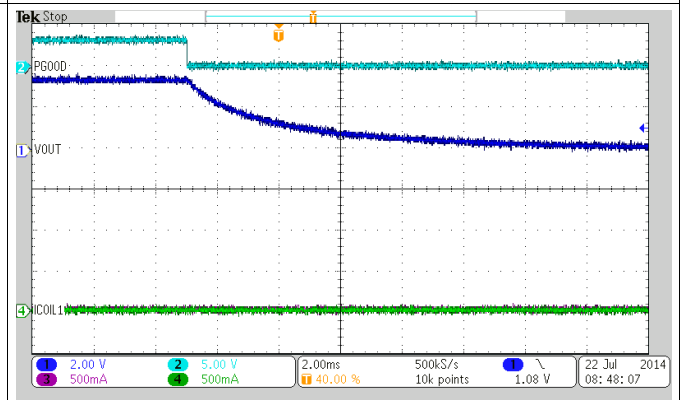
Figure 25. Startup into 0.5 Ω (6.6 A)
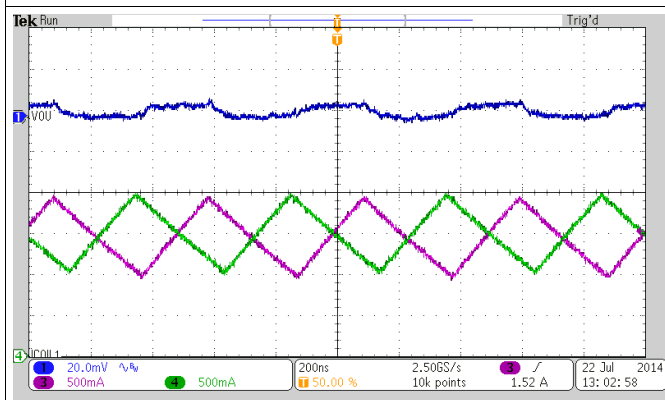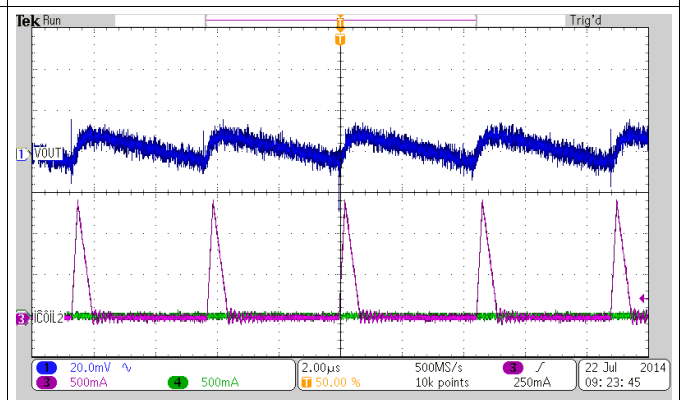
Figure 26. Output Discharge (No load)

I_{OUT} = 3 A

Figure 27. Typical Operation (PWM)

I_{OUT} = 100 mA

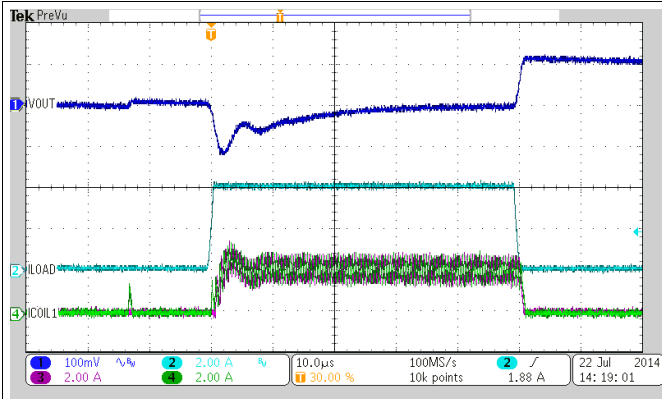**Figure 28. Typical Operation (PSM)**

Product Folder Links: *TPS62180 TPS62182*

Figure 29. Load Transient Response (PSM-PWM)

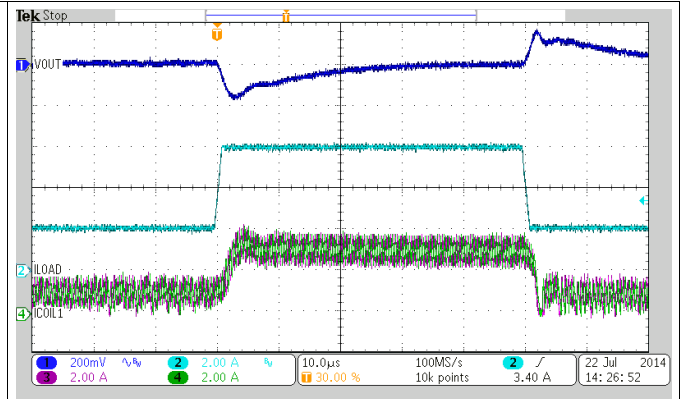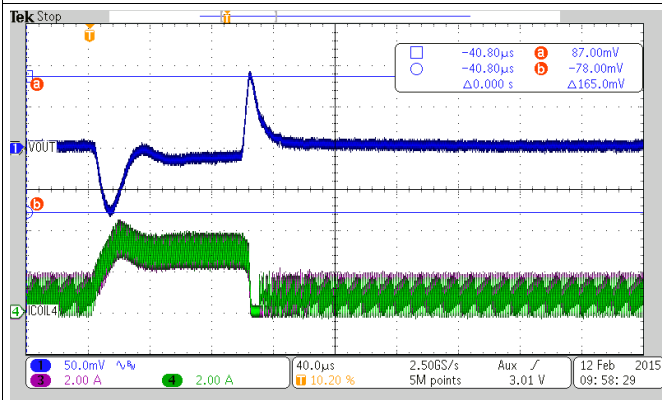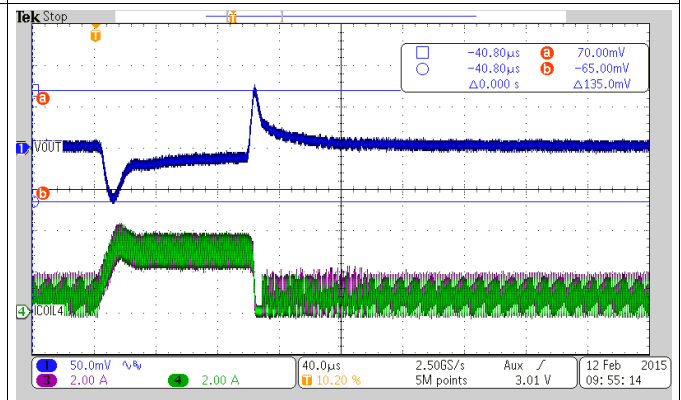**Figure 30. Load Transient Response (PWM-PWM)**

V_{OUT} = 1.8 V C_{OUT} = 6x47 µF

Figure 31. Transient Response to a load step of 1-6A (1A/µs)

V_{OUT} = 1.8 V C_{OUT} = 6x47 µF   additional C_{FF} = 82 pF

Figure 32. Transient Response to a load step of 1-6A (1A/µs)
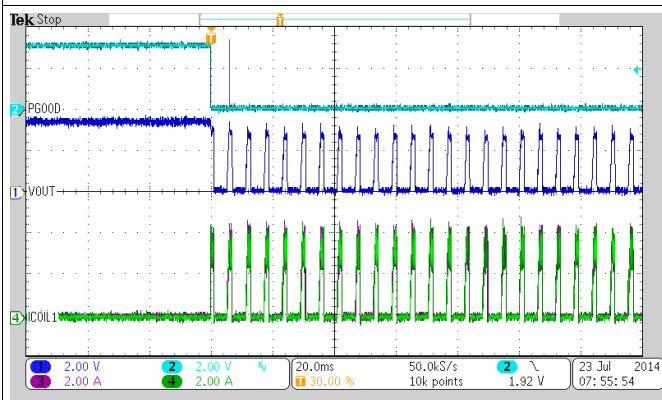
R_{LOAD} = 0.33 Ω

Figure 33. HICCUP at Overload Condition

R_{LOAD} = 0.33 Ω

Figure 34. HICCUP at Overload Condition

Product Folder Links: *TPS62180 TPS62182*
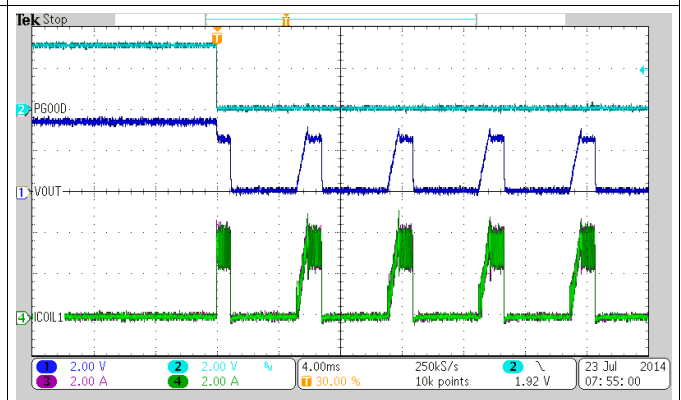
Figure 35. HICCUP at Short Circuit

Figure 36. HICCUP at Short Circuit

Figure 37. Maximum Ambient Temperature

9.2.2 TPS62180 Low Profile Solution

This design example is based on Figure 10 again, providing a very small (see Figure 38) and low profile solution, using low profile inductors.

9.2.2.1 Design Requirements

The input parameters used for this design are given in Table 7 and give a total solution size of about 72mm^2, using inductors with a maximum height of 1.2 mm:
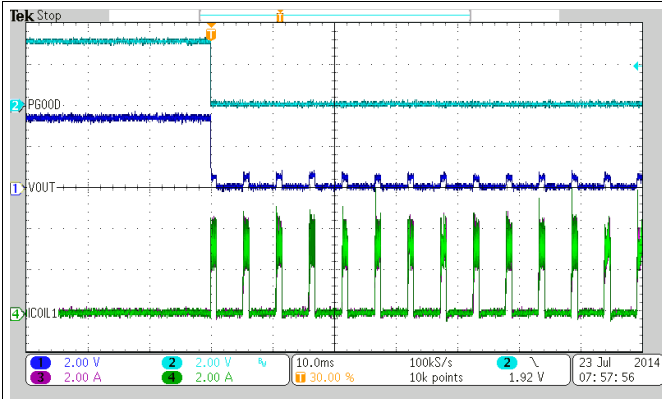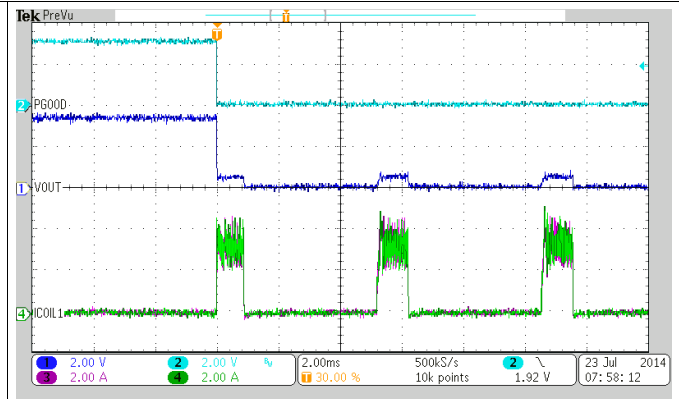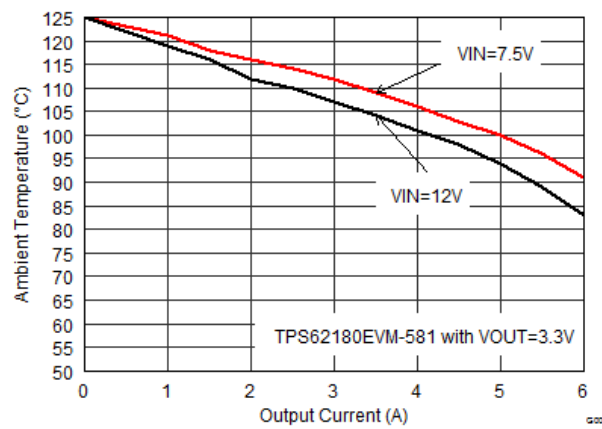
Table 7. Components Used for Application Characteristics

REFERENCE NAME	DESCRIPTION / VALUE	MANUFACTURER
TPS62180YZF	2 phase step down converter, 2 x 3 mm WCSP	Texas Instruments
L1, L2	Inductor DFE252012P, 1 μH ±20%, 2.5 x 2 x 1.2 mm	Toko
C_{IN}	Ceramic capacitor GRM21BR61E226ME44, 2 x 22 μF, 25 V, X5R, 0805	muRata
C_{OUT}	Ceramic capacitor GRM21BR60J476ME15, 2 x 47 μF, 6.3 V, X5R, 0805	muRata
C_{SS}	Ceramic capacitor, 10 nF	Standard
R1	Chip resistor, value depending on V_{OUT}	Standard
R2	Chip resistor, value depending on V_{OUT}	Standard
R3	Chip resistor, 470 kΩ, 0603, 1/16 W, 1%	Standard

9.2.2.2 Detailed Design Procedure

As opposed to the previous example, the solution size, including height, is limited and the soft start time is longer. This is achieved by using smaller inductors, as well as using a different soft start capacitor.

9.2.2.2.1 Inductor

Using Table 5, the 1-μH DFE252012P is chosen with dimensions of 2.5 x 2.0 x 1.2 mm. The larger DCR of 42 mΩ maximum causes some efficiency drop (see comparison below).
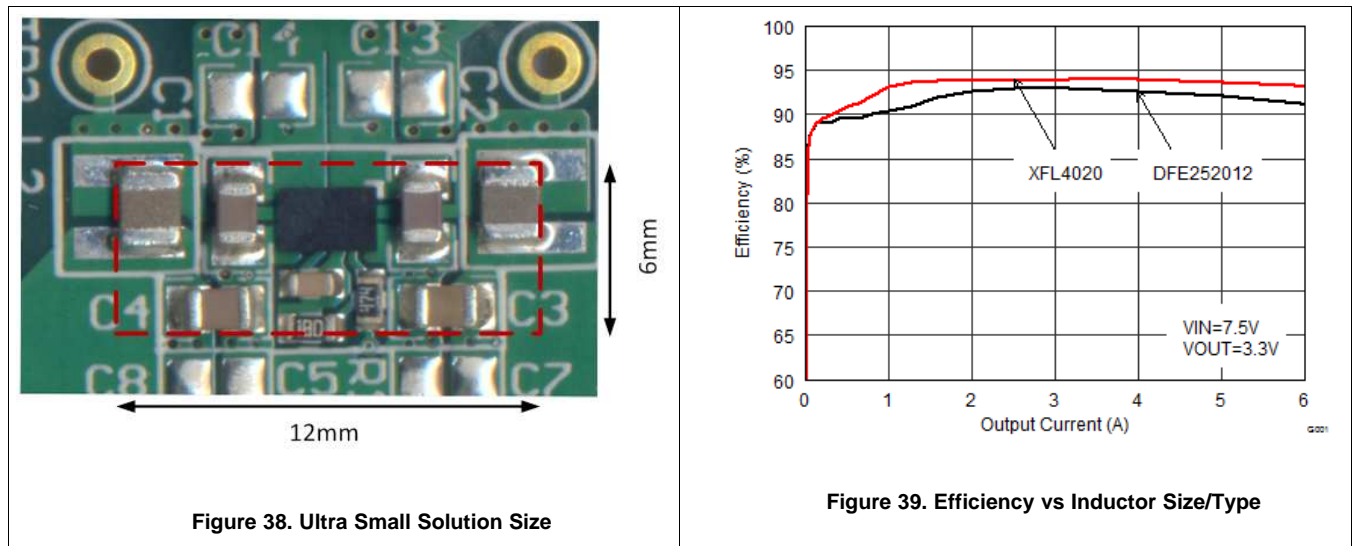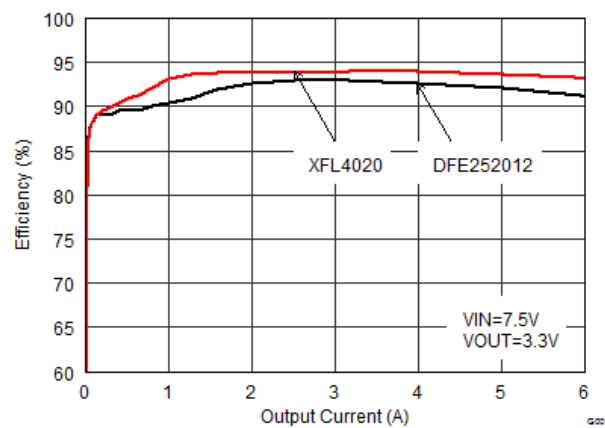

Figure 38. Ultra Small Solution Size

Figure 39. Efficiency vs Inductor Size/Type

Product Folder Links: *TPS62180 TPS62182*

9.2.2.2.2 Input and Output Capacitors

Since electrical design parameters are unchanged, the same values as chosen in the previous example are used for these capacitors.

9.2.2.2.3 Soft Start Capacitor

Using Equation 14 again, and inserting t_{SS} = 2.5 ms gives a capacitance of 10 nF, which is chosen.

9.2.2.2.4 Using the Accurate EN Threshold

The TPS6218x provides a very accurate EN threshold voltage. This can be used to switch on the device according to a V_{IN} or another voltage level by using a resistive divider as shown below.
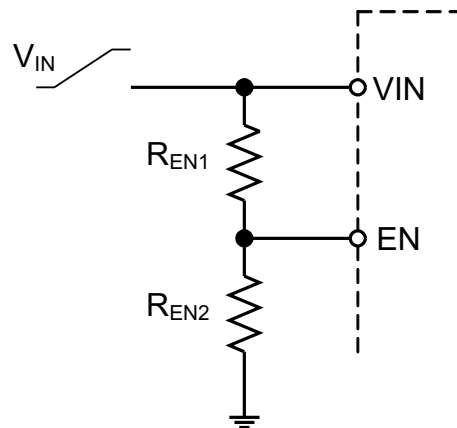
Figure 40. Resistive Divider for Controlled EN Threshold

The values of R_{EN1} and R_{EN2}, needed to set EN = High at a specific V_{IN} can be calculated according to Kirchhoff's laws, shown in Equation 15 and used in the following example:

$$V_{IN} = V_{EN\_threshold} \cdot \frac{R_{EN1} + R_{EN2}}{R_{EN2}}$$

(15)

For a typical 8-V input rail, the device turn on target value is set to 5.5 V. The current through the resistive divider is set to 10 µA, which indicates a total resistance of about 800 kΩ. Appropriate standard resistor values, fitting Equation 15, are R_{EN1} = 680 kΩ and R_{EN2} = 150 kΩ. As a result, the device switches on, when V_{IN} has reached 5.5 V and the current through the divider is 9.6 µA. The device switches off at a threshold of 0.9 V. Using Equation 15 again, this case gives a level of V_{IN} = 5.0 V.

Figure 47 to Figure 50 show thresholds and appropriate device behavior with a startup time of about 800 µs.

9.2.2.3 Application Performance Curves

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)
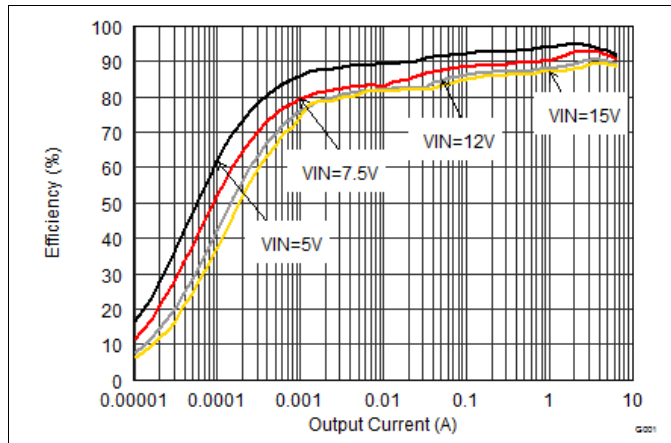
Figure 41. Efficiency vs Load Current
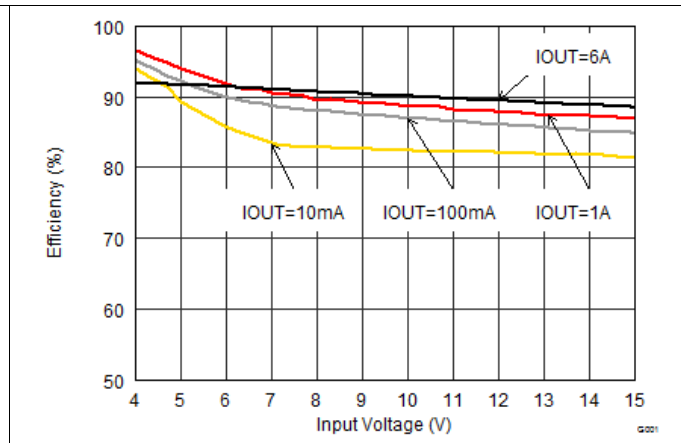
Figure 42. Efficiency vs Input Voltage
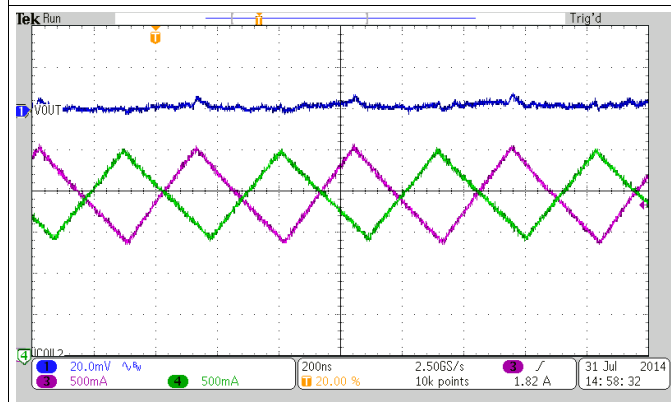
V_{IN} = 8 V, I_{OUT} = 4 A

Figure 43. Typical Operation (PWM)
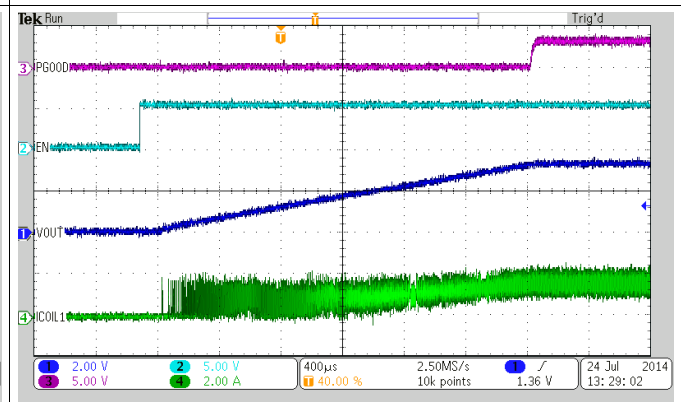
C_{SS} = 10 nF

Figure 44. Startup into 1 Ω (3.3 A)
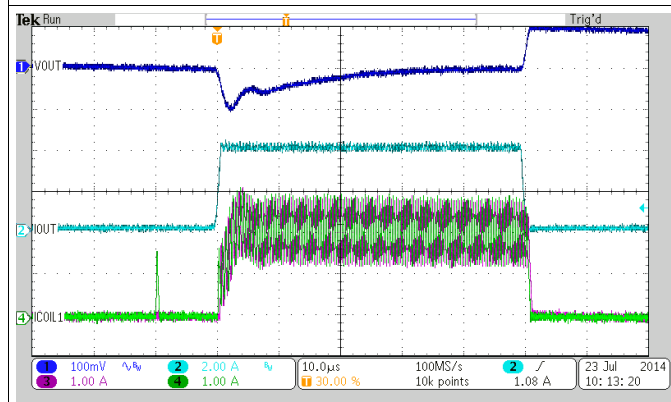
Figure 45. Load Transient Response (PSM-PWM)
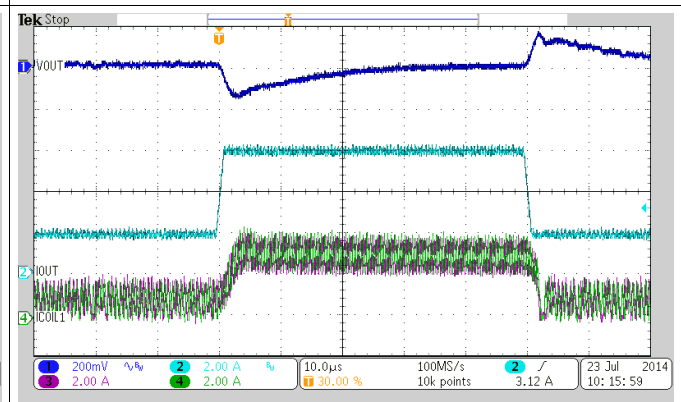
Figure 46. Load Transient Response (PWM-PWM)

Product Folder Links: *TPS62180 TPS62182*
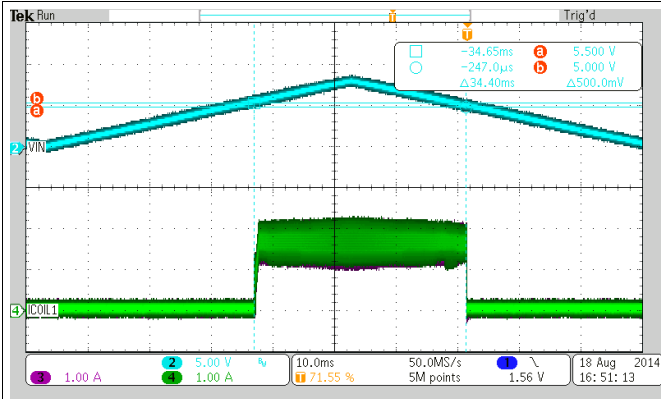
V_{IN} = 5.5 V (Rising), V_{IN} = 5.0 V (Falling)

Figure 47. Accurate EN Threshold
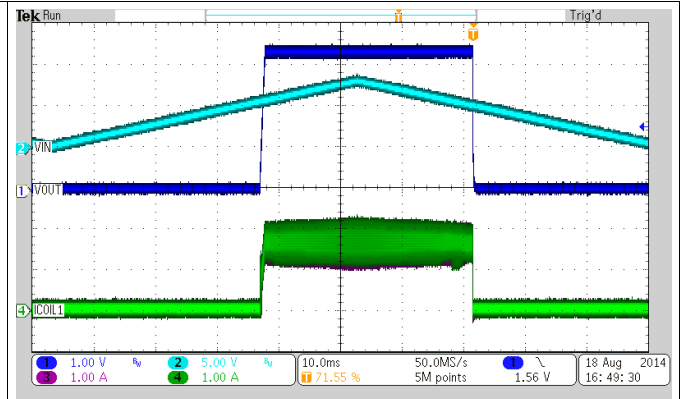
Figure 48. Accurate EN Threshold Showing V_{OUT}
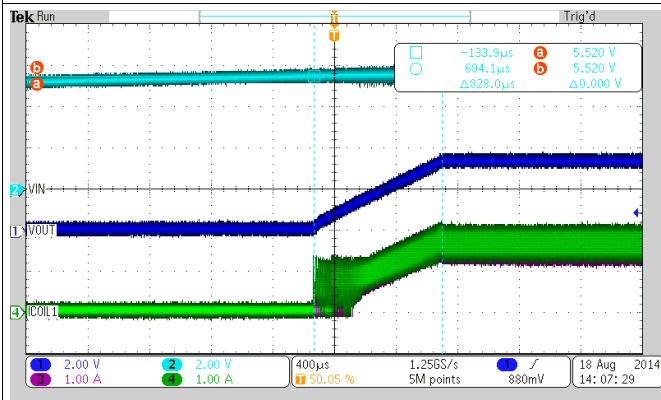
V_{IN} = 5.5 V (Rising)

Figure 49. Accurate EN Threshold
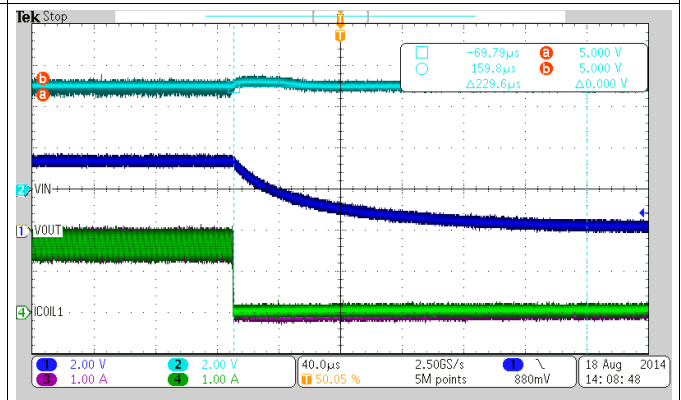
V_{IN} = 5.0 V (Falling)

Figure 50. Accurate EN Threshold

9.3 TPS62180 Output Voltage Application Examples

This section provides typical schematics for commonly used output voltage values.

9.3.1 Application Schematic Examples
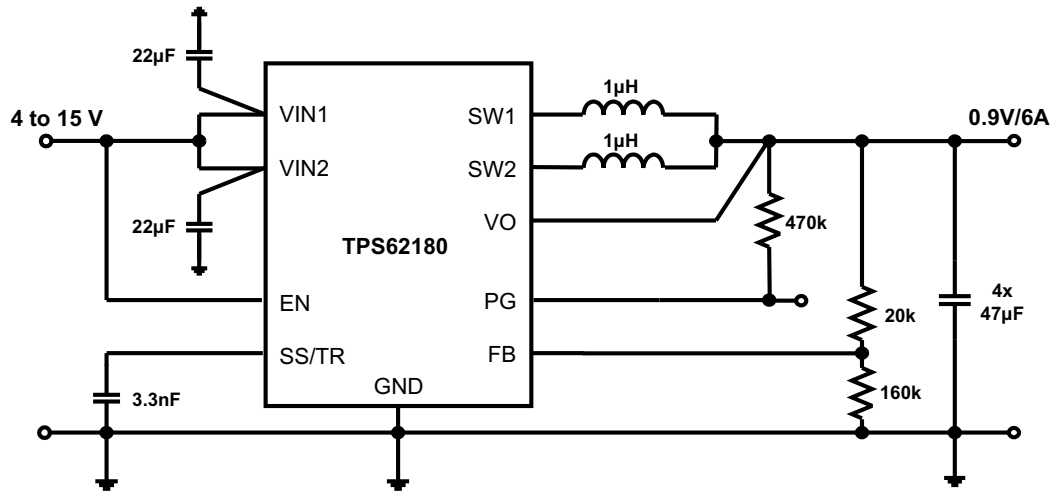
Copyright © 2017, Texas Instruments Incorporated

Figure 51. 0.9-V/6-A Power Supply
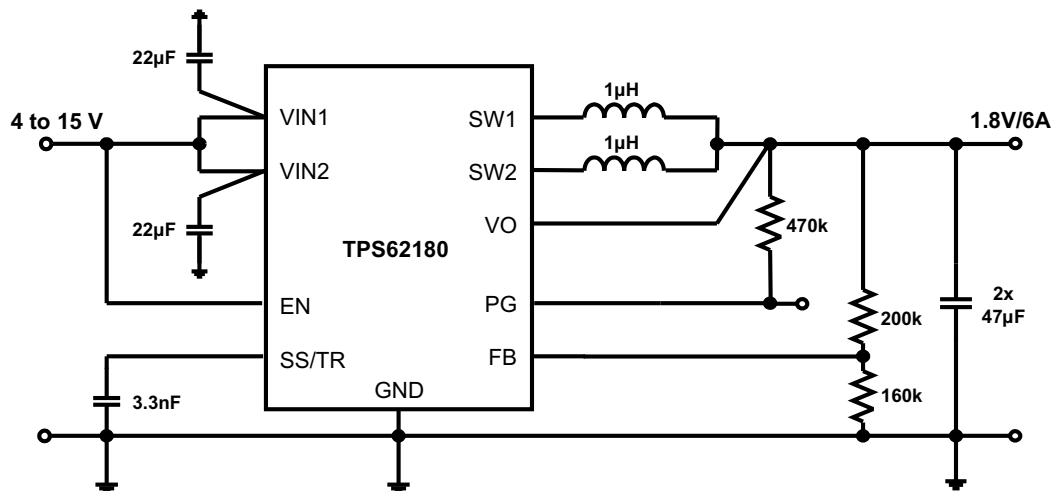
Copyright © 2017, Texas Instruments Incorporated

Figure 52. 1.8-V/6-A Power Supply

TPS62180 Output Voltage Application Examples (continued)
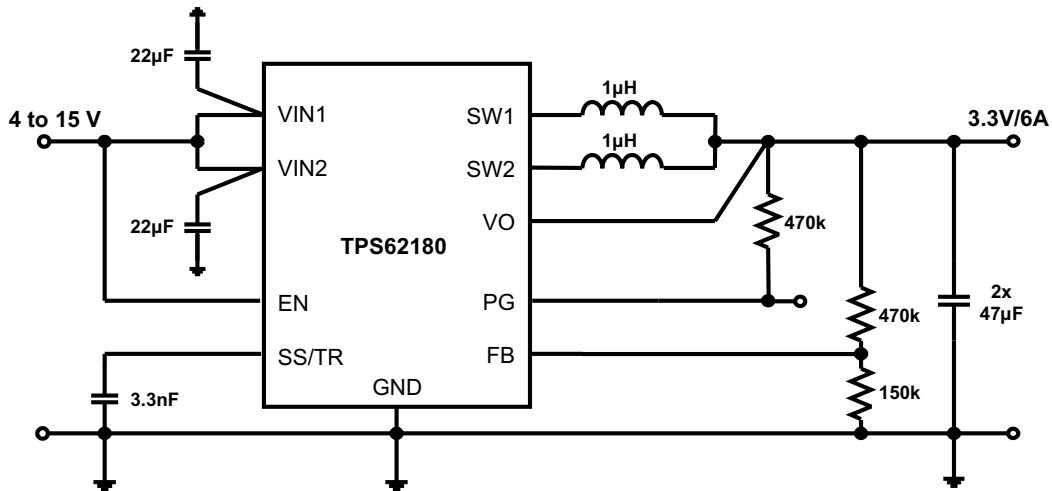
Copyright © 2017, Texas Instruments Incorporated

Figure 53. 3.3-V/6-A Power Supply
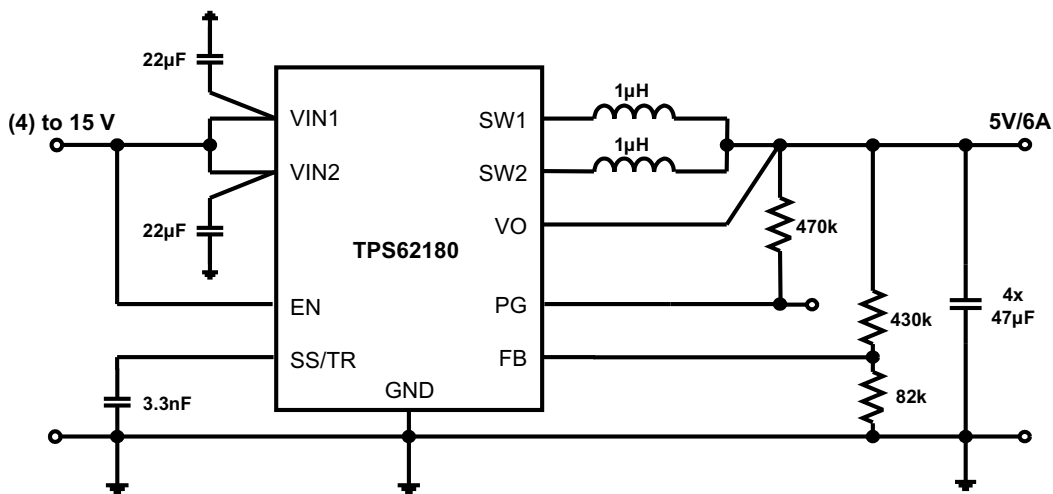
Copyright © 2017, Texas Instruments Incorporated

Figure 54. 5-V/6-A Power Supply

9.3.2 Design Requirements

Based on Figure 10, the schematics shown in Figure 51 through Figure 54 show different output voltage divider values to get different V_{OUT}. Another design target is to have about 5-µA current through the divider.

9.3.3 External Component Selection

The values for the voltage divider are derived using the procedure given in Programming the Output Voltage. While Equation 10 and Equation 11 are used to calculate R2 and R1, the values are aligned with standard resistor values.

10 Power Supply Recommendations

The TPS6218x are designed to operate from a 4-V to 15-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

The PCB layout of the TPS6218x demands careful attention to ensure proper operation, thermal profile, low noise emission and to achieve best performance. A poor layout can lead to issues like poor regulation, stability and accuracy weaknesses, increased EMI radiation and noise sensitivity. While the TPS6218x provides very high power density, the PCB layout also contributes significantly to the thermal performance.

11.1.1 PCB Layout

A recommended PCB layout for the TPS62180 dual phase solution is shown below. It ensures best electrical and optimized thermal performance considering the following important topics:

- The input capacitors must be placed as close as possible to the appropriate pins of the device. This provides low resistive and inductive paths for the high di/dt input current. The input capacitance is split, as is the V_{IN} connection, to avoid interference between the input lines.
- The SW node connection from the IC to the inductor conducts high currents. It should be kept short and can be designed in parallel with an internal or bottom layer plane, to provide low resistance and enhanced thermal behavior.
- The V_{OUT} regulation loop is closed with C_{OUT} and its ground connection. If a ground layer or plane is used, a direct connection by vias, as shown, is recommended. Otherwise the connection of C_{OUT} to GND must be short for good load regulation.
- The FB node is sensitive to dv/dt signals. Therefore the resistive divider should be placed close to the FB pin, avoiding long trace distance. Using the TPS62182 (fixed output voltage version), the FB pin can be left floating, but it is good practice and recommended to connect it to AGND for best thermal characteristics.

11.2 Layout Example
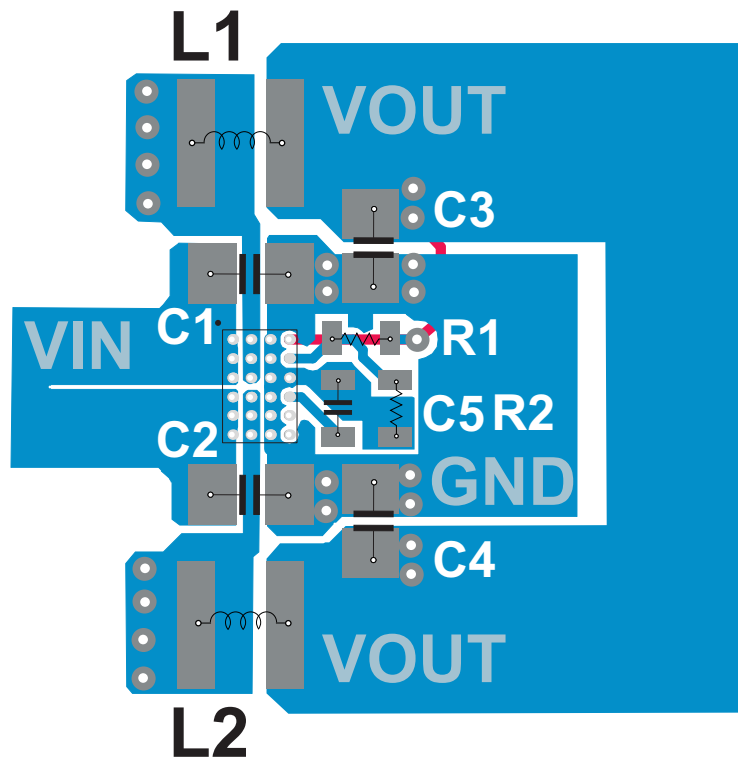
Figure 55. TPS62180 Board Layout

Product Folder Links: *TPS62180 TPS62182*

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62180	Click here	Click here	Click here	Click here	Click here
TPS62182	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

AEE, NanoFree are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62180YZFR	ACTIVE	DSBGA	YZF	24	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC180	Samples
TPS62180YZFT	ACTIVE	DSBGA	YZF	24	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC180	Samples
TPS62182YZFR	ACTIVE	DSBGA	YZF	24	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC182	Samples
TPS62182YZFT	ACTIVE	DSBGA	YZF	24	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ELC182	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62180YZFR	DSBGA	YZF	24	3000	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1
TPS62180YZFT	DSBGA	YZF	24	250	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1
TPS62182YZFR	DSBGA	YZF	24	3000	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1
TPS62182YZFT	DSBGA	YZF	24	250	330.0	12.4	2.25	3.25	0.81	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62180YZFR	DSBGA	YZF	24	3000	367.0	367.0	35.0
TPS62180YZFT	DSBGA	YZF	24	250	367.0	367.0	35.0
TPS62182YZFR	DSBGA	YZF	24	3000	367.0	367.0	35.0
TPS62182YZFT	DSBGA	YZF	24	250	367.0	367.0	35.0

YZF (R−XBGA−N24)   DIE−SIZE BALL GRID ARRAY

PIN A1
INDEX AREA

1,50

0,50

0,25

0,25

2,50

0,50

F
E
D
C
B
A

1   2   3   4

24X Ø $\frac{0,35}{0,25}$

$\oplus$ | Ø 0,015 Ⓜ | C | A | B

$\frac{0,35}{0,15}$

0,625 MAX

C

SEATING PLANE

$\bigtriangleup$ | 0,05 | C

D: Max = 3.13 mm, Min = 3.07 mm

E: Max = 2.13 mm, Min = 2.07 mm

4205058−6/P   07/13
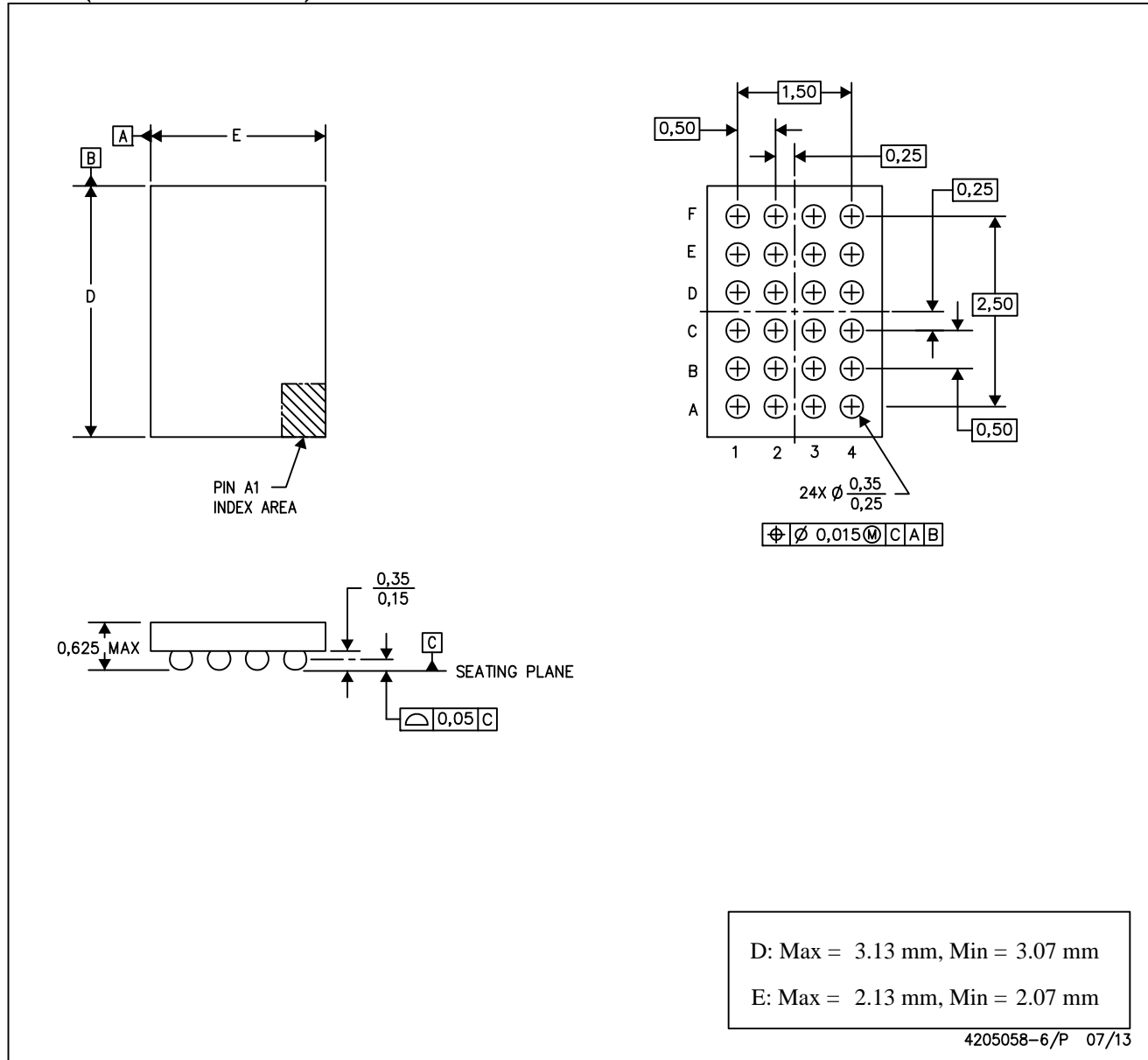
NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   NanoFree™ package configuration.

TEXAS INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.