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PS176 DisplayPort™-to-HDMI 2.0 Protocol Converter Datasheet

Version 0.6

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KEY FEATURES

- Compliant to DisplayPort™ Specification 1.2a for 1.62Gbps, 2.7Gbps and 5.4Gbps
- Supports DisplayPort™ 1, 2, and 4 lanes
- Supports full link training and no link training
- Supports multiple color formats:
  - DP: RGB 6/8/10/12-bit per component (bpc) and YCbCr4:4:4, YCbCr4:2:2 bpc 8/10/12 bpc
  - HDMI: RGB 8/10/12 bpc; YCbCr4:4:4, YCbCr4:2:2 and YCbCr4:2:0 8/10/12 bpc
- Compliant to HDMI Specification 2.0, data rate up to 6Gbps
- Supports TMDS scrambling for EMI/RFI reduction
- Supports SCDC (Status and Control Data Channel)
- Supports up to 8-channel LPCM, compressed audio (AC-3, DTS) and HBR audio formats
- Supports up to 192kHz audio frame rate and up to 24-bit audio sample size
- Content protection
  - Supports HDCP 1.4 repeater with on-chip keys
  - Supports HDCP 2.2 repeater
- On-chip microprocessor with embedded SPI ROM
- ESD:
- 1.2V Core Power Supply & 3.3V I/O Power Supply
- 0°C to 70°C Ambient Operating Temperature Range
- 48-pin 6x6mm QFN Halogen free RoHS package

APPLICATIONS

- Dongle Application

Typical Application

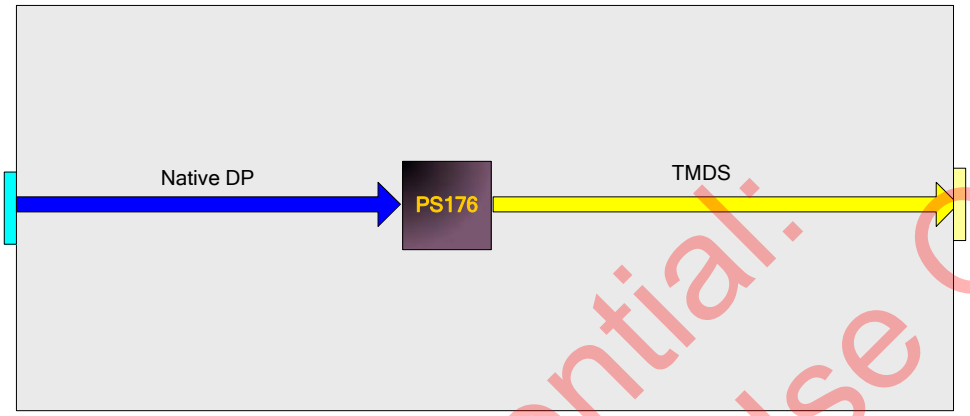


Figure1. Typical Application

DESCRIPTION

PS176 is a DisplayPort 1.2a to HDMI 2.0 Protocol Converter which receives both video and audio streams from DisplayPort link and converts to TMDS output. The TMDS transmitter is compliant to HDMI 2.0 specification with data rate up to 6Gbps.

PS176 supports HDCP 1.4 and HDCP 2.2 repeater for downstream sink with an embedded key.

PS176 has integrated an on-chip microcontroller for system configuration purposes. The device can be configured with an SPI Flash for customized applications.

The system level block diagram of PS176 is described in Figure 2. Detailed descriptions of each functional block are given in the following sections.

FUNCTIONAL BLOCK DIAGRAM

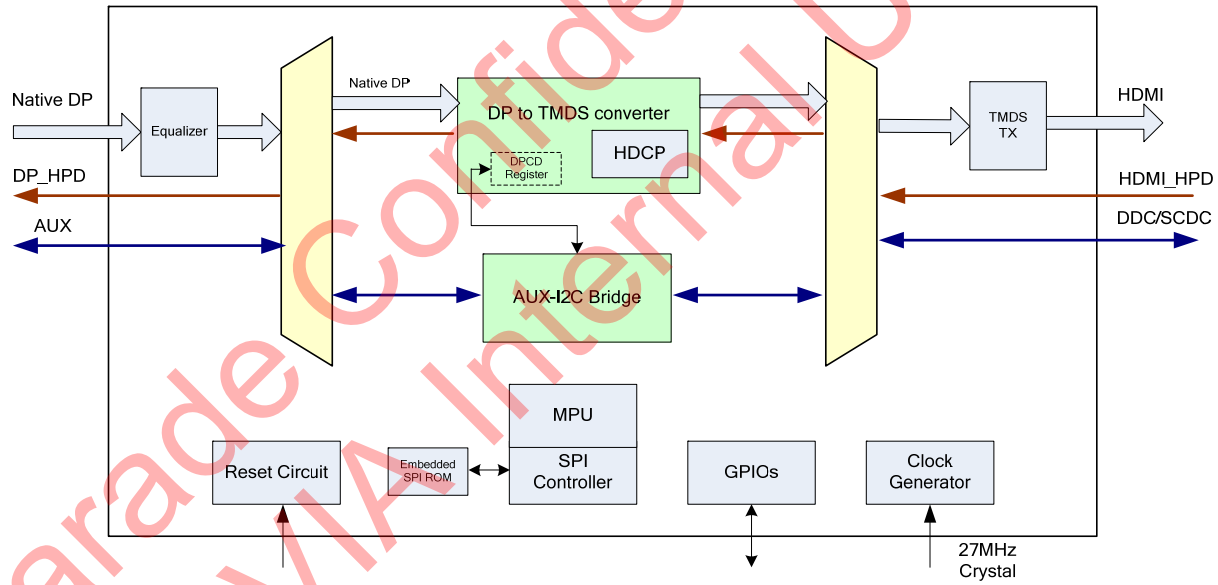


Figure2. PS176 Functional Block Diagram

DISPLAYPORT™ RECEIVER

The DisplayPort™ Receiver interface implemented in PS176 is fully compliant to the *VESA DisplayPort Standard, Version 1.2a.*

Physical Layer (PHY)

The DisplayPort™ main link operates at a data rate of 1.62Gbps (Reduced Bit Rate - RBR), 2.7Gbps (High Bit Rate - HBR) or 5.4Gbps (High Bit Rate 2 - HBR2). DisplayPort™ Receiver receives serial data stream, de-serializes it, and decodes it in ANSI 8B/10B format. Subsequently, the receiver unscrambles and de-skews the decoded data.

The DisplayPort™ AUX channel is a half-duplex, bi-directional channel which supports bit rate at 1 Mbps. The logical sub-block of AUX channel generates and detects Start/Stop condition and locks to Sync pattern, encodes or decodes of data using Manchester-II coding. The electrical sub-block of AUX channel consists of one differential pair which operates as a half-duplex bi-directional channel. The AUX channel provides Link Configuration, Link maintenance and EDID access.

The DisplayPort™ Hot Plug/Unplug detection is indicated by HPD signal. The HPD signal is asserted whenever the sink device is connected to its main power supply and the source (DP Tx) is detected. The pulsed HPD signal is also used as an Interrupt Request (IRQ) by sink device. The low-going pulse width within 0.5ms to 1.0ms is asserted as Interrupt Request (IRQ) from sink device to source device which shall read link status field of DisplayPort™ Configuration Data (DPCD) and take proper action.

Link Layer

The DisplayPort™ receiver Link Layer services reconstruct original video and audio data and timing base through isochronous transport services over main link. It also handles AUX Channel link service and device service. The main link supports 4-lane, 2-lane and 1-lane at 1.62Gbps, 2.7Gbps or 5.4Gbps data rate. The optimal lane count and data rate shall be negotiated through capability discovery and link training between source and sink devices. The isochronous transport services of Link Layer provide packing/unpacking, stuffing/un-stuffing, framing/un-framing, inter-lane skewing/de-skewing, stream clock recovery, insertion/extraction of Main Stream Attributes data and/or inserting/extracting of secondary-data packet with ECC (Error Control Code) for audio stream packet & CEA861-F InfoFrame packet.

PS176 DisplayPort™ receiver supports RGB444 (6/8/10/12-bit), YCbCr444 (8/10/12-bit) and YCbCr422 (8/10/12-bit) video input formats and supports up to 8 channels LPCM, compressed audio format (AC-3, DTS) and HBR audio format. It also supports audio frame rate of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz and audio sample size of 16, 20 and 24 bits per sample.

HDMI TRANSMITTER

The High Definition Multimedia Interface (HDMI) implemented in PS176 is fully compliant to the *High-Definition Multimedia Interface Specification, Version 2.0, September 4, 2013.*

Compliance includes the capability to deliver audio and video content from the decoded DisplayPort™ audio and video streams onto an HDMI TMDS output. The HDMI TMDS provides support for up to 6.0Gbps data rate, allowing display up to 4kx2k at 60Hz refresh rate with 8-bit deep color and 3D video formats up to 1080p at 120Hz. Audio output support consists of up to 8 channels of LPCM at 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz sample rate and audio sample size of 16, 20 and 24-bits per sample, decoded by DisplayPort™ receiver. The PS176 also supports compressed audio formats (AC-3, DTS) and HBR audio format.

PS176 provides support for a SCDC channel for EDID reading and exchange of point-to-point dynamic data between the Source and the Sink. PS176 also supports a monitor hot plug detect signal HPD to detect the attachment and presence of a sink device.

HDCP

The HDCP provides a secure audio and video content on DisplayPort™ receiver and TMDS transmitter interfaces, it also provides appropriate security measures to prevent discovery and nullification of the HDCP keys stored within the PS176. PS176 supports both HDCP version 1.4 specification and HDCP version 2.2 specification. The features of HDCP are summarized as below:

- The DisplayPort™ receiver side performs upstream HDCP 1.4/2.2 function including HDCP authentication and HDCP decryption.
- The TMDS transmitter side performs downstream HDCP 1.4/2.2 function including HDCP authentication and HDCP encryption.
- Software will interface with both upstream and downstream HDCP authentication engine to implement the HDCP repeater functions.
- Integrated both HDCP receiver and transmitter Key ROMs

HOT PLUG DETECTION (HPD)

PS176 has two hot plug detection signals.

- HDMI_HPD: downstream port hot plug detection input
- DP_HPD: upstream port hot plug detection output

HDMI_HPD

HDMI_HPD is an input signal. A HIGH on this signal indicates that a sink is connected. It is the hardware that is responsible for detecting the state change on this pin. Firmware will interpret the signal and take

actions after the HDMI_HPD state change. HDMI_HPD state changes are mainly used in the PS176 operation and power state machine maintained by PS176 firmware.

DP_HPD

DP_HPD is an output signal. A HIGH on this signal indicates that PS176 is ready to take DisplayPort™ input. Firmware will control this signal according to PS176 operation and power state machine.

After power on, DP_HPD signal will stay at low. Once PS176 is ready to take DisplayPort™ input, this signal will be asserted HIGH.

In addition to hot plug detection, DP_HPD signal is also used for the following:

- DisplayPort™ IRQ, including Link Status change, AUTOMATED_TEST_REQUEST and CP_IRQ. In these events, hardware will generate short low-going pulse (0.5ms ~ 1ms) on DP_HPD pin
- DisplayPort™ MCCS_IRQ and SINK_SPECIFIC_IRQ. Firmware will generate short low-going pulse (0.5ms ~ 1ms) in the two events

AUX TO I2C BRIDGE

AUX to I2C bridge acts as a bidirectional repeater function from DisplayPort™ AUX CH interface to HDMI DDC interface. It monitors DisplayPort™ AUX CH traffic and converts only those I2C-over-AUX CH transactions targeted to the HDMI sink device, as described below, into HDMI DDC interface.

- EDID access: I2C slave address of 60h, 61h, A0h and A1h
- MCCS communication: I2C slave address of 6Eh and 6Fh
- VESA DisplayID standard (proposed and legacy): I2C slave address of A0h through A7h

All other I2C-over-AUX transactions are blocked and assumed to be accessing functions within the PS176.

The AUX to I2C bridge provides an interface for PS176 firmware to interface AUX CH directly. This is to provide hardware support for firmware to handle all possible native AUX transactions and I2C-over-AUX transactions, including those targeted to the HDMI sink device.

The AUX to I2C bridge also provides an interface for PS176 to directly access HDMI DDC port. This function will be used when firmware needs to read EDID from downstream device, or to read downstream HDCP port directly.

ON-CHIP MICROPROCESSOR (MPU)

PS176 integrates a micro-processor unit (MPU). The MPU core is an 8-bit processor which executes 8031/8051 type instructions. The instructions are stored in an internal flash ROM with Serial Peripheral Interface (SPI) and can be accessed through the internal ROM bus. 512 bytes internal RAM and 128 bytes SFR (special function register) provide the temporal data storage space. The MPU accesses the internal registers through a memory bus.

There is total 512K bytes SPI ROM space available for the MPU in PS176. PS176 firmware is stored in this ROM. There are two ways to update the SPI ROM. One is through PS176 control I2C port and another one is through AUX CH.

EDID

EDID Relay: EDID can be relayed from DDC bus in HDMI transmitter interface to AUX/DDC channel of upstream Dual-Mode DP source. When relaying the EDID from HDMI to upstream DP source, PS176 does not do any modifications.

GENERIC I/O INTERFACES

There are 4 dedicated General Purpose Input/Output pin (GPIO) in PS176.

CONTROL I2C SLAVE

Control I2C slave is the programming interface for external device to access internal registers, including DPCD registers. This bus is used to configure, control or debug PS176 internal functions.

DISPLAY RESOLUTIONS FOR TMDS OUTPUT

Following tables provide the popular video modes that PS176 may support. PS176 will also support other video modes as long as they are within available DisplayPort™ bandwidth, TMDS clock frequency range of 25MHz to 340MHz (HDMI Specification 1.4b) and TMDS character rate (1/4 of TMDS clock frequency) range of 85MHz to 150MHz (HDMI Specification 2.0).

Table 1. Video clock table for monitors

Resolution	Refresh Rate	Horizontal Frequency	Pixel Frequency	Standard Type	Original Document	Date
640 x 350	85 Hz	37.9 kHz	31.500 MHz	VESA Standard	VDMTPROP	3/1/96
640 x 400	85 Hz	37.9 kHz	31.500 MHz	VESA Standard	VDMTPROP	3/1/96
720 x 400	85 Hz	37.9 kHz	35.500 MHz	VESA Standard	VDMTPROP	3/1/96
640 x 480	60 Hz	31.5 kHz	25.175 MHz	Industry Standard	n/a	n/a
	72 Hz	37.9 kHz	31.500 MHz	VESA Standard	VS901101	12/2/92
	75 Hz	37.5 kHz	31.500 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	43.3 kHz	36.000 MHz	VESA Standard	VDMTPROP	3/1/96
800 x 600	56 Hz	35.1 kHz	36.000 MHz	VESA Guidelines	VG900601	8/6/90
	60 Hz	37.9 kHz	40.000 MHz	VESA Guidelines	VG900602	8/6/90
	72 Hz	48.1 kHz	50.000 MHz	VESA Standard	VS900603A	8/6/90
	75 Hz	46.9 kHz	49.500 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	53.7 kHz	56.250 MHz	VESA Standard	VDMTPROP	3/1/96
848 x 480	60 Hz	31.0 kHz	33.750 MHz	VESA Standard	AddDMT	3/4/03
1024 x 768	43 Hz Interlaced	35.5 kHz	44.900 MHz	Industry Standard	n/a	n/a
	60 Hz	48.4 kHz	65.000 MHz	VESA Guidelines	VG901101A	9/10/91
	70 Hz	56.5 kHz	75.000 MHz	VESA Standard	VS910801-2	8/9/91
	75 Hz	60.0 kHz	78.750 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	68.7 kHz	94.500 MHz	VESA Standard	VDMTPROP	3/1/96
1152 x 864	75 Hz	67.5 kHz	108.000 MHz	VESA Standard	VDMTPROP	3/1/96
1280 x 768	60 Hz	47.4 kHz	68.250 MHz	CVT Red. Blanking	AddDMT	3/4/03
	60 Hz	47.8 kHz	79.500 MHz	CVT	AddDMT	3/4/03
	75 Hz	60.3 kHz	102.250 MHz	CVT	AddDMT	3/4/03
	85 Hz	68.6 kHz	117.500 MHz	CVT	AddDMT	3/4/03
1280 x 960	60 Hz	60.0 kHz	108.000 MHz	VESA Standard	VDMTPROP	3/1/96
	85 Hz	85.9 kHz	148.500 MHz	VESA Standard	VDMTPROP	3/1/96
1280 x 1024	60 Hz	64.0 kHz	108.000 MHz	VESA Standard	VDMTREV	12/18/96
	75 Hz	80.0 kHz	135.000 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	91.1 kHz	157.500 MHz	VESA Standard	VDMTPROP	3/1/96
1360 x 768	60 Hz	47.7 kHz	85.500 MHz	VESA Standard	AddDMT	3/4/03
1400 x 1050	60 Hz	64.7 kHz	101.000 MHz	CVT Red. Blanking	AddDMT	5/13/03
	60 Hz	65.3 kHz	121.750 MHz	CVT	AddDMT	3/4/03
	75 Hz	82.3 kHz	156.000 MHz	CVT	AddDMT	3/4/03
	85 Hz	85.0 kHz	179.500 MHz	CVT	AddDMT	3/4/03
1440 x 900	60 Hz	55.5 kHz	88.750 MHz	CVT Red. Blanking	CVT 1.30MA	7/14/04
	60 Hz	59.9 kHz	106.500 MHz	CVT	CVT 1.30MA	7/14/04
	75 Hz	75.0 kHz	136.750 MHz	CVT	CVT 1.30MA	7/14/04

	85 Hz	84.8 kHz	157.000 MHz	CVT	CVT 1.30MA	7/14/04
1600 x 1200	60 Hz	75.0 kHz	162.000 MHz	VESA Standard	VDMTREV	12/18/96
	65 Hz	81.3 kHz	175.500 MHz	VESA Standard	VDMTREV	12/18/96
	70 Hz	87.5 kHz	189.000 MHz	VESA Standard	VDMTREV	12/18/96
	75 Hz	93.8 kHz	202.500 MHz	VESA Standard	VDMTREV	12/18/96
	85 Hz	106.3 kHz	229.500 MHz	VESA Standard	VDMTREV	12/18/96
1680 x 1050	60 Hz	64.7 kHz	119.000 MHz	CVT Red. Blanking	CVT 1.76MA	7/14/04
	60 Hz	65.3 kHz	146.250 MHz	CVT	CVT 1.76MA	7/14/04
	75 Hz	74.9 kHz	187.000 MHz	CVT	CVT 1.76MA	7/14/04
	85 Hz	93.9 kHz	214.75 MHz	CVT	CVT 1.76MA	7/14/04
1792 x 1344	60 Hz	83.64 kHz	204.750 MHz	VESA Standard	VDMTREV	9/17/98
1856 x 1392	60 Hz	86.33 kHz	218.250 MHz	VESA Standard	VDMTREV	9/17/98
1920 x 1200	60 Hz	74.0 kHz	154.000 MHz	CVT Red. Blanking	AddDMT	3/4/03
	60 Hz	74.6 kHz	193.250 MHz	CVT	AddDMT	3/4/03
	75 Hz	94.0 kHz	245.250 MHz	CVT	AddDMT	3/4/03
1920 x 1440	60 Hz	90.000 kHz	234.000 MHz	VESA Standard	VDMTREV	9/17/98

Table 2. Video clock table for TV devices

Field Rate	VIC	Hactive	Vactive	I / P	Htotal	Hblank	Vtotal	Vblank	H Freq (kHz)	V Freq (Hz)	Pixel Freq (MHz)
Low	60,65	1280	720	Prog	3300	2020	750	30	18.000	24.000	59.400
	61,66	1280	720	Prog	3960	2680	750	30	18.750	25.000	74.250
	62,67	1280	720	Prog	3300	2020	750	30	22.500	30.000	74.250
	32,72	1920	1080	Prog	2750	830	1125	45	27.000	24.000	74.250
	33,73	1920	1080	Prog	2640	720	1125	45	28.125	25.000	74.250
	34,74	1920	1080	Prog	2200	280	1125	45	33.750	30.000	74.250
	79	1680	720	Prog	3300	1620	750	30	18.000	24.000	59.400
	80	1680	720	Prog	3168	1488	750	30	18.750	25.000	59.400
	81	1680	720	Prog	2640	960	750	30	22.500	30.000	59.400
	86	2560	1080	Prog	3750	1190	1100	20	26.400	24.000	99.000
	87	2560	1080	Prog	3200	640	1125	45	28.125	25.000	90.000
	88	2560	1080	Prog	3520	960	1125	45	33.750	30.000	118.800
	93,103	3840	2160	Prog	5500	1660	2250	90	54.000	24.000	297.000
	94,104	3840	2160	Prog	5280	1440	2250	90	56.250	25.000	297.000
	95,105	3840	2160	Prog	4400	560	2250	90	67.500	30.000	297.000
	98	4096	2160	Prog	5500	1404	2250	90	54.000	24.000	297.000
	99	4096	2160	Prog	5280	1184	2250	90	56.250	25.000	297.000
	100	4096	2160	Prog	4400	304	2250	90	67.500	30.000	297.000
50Hz	17,18	720	576	Prog	864	144	625	49	31.250	50.000	27.000
	19,68	1280	720	Prog	1980	700	750	30	37.500	50.000	74.250
	20	1920	1080	Int	2640	720	1125	22.51	28.125	50.000	74.250
	21,22	1440	576	Int	1728	288	625	24.51	15.625	50.000	27.000
	23,24	1440	288	Prog	1728	288	312	24	15.625	50.080	27.000
	23,24	1440	288	Prog	1728	288	313	25	15.625	49.920	27.000
	23,24	1440	288	Prog	1728	288	314	26	15.625	49.761	27.000

	25,26	2880	576	Int	3456	576	625	24.51	15.625	50.000	54.000
	27,28	2880	288	Prog	3456	576	312	24	15.625	50.080	54.000
	27,28	2880	288	Prog	3456	576	313	25	15.625	49.920	54.000
	27,28	2880	288	Prog	3456	576	314	26	15.625	49.761	54.000
	29,30	1440	576	Prog	1728	288	625	49	31.250	50.000	54.000
	31,75	1920	1080	Prog	2640	720	1125	45	56.250	50.000	148.500
	37,38	2880	576	Prog	3456	576	625	49	31.250	50.000	108.000
	39	1920	1080	Int	2304	384	1250	85	31.250	50.000	72.000
	82	1680	720	Prog	2200	520	750	30	37.500	50.000	82.500
	89	2560	1080	Prog	3300	740	1125	45	56.250	50.000	185.625
	96,106	3840	2160	Prog	5280	1440	2250	90	112.500	50.000	594.000
	101	4096	2160	Prog	5280	1184	2250	90	112.500	50.000	594.000
60Hz	1	640	480	Prog	800	160	525	45	31.469	59.9403	25.175
	2,3	720	480	Prog	858	138	525	45	31.469	59.9403	27.000
	4,69	1280	720	Prog	1650	370	750	30	45.000	60.0003	74.250
	5	1920	1080	Int	2200	280	1125	22.51	33.750	60.0003	74.250
	6,7	1440	480	Int	1716	276	525	22.51	15.734	59.9403	27.000
	8,9	1440	240	Prog	1716	276	262	22	15.734	60.0543	27.000
	8,9	1440	240	Prog	1716	276	263	23	15.734	59.8263	27.000
	10,11	2880	480	Int	3432	552	525	22.51	15.734	59.9403	54.000
	12,13	2880	240	Prog	3432	552	262	22	15.734	60.0543	54.000
	12,13	2880	240	Prog	3432	552	263	23	15.734	59.8263	54.000
	14,15	1440	480	Prog	1716	276	525	45	31.469	59.9403	54.000
	16,76	1920	1080	Prog	2200	280	1125	45	67.500	60.0003	148.500
	35,36	2880	480	Prog	3432	552	525	45	31.469	59.9403	108.000
	83	1680	720	Prog	2200	520	750	30	45.000	60.0003	99.000
	90	2560	1080	Prog	3000	440	1100	20	66.000	60.0003	198.000
	97,107	3840	2160	Prog	4400	560	2250	90	135.000	60.0003	594.000
	102	4096	2160	Prog	4400	304	2250	90	135.000	60.0003	594.000

(CEC-861-F, March 2013)

Table 3. 4K x 2K video formats

HDMI_VIC	Description	Pixel Freq (MHz)	Hactive	Hblank	Vfreq (Hz)	Vactive	Vblank
0x01	4K x 2K 29.97, 30Hz	297.000 296.703	3840	560	30.000 29.970	2160	90
0x02	4K x 2K 25Hz	297.000	3840	1440	25.000	2160	90
0x03	4K x 2K 23.98, 24Hz	297.000 296.703	3840	1660	24.000 23.976	2160	90
0x04	4K x 2K 24Hz (SMPTE)	297.000	4096	1404	24.000	2160	90

(HDMI Specification Version 1.4b, October 11, 2011)

Table 4. DisplayPort to HDMI 3D video formats mapping and list

DisplayPort 3D Video Formats	HDMI 3D Video Formats
Stacked Frame	Framing packing
Frame Sequential	Framing packing
Pixel Interleaved (Line interleave only)	Line alternative
Side-by-Side (Full mode)	Side-by-Side (Full)

3D Structure	VIC	Description	Hactive	Hblank	Vactive	Vact_space	Vblank	Pixel freq (MHz)	V freq (Hz)
0000 Frame Packing	32	1080p, 23.98/24Hz	1920	830	1080	45	45	148.35/148.50	23.976/24.000
	4	720p, 59.94/60Hz	1280	370	720	30	30	148.35/148.50	59.940/60.000
	19	720p, 50Hz	1280	700	720	30	30	148.50	50.000
0010 Line alternative	16	1080p 60Hz	1920	280	1080	n.a.	45	297.00	60.000
	31	1080p 50Hz	1920	720	1080	n.a.	45	297.00	50.000
0011 Side-by-Side(Full)	16	1080p 60Hz	1920	280	1080	n.a.	45	297.00	60.000
	31	1080p 50Hz	1920	720	1080	n.a.	45	297.00	50.000

(HDMI Specification Version 1.4b, October 11, 2011)

Note: *All the supported 3D video formats in the mapping table can support all the timing data rates less than 3.0Gbps, the timing list table only shows some examples.*

POWER ON HARDWARE CONFIGURATION

The configuration mechanism is through configuration pin as shown in Table 5.

Table 5. Power On Configuration

Configuration Signal	Purpose	Definition
I2C_ADDR	Control I2C address selection	'0': 10h – 2Fh (default) '1': 90h – 9Fh, D0h – DFh

PIN ASSIGNMENT & DESCRIPTION

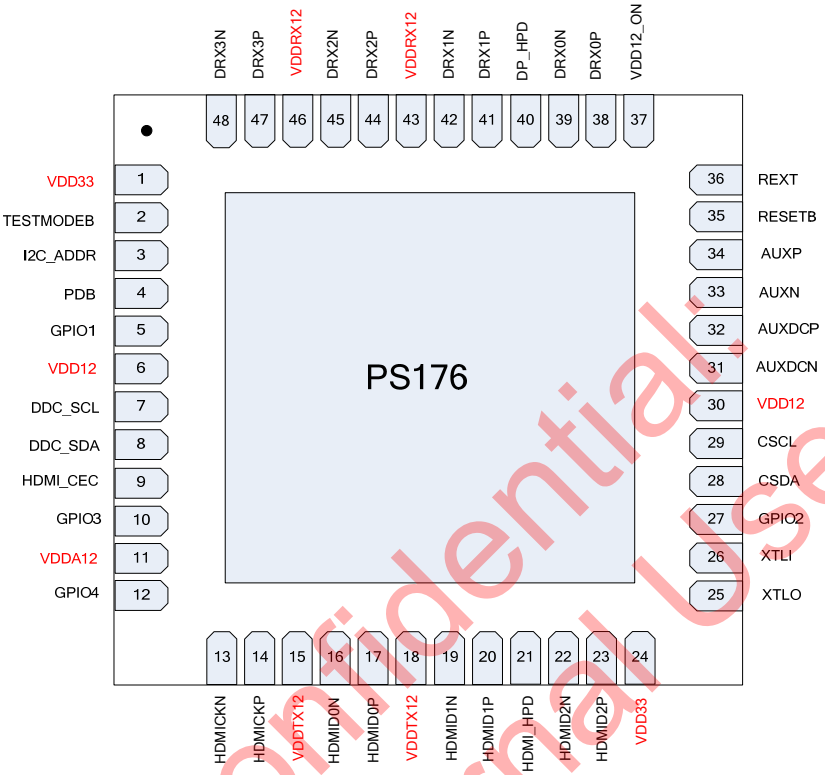


Figure3. PS176 PIN Assignment

Table 6. PS176 Pin Descriptions

Pin#	Pin Name	I/O Type	I/O Dir	Description
38	DRX0P	ANALOG	I	DP Main Link: DP_Lane0_p
39	DRX0N	ANALOG	I	DP Main Link: DP_Lane0_n
41	DRX1P	ANALOG	I	DP Main Link: DP_Lane1_p
42	DRX1N	ANALOG	I	DP Main Link: DP_Lane1_n
44	DRX2P	ANALOG	I	DP Main Link: DP_Lane2_p
45	DRX2N	ANALOG	I	DP Main Link: DP_Lane2_n
47	DRX3P	ANALOG	I	DP Main Link: DP_Lane3_p
48	DRX3N	ANALOG	I	DP Main Link: DP_Lane3_n
34	AUXP	ANALOG	I/O	DP AUX_p
33	AUXN	ANALOG	I/O	DP AUX_n
40	DP_HPD	ANALOG	O	DP RX Hot Plug Detect
14	HDMICKP	ANALOG	O	HDMI Tx clock channel positive
13	HDMICKN	ANALOG	O	HDMI Tx clock channel negative
17	HDMID0P	ANALOG	O	HDMI Tx data channel 0 positive
16	HDMID0N	ANALOG	O	HDMI Tx data channel 0 negative
20	HDMID1P	ANALOG	O	HDMI Tx data channel 1 positive
19	HDMID1N	ANALOG	O	HDMI Tx data channel 1 negative
23	HDMID2P	ANALOG	O	HDMI Tx data channel 2 positive
22	HDMID2N	ANALOG	O	HDMI Tx data channel 2 negative
7	DDC_SCL	Schmitt, OD	I/O	HDMI DDC CLK
8	DDC_SDA	Schmitt, OD	I/O	HDMI DDC DATA
21	HDMI_HPD	LVTTL	I	HDMI Hot Plug Detect
9	HDMI_CEC	ANALOG	I/O	HDMI CEC (Optional) Internal pull-up at 27kΩ
36	REXT	ANALOG	I	Connection to external resistor.
35	RESETB	Schmitt	I	Reset; ACTIVE LOW
4	PDB	Schmitt	I	Power down; ACTIVE LOW
2	TESTMODEB	Schmitt	I	Test mode control, NC for normal operation
37	VDD12_ON	DIG	O	Signal to active 1.2V power supply; Active High
29	CSCL	Schmitt, OD	I/O	Control I2C slave clock for debugging use
28	CSDA	Schmitt, OD	I/O	Control I2C slave data for debugging use
26	XTLI	ANALOG	I	Crystal oscillator clock input;
25	XTLO	ANALOG	O	Crystal oscillator clock output;
3	I2C_ADDR	LVTTL	I/O	I2C slave address selection Internal pull-down at ~80kΩ
5	GPIO1	LVTTL	I/O	General Purpose I/O Internal pull-up at ~80kΩ
27	GPIO2	LVTTL	I/O	General Purpose I/O Internal pull-up at ~80kΩ
10	GPIO3	LVTTL	I/O	General Purpose I/O Internal pull-up at ~80kΩ
12	GPIO4	LVTTL	I/O	General Purpose I/O Internal pull-down at ~80kΩ
31	AUXDCN	ANALOG	I	DP source detection
32	AUXDCP	ANALOG	I	DP source detection

1	VDD33	PWR		3.3V VDD Power Supply
24	VDD33	PWR		3.3V VDD Power Supply
43	VDDRX12	PWR		1.2V VDD for DP receiver
46	VDDRX12	PWR		1.2V VDD for DP receiver
11	VDDA12	PWR		1.2V VDD for analog
6	VDD12	PWR		1.2V VDD for digital logic
30	VDD12	PWR		1.2V VDD for digital logic
15	VDDTX12	PWR		1.2V VDD for HDMI transmitter
18	VDDTX12	PWR		1.2V VDD for HDMI transmitter
	EPAD			Ground

ABSOLUTE MAXIMUM RATINGS

Parameters	Comments	Min	Typ	Max	Unit
Supply Voltage Range:					
VDD33		-0.5		4	V
VDDRX12, VDDA12, VDD12, VDDTX12		-0.5		1.45	V
Normal I/O Voltage Range		-0.5		4	V
T_J	Junction temperature			125	°C
T_S	Storage temperature	-40		150	°C
ESD	Human Body Model				V
	Machine Model				V
	Charged Device Model				V

ESD Standard:

Human Body Mode: JESD22-A114-D

Machine Mode: JESD22-A115-A

Charged Device Mode: JESD22-C101-A

Latch-up Standard: JESD78; I-Test: +/- 200 mA; V-Test: 1.5X of Vcc

NORMAL OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Supply Voltage:				
VDD33	3.0	3.3	3.6	V
VDDRX12, VDDA12, VDD12, VDDTX12	1.14	1.2	1.26	V
Operation Temperature:				
Ta - Ambient Temperature	0		70	°C
Tc - Case Temperature	0		85	°C

POWER CONSUMPTIONS

Parameter	Conditions	Min	Typ	Max	Unit
DP input 4lane/5.4Gbps, HDMI output 5.94Gbps	Tested at				
1.2V Normal Supply Current, I_{DD}	VDD33 = 3.3V		432.2		mA
3.3V Normal Supply Current, I_{DD}	VDDRX12 = 1.2V		18.5		mA
Standby when DPCD600h = 02h	VDDA12 =1.2V				
1.2V Normal Supply Current, I_{DD}	VDD12=1.2V		16.8		mA
3.3V Normal Supply Current, I_{DD}	VDDTX12=1.2V		16		mA
Auto Power Down					
1.2V Normal Supply Current, I_{DD}			0		uA
3.3V Normal Supply Current, I_{DD}			70		uA
Power down when PDB pin is asserted					
1.2V Normal Supply Current, I_{DD}			0		uA
3.3V Normal Supply Current, I_{DD}			30		uA
DP input 4lane/5.4Gbps, HDMI output 5.94Gbps					
Power consumption			579.7		mW
Standby when DPCD600h = 02h					
Power consumption			73		mW
Auto Power Down					
Power consumption			0.23		mW
Power down when PDB pin is asserted					
Power consumption			0.1		mW

PACKAGE DISSIPATION RATINGS

48-pin QFN	Still air, 4-layer PCB
θ_{JA} - Junction to Ambient Thermal Resistance	28.5 C/W
θ_{JC} - Junction to Case Thermal Resistance	12.1 C/W
Maximum Power Dissipation Rating, Ta = 70 °C	1930 mW

I/O DC CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
I2C pins:					
CSCL/CSDA					
V_{OH} High-level output voltage	External 1.5 kΩ pull-up to		VDD33		V
V_{OL} Low-level output voltage	VDD33, I_{OL} = 8 mA			0.4	V
Control input pin: RESETB, PDB					
V_{IH} Input High-level voltage		0.7VDD33			V
V_{IL} Input Low-level voltage				0.25VDD33	V
Status I/O pins: GPIOx (x= 1~4)					
V_{OH} High-level output voltage		0.8VDD33			V
V_{OL} Low-level output voltage				0.15VDD33	V

I/O AC CHARACTERISTICS

Parameter	Test Conditions	Min	Typ[2]	Max	Unit
Supply ramp up time: (both supplies ramp at the same starting point)					
$t_{3.3}$ 3.3V supply ramp up time	10% to 90% of the 3.3V supply voltage			+10	ms
$t_{1.2}$ 1.2V supply ramp up time	10% to 90% of the 1.2V supply voltage			+10	ms
dt VDD33 and VDD12 power ramp up separation	Time difference between the mid points of VDD33 and VDD12	-10		+10	ms
Status output pins: GPIOx (x=1~4)					
t_r Output rise time	CL = 10 pF			6	ns
t_f Output fall time				6	ns
Hot plug detection pin: DP_HPD					
IRQ HPD pulse width (driven by sink device)		0.5		1.0	ms

POWER UP AND RESET TIMING SEQUENCE

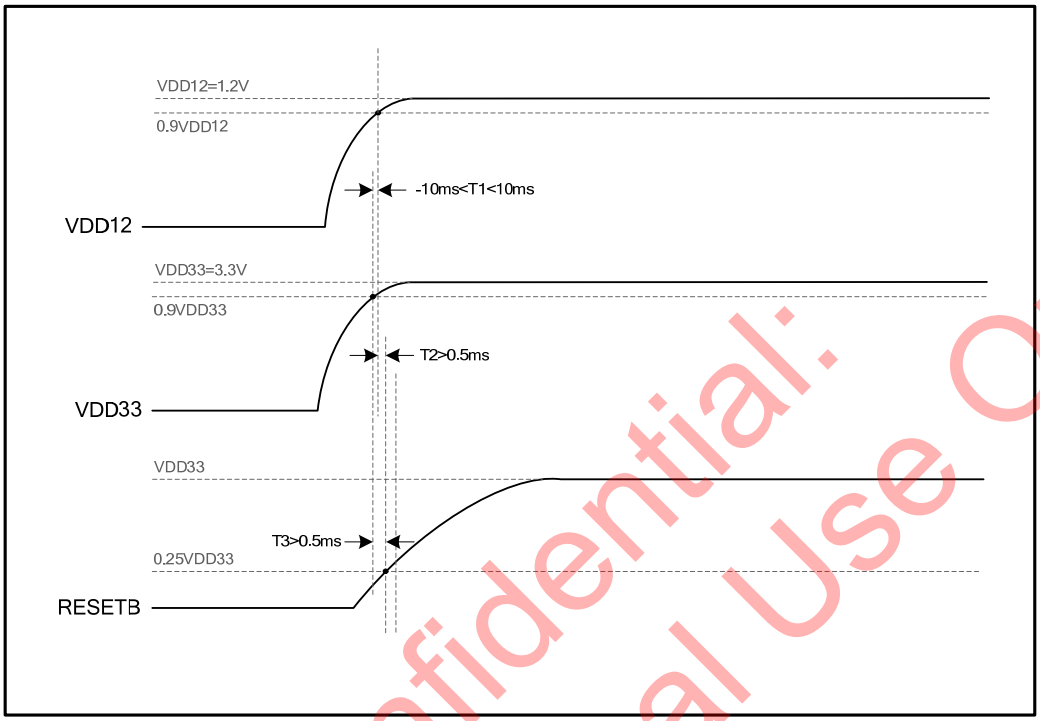


Figure 4. Power Up and Reset Timing Sequence

Note: The de-assertion of the RESETB shall follow by the timing sequence as given in the above diagram.

DISPLAYPORT™ AUX CHANNEL CHARACTERISTICS

Symbol and Parameter		Test Conditions	Min	Typ	Max	Unit
UI:	Unit Interval for AUX channel		0.4	0.5	0.6	µs
$V_{AUX-DIFF-p-p}$:	AUX differential peak-to-peak voltage at TP1 When AUX CH is driving the bus		400		900	mV
$V_{AUX-DIFF-p-p}$:	AUX differential peak-to-peak voltage at TP2 When AUX CH is receiving the bus		320		1360	mV
$I_{AUX-SHORT}$:	AUX channel short circuit current				20	mA
C_{AUX}:	AUX AC coupling capacitor		75		200	nF

DISPLAYPORT™ MAIN LINK RECEIVER CHARACTERISTICS

Symbol and Parameter	Test Conditions	Min	Typ	Max	Unit
Spread spectrum clock, down-spreading by SOURCE			0.5		%
Modulation Frequency		30		33	kHz
$V_{RX-DIFFp-p}$: Differential peak-to-peak input voltage at package pins		100		1360	mV
Maximum adaptive RX equalization level at 1.35GHz			9		dB
$V_{RX\_DC\_CM}$: RX input DC common mode voltage			GND		V
$R_{RX-DIFF}$: Differential termination resistance		80	100	120	Ω
R_{RX-SE}: Single-ended termination resistance		40	50	60	Ω
I_{RX_SHORT}: Rx short circuit current limit				20	mA
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (HBR2)				50	ps
RX intra-pair skew tolerance at HBR2					
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (HBR)				150	ps
RX intra-pair skew tolerance at HBR					
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (RBR)				300	ps
RX intra-pair skew tolerance at RBR					
Receiver Jitter Tolerance for High Bit Rate 2 (HBR2)					
Total jitter tolerance at 2MHz		1026			mUI
Total jitter tolerance at 10MHz		636			mUI
Total jitter tolerance at 20MHz		624			mUI
Total jitter tolerance at 100MHz		620			mUI
Receiver Jitter Tolerance for High Bit Rate (HBR)					
Total jitter tolerance at 2MHz		1227			mUI
Total jitter tolerance at 10MHz		548			mUI
Total jitter tolerance at 20MHz		505			mUI
Total jitter tolerance at 100MHz		491			mUI
Receiver Jitter Tolerance for Reduced Bit Rate (RBR)					
Total jitter tolerance at 2MHz		1648			mUI
Total jitter tolerance at 10MHz		778			mUI
Total jitter tolerance at 20MHz		747			mUI
Note: Jitter Tolerance Testing follows *VESA DisplayPort™ PHY Compliance Testing Specification, Version 1.2b.*					

HDMI TRANSMITTER CHARACTERISTICS

Symbol and Parameter	Test Conditions	Min	Typ	Max	Unit
1.65GHz<Data rate<3.4GHz					
V_{OD} Peak-to-peak differential output swing	AVcc = 3.3V, RT = 50 Ω	800	1000	1200	mV
V_{OH} Single end high-level output voltage		AVcc-200		AVcc+10	mV
V_{OL} Single end low-level output voltage		AVcc-700		AVcc-400	mV
t_r differential output rise time	AVcc = 3.3V, RT = 50 Ω	90		166	ps
t_f differential output fall time		90		166	ps
t_{sk_intra} intra-pair differential skew				0.15	T_{bit}
t_{sk_inter} inter-pair differential skew				0.50	T_{bit}
$t_{CK\text{-}jitter}$ output clock jitter	With 4MHz clock recovery bandwidth defined in HDMI CTS			0.25	T_{bit}
$t_{DATA\text{-}jitter}$ output data jitter				0.30	T_{bit}
3.4GHz<Data rate<6GHz					
Clock Channel	AVcc = 3.3V, RT = 50 Ω				
V_{OD} Peak-to-peak differential output swing		400	1000	1200	mV
V_{OH} Single end high-level output voltage		AVcc-400		AVcc+10	mV
V_{OL} Single end low-level output voltage		AVcc-1000		AVcc-200	mV
Data Channels					
V_{OD} Peak-to-peak differential output swing		800	1000	1200	mV
V_{OH} Single end high-level output voltage		AVcc-400		AVcc+10	mV
V_{OL} Single end low-level output voltage		AVcc-1000		AVcc-400	mV
Clock Channel	AVcc = 3.3V, RT = 50 Ω				
t_r differential output rise time		75			ps
t_f differential output fall time		75			ps
Data Channels					
t_r differential output rise time		42.5			ps
t_f differential output fall time		42.5			ps
t_{sk_intra} intra-pair differential skew				0.15	T_{bit}
t_{sk_inter} inter-pair differential skew				0.20	$T_{character}$

$t_{CK\text{-}jitter}$ output clock jitter	With 4MHz clock recovery bandwidth defined in HDMI CTS			0.30	T_{bit}
$t_{DATA\text{-}jitter}$ output data jitter				1-H	T_{bit}

Note: H is defined in HDMI specification 2.0, Figure 6-4 Eye Diagram at TP2_EQ

MEASUREMENT INFORMATION

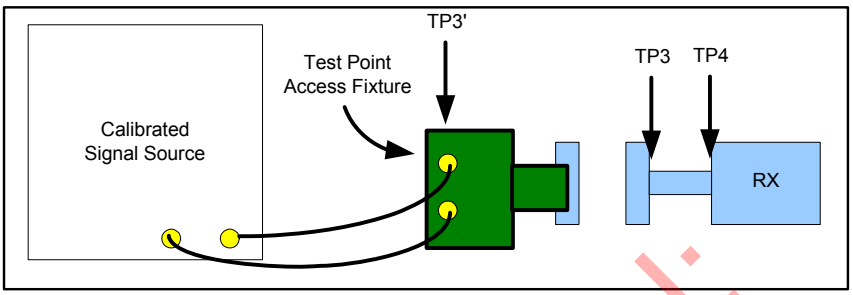


Figure 5. Measurement Setup for DisplayPort Sink Device

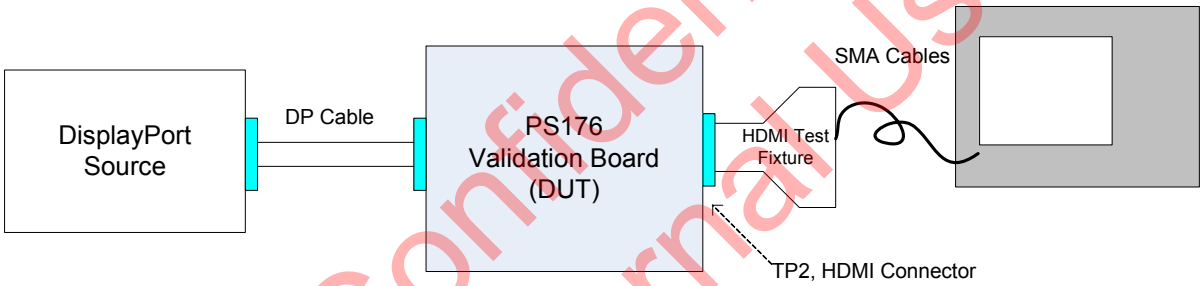


Figure 6. Measurement Setup for HDMI Source Device

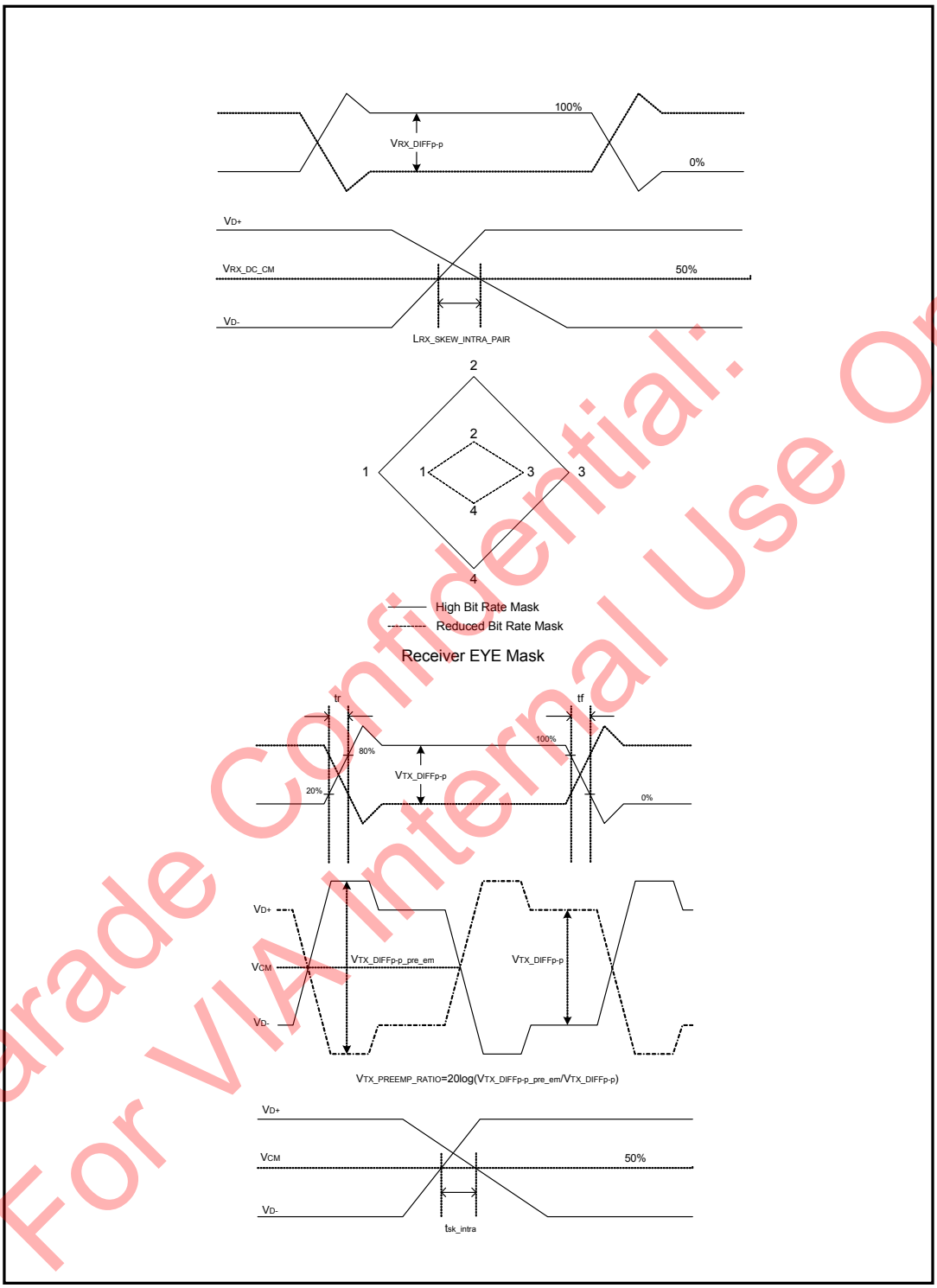


Figure 7. Definition of Key Parameters

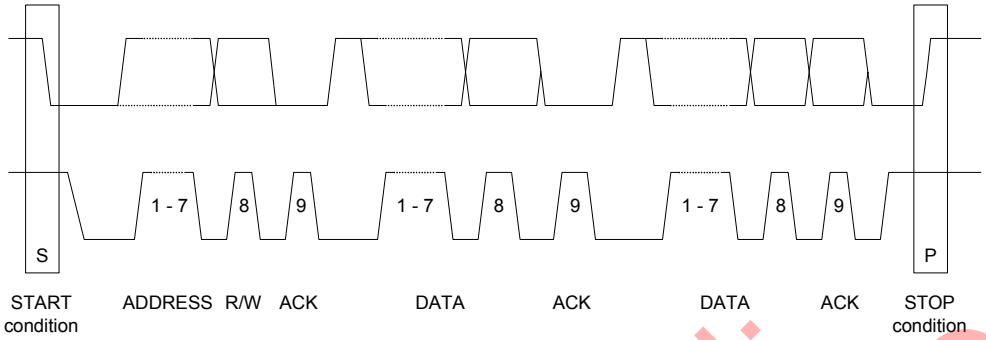


Figure 8. I2C Complete Data Transfer

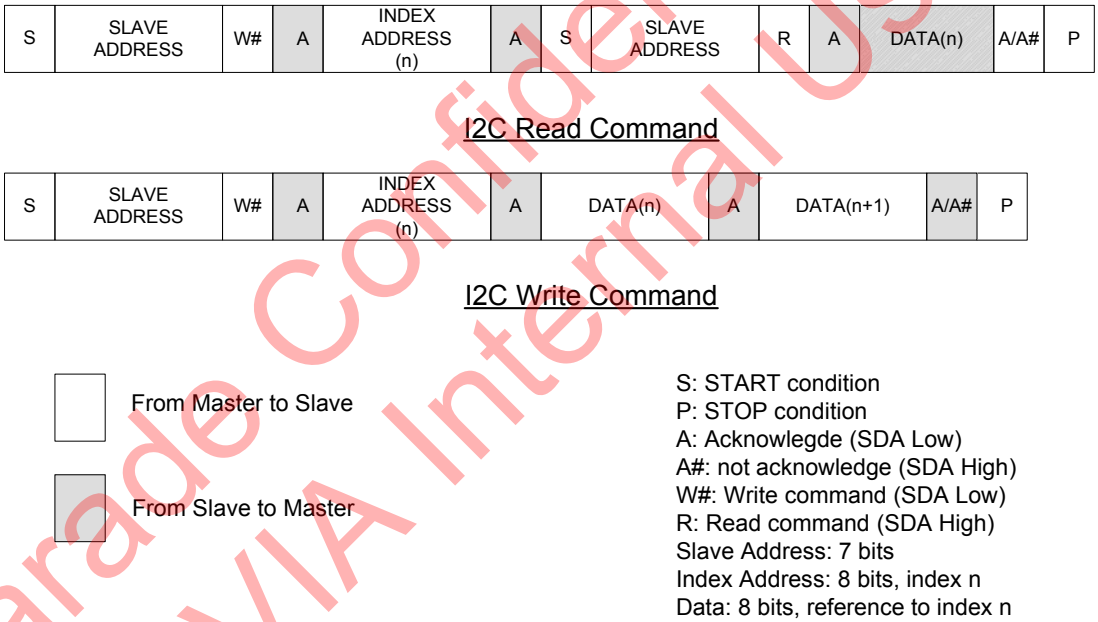


Figure 9. I2C Read and Write Command

Layout guidelines

High Speed Interfaces

- Select proper PCB stack up and trace width for 100 ohm differential transmission line impedance for high speed DisplayPort main link and AUX channels
- Avoid tight bend for differential signals
- Match intra-pair and inter-pair traces length within each differential pair
- Keep uninterrupted ground plane beneath differential signals
- Keep wide and shortest traces for both power and ground path to PS176

Filtering Capacitors

- Place 0.1uF capacitors on all VDD33, VDD12, VDDA12, VDDTX12 and VDDRX12 power pins. These capacitors shall be placed as close as possible to the chip package pins
- Place additional 0.01uF capacitor on the VDD12, VDDA12, VDDTX12 and VDDRX pins. These capacitors shall be placed as close as possible to the chip package pins

PCB LAYOUT PATTERN GUIDELINES – QFN48

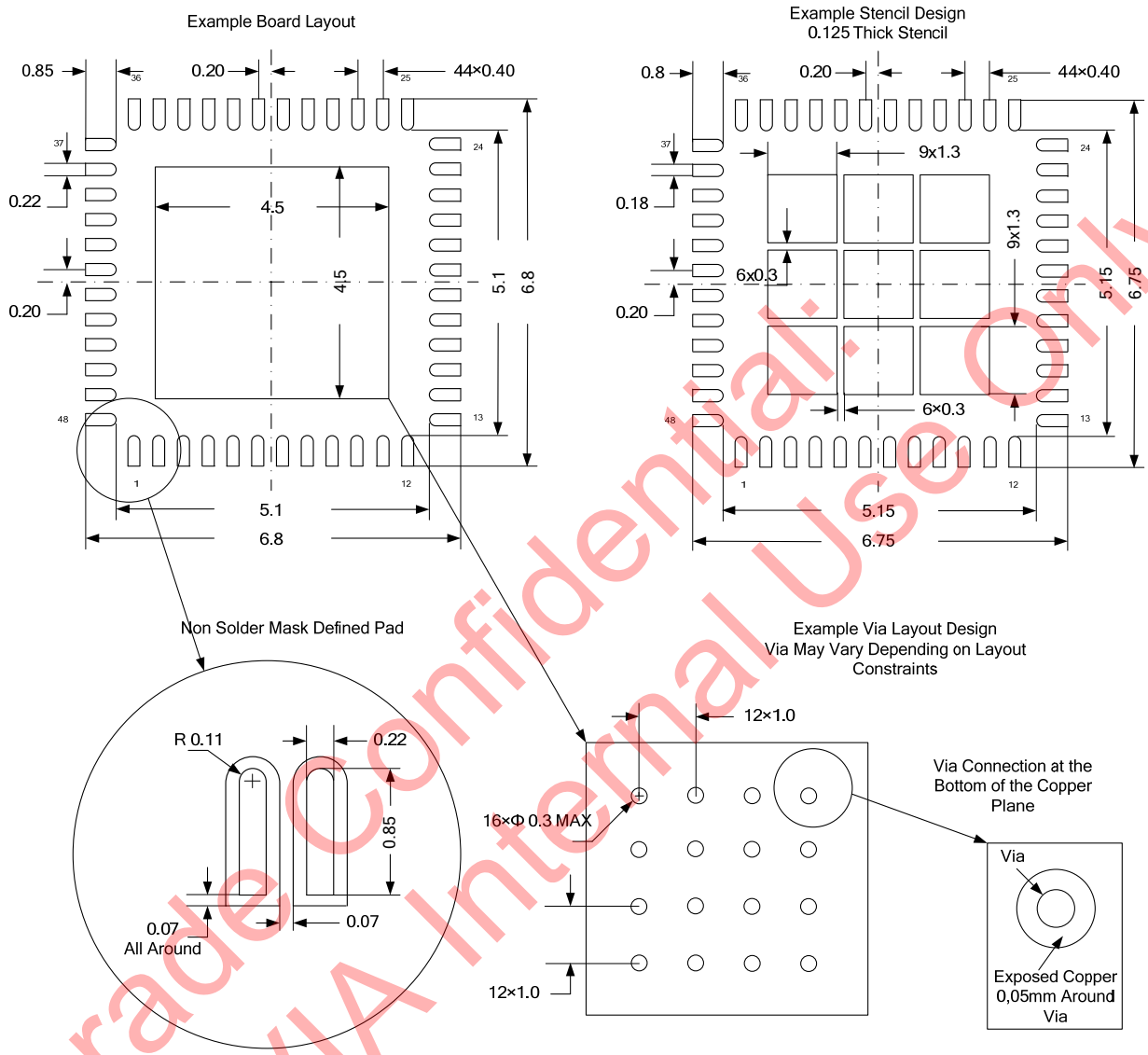


Figure10. The Exposed Thermal Pad Layout Guidelines – QFN48

NOTES:

1. All dimensions are in millimeters.
2. The drawing is subject to change without notice.
3. Customers should contact their board fabrication site for recommend solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

ORDER & PACKAGING INFORMATION – QFN48

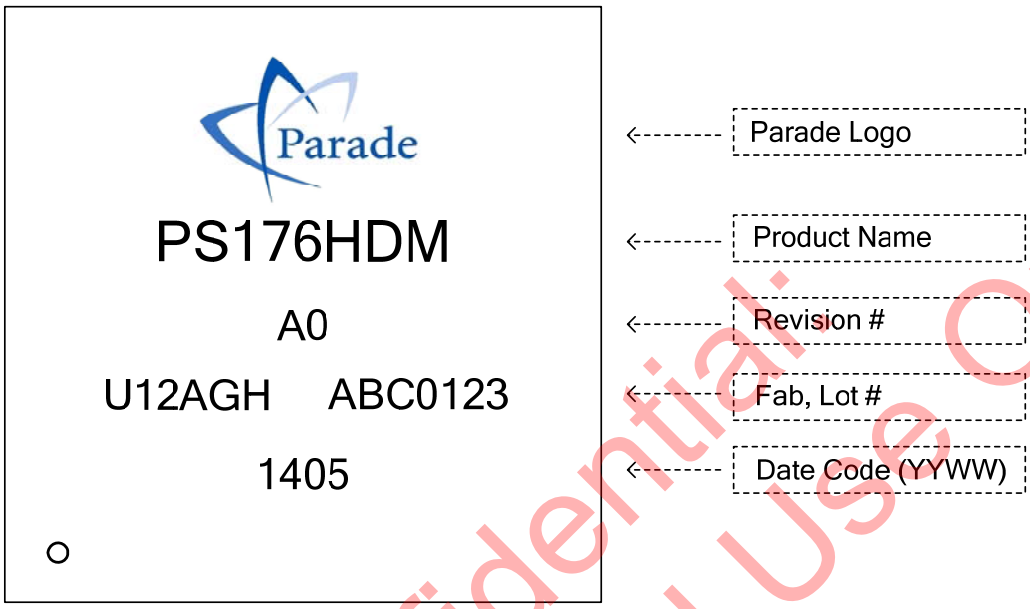
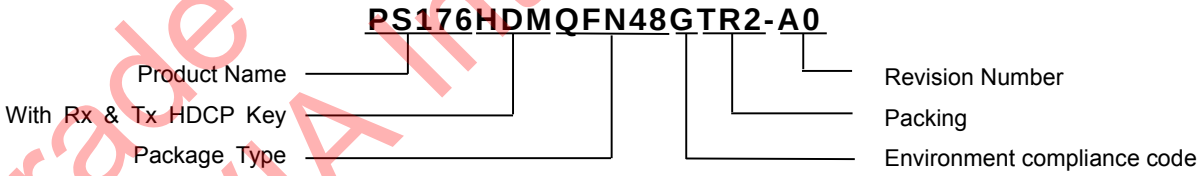


Figure11. Top Side Marking

Order Information:

Part number:

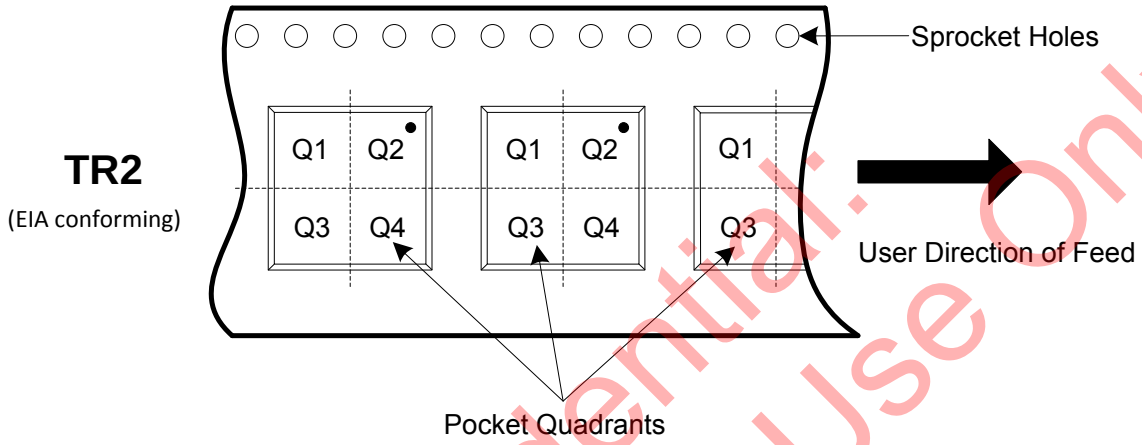


Part Number	Packing
PS176HDMQFN48GTR2-A0	Tape and Reel (EIA conforming)

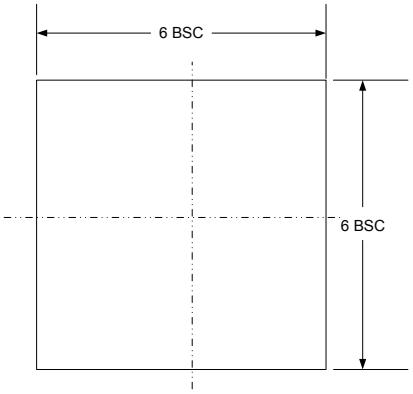
Lead Finish: 100% Sn

TAPE AND REEL PACKING PIN1 ORIENTATION – QFN48

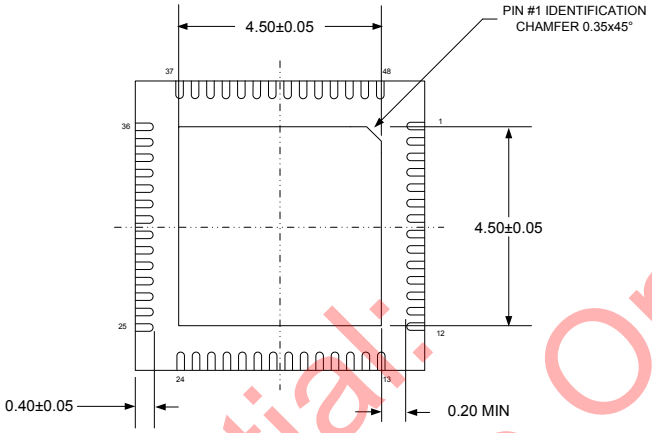
QUADRANT ASSIGNMENT FOR PIN1 ORIENTATION IN TAPE



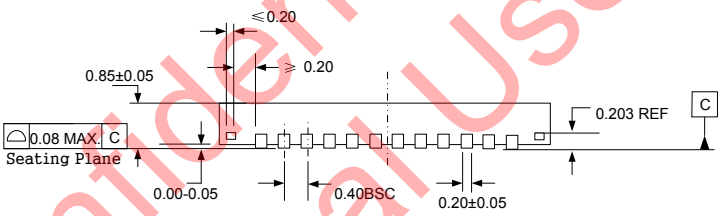
PHYSICAL DIMENSIONS – QFN48



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES:

1. All dimensions are in mm. Angles in degrees.
2. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
3. Refer JEDEC M0-220 modified.

REVISION HISTORY

Version	Date	Items
Preliminary	4/10/2014	Initial preliminary draft
Version 0.5	5/21/2014	Updated pin assignment
Version 0.6	8/21/2014	Update QFN package pin assignment, power consumption and thermal data