

## Description

The 25P06 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for high current load applications.

## General Features

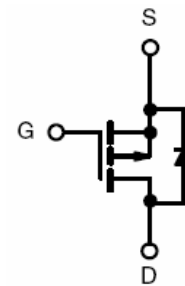
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$V_{DSS}$	$R_{DS(ON)}$ @ -4.5V(typ)	$I_D$
-60V	39m $\Omega$	-25A

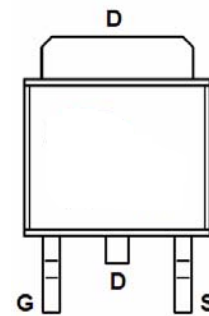
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

## Application

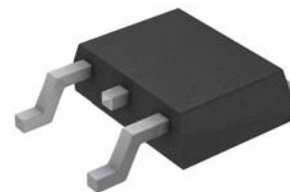
- High side switch for full bridge converter
- DC/DC converter for LCD display



Schematic diagram



Marking and pin assignment



To-252

## Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-25	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	-17.7	A
Pulsed Drain Current	$I_{DM}$	-60	A
Maximum Power Dissipation	$P_D$	90	W
Derating factor		0.72	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	300	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.4	°C/W
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## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

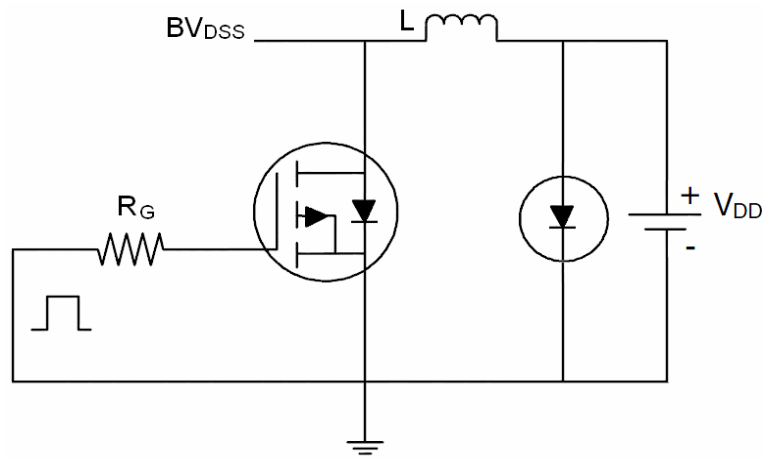
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-2	-2.9	-3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	39	45	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-10V, I_D=-10A$	-	25	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=-30V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	3430	-	PF
Output Capacitance	$C_{oss}$		-	391	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	272	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=1.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	12	-	nS
Turn-on Rise Time	$t_r$		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	nS
Turn-Off Fall Time	$t_f$		-	15	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-30, I_D=-20A,$ $V_{GS}=-10V$	-	46	-	nC
Gate-Source Charge	$Q_{gs}$		-	9.5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	10.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=-10A$	-	-	-1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	-25	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = -10A$	-	47	-	nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = -100A/\mu s(\text{Note 3})$	-	53	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

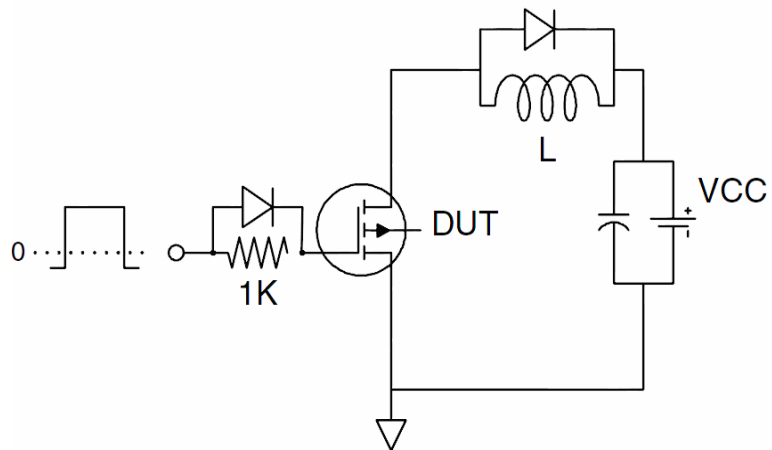
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^\circ\text{C}, V_{DD}=-20V, V_G=-10V, L=1\text{mH}, R_g=25\Omega, I_{AS}=33A$

## Test Circuit

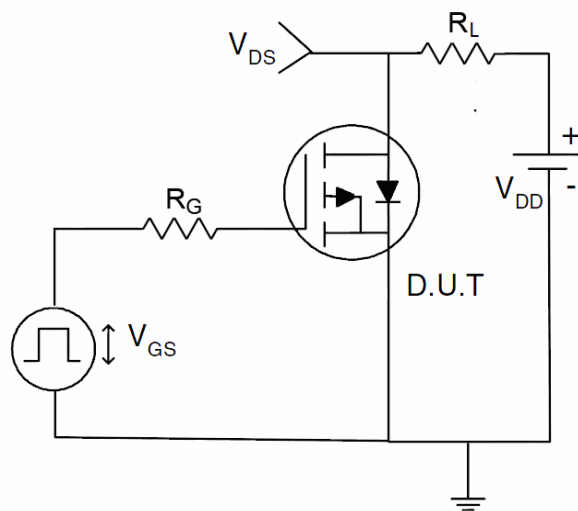
### 1) $E_{AS}$ Test Circuit



### 2) Gate Charge Test Circuit



### 3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

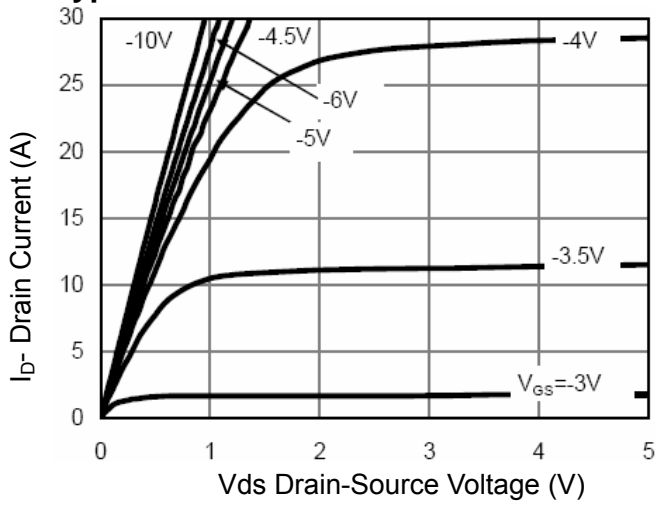


Figure 1 Output Characteristics

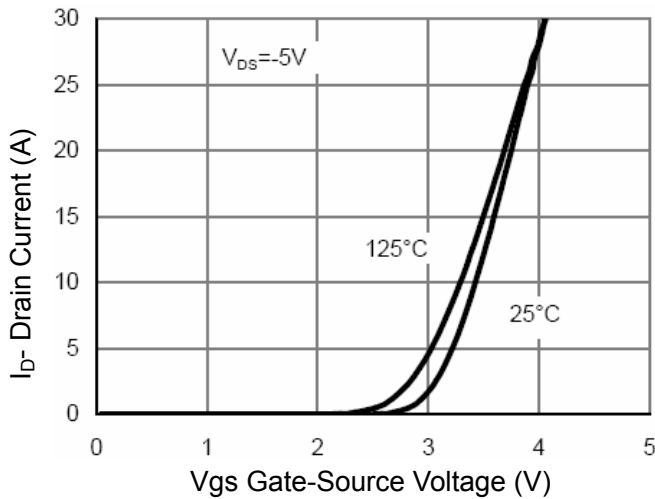


Figure 2 Transfer Characteristics

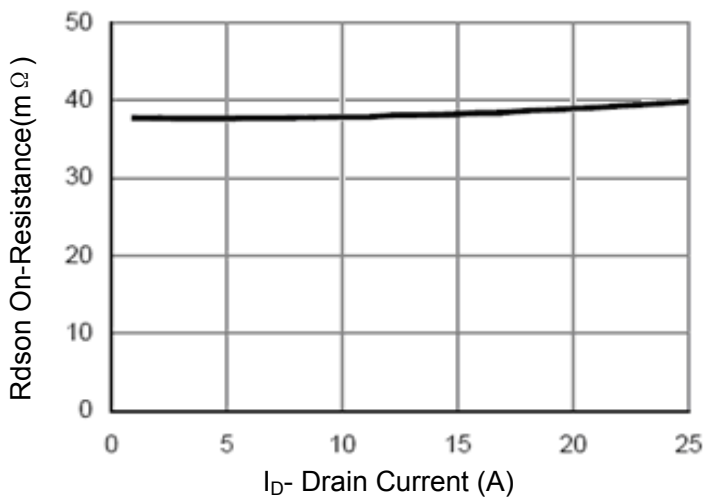


Figure 3 Rdson- Drain Current

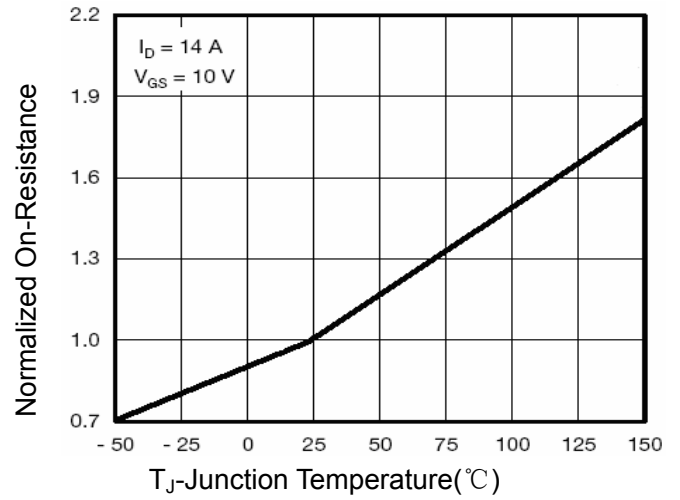


Figure 4 Rdson-Junction Temperature

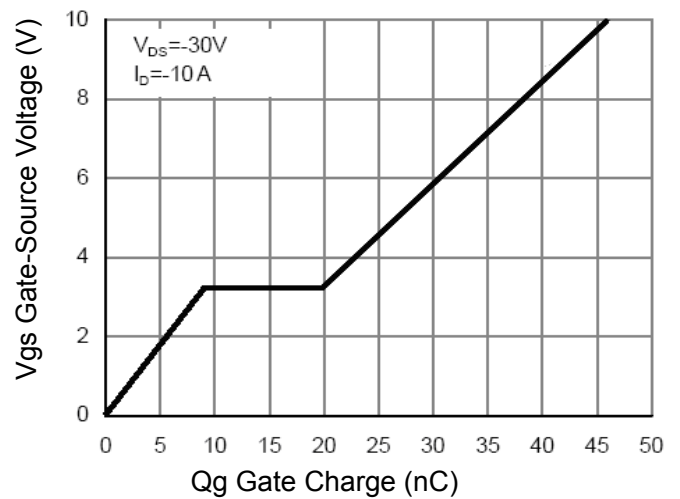


Figure 5 Gate Charge

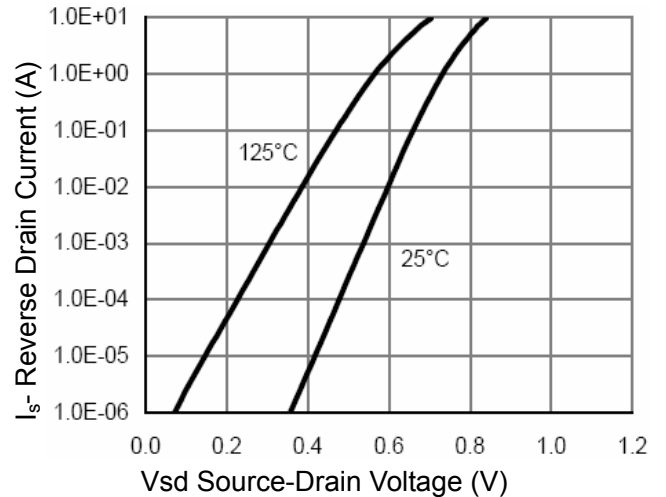


Figure 6 Source- Drain Diode Forward

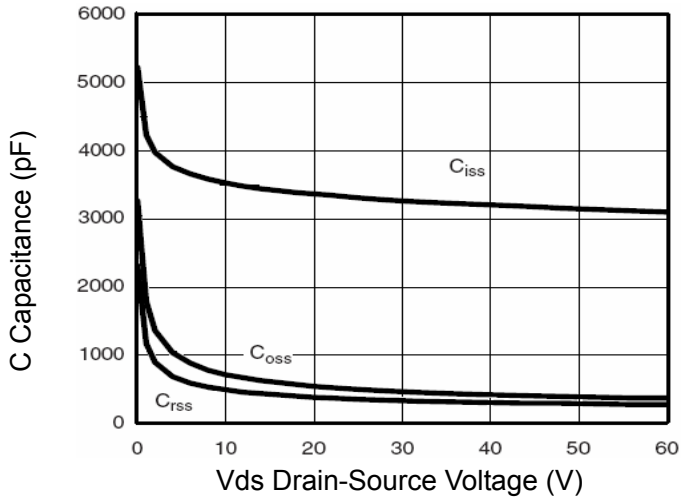


Figure 7 Capacitance vs Vds

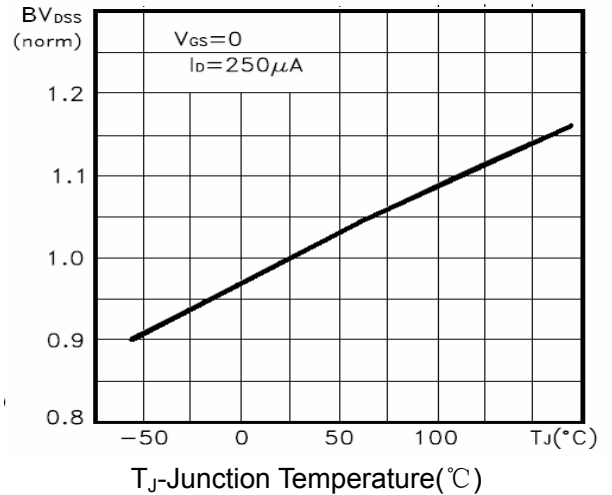


Figure 9  $BV_{DSS}$  vs Junction Temperature

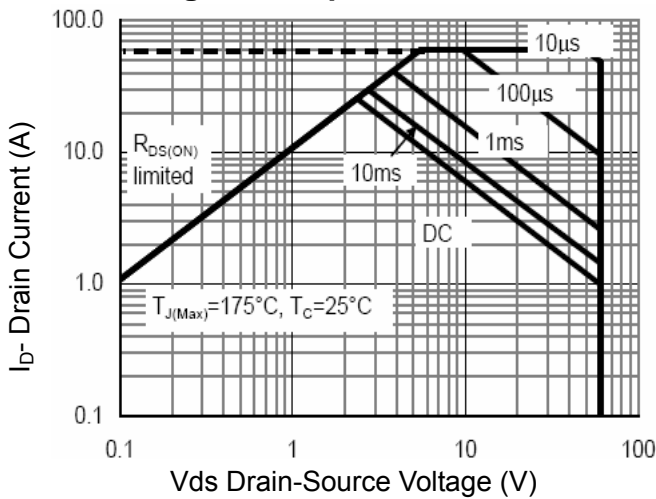


Figure 8 Safe Operation Area

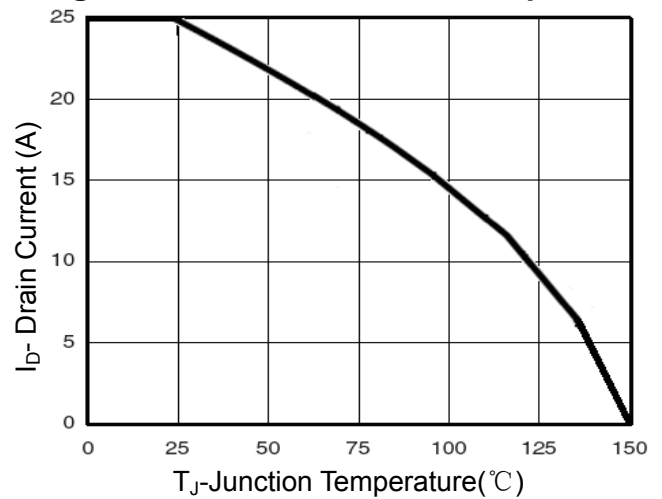


Figure 10  $I_D$  Current De-rating

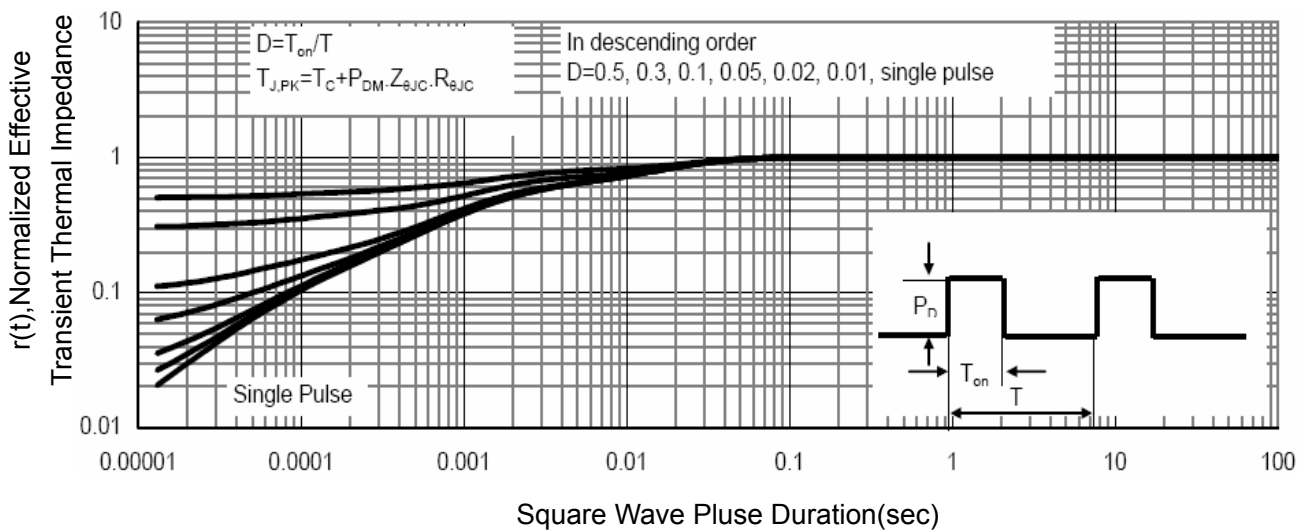


Figure 11 Normalized Maximum Transient Thermal Impedance