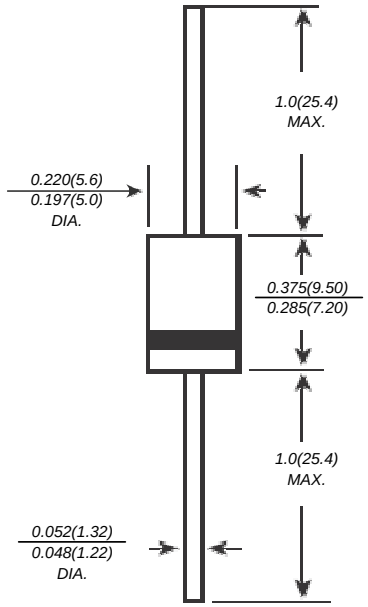
SB540L THRU SB5100L

Low-VF SCHOTTKY BARRIER RECTIFIER

Reverse Voltage -40 to 100 Volts Forward Current - 5.0 Ampere

DO-201AD



Dimensions in inches and (millimeters)

FEATURES

- The plastic package carris Underwriters Laboratory Flammability Classification 94V-0
- Construction utilizes void-free molded plastic technique
- Low reverse leakage
- High forward surge current capability
- High temperature soldering guaranteed: 250℃/10 seconds, 0.375" (9.5mm) lead length, 5 lbs. (2.3kg)tension

MECHANICAL DATA

Case: JEDECDO-201AD, Molded plastic body
Terminals: Plated axial leads, solderable per MIL-STD-750，Method 2026
Polarity: Color band denotse cathode end
Mounting Position: Any
Weight: 1.12 gram

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25℃ ambient temperature unless otherwis e specified.
Single phase half-wave 60Hz,resistive or inductive load,for capacitive load current derate by 20%.

PARAMETER	*SYMBOLS*	SB540L	SB545L	SB560L	SB5100L	UNITS
Maximum repetitive peak reverse voltage	V_{RRM}	40	45	60	100	Volts
Maximum RMS voltage	V_{RMS}	28	31.5	42	70	Volts
Minimum DC Breakdown Voltage	V_{DC}	40	45	60	100	Volts
Average Rectified current (see FIG-3.)	$I_{F(AV)}$	5.0				Amp
Non-repetitive Peak Forward Surge Current (note 1.)	I_{FSM}	150				Amps
Maximum Forward Voltage at 5.0A	V_F	0.49			0.7	Volts
Maximum DC Reverse Current T_J=25℃ at Reated DC Blocking Voltage T_J=100℃	I_R	0.5 50				mA
Typical Thermal Resistance (NOTE 2)	$R_{\theta JL}$	10			45	℃/W
Operating Junction Temperature Range	T_J	-55 ～ +150				℃
Storage Temperature Range	T_{STG}	-55 ～ +150				℃

Note: 1. 8.3ms single half sine-wave superimposed on rated load(JEDEC method)
2. Thermal Resistance Junction to Lead Vertical PC Board Mounting .375" (9.5mm) Lead Lengths.
3. T_J=25℃ unless otherwise specified.

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RATINGS AND CHARACTERISTIC CURVES

FIG. 1- Typical Forward Characteristics
40V~60V

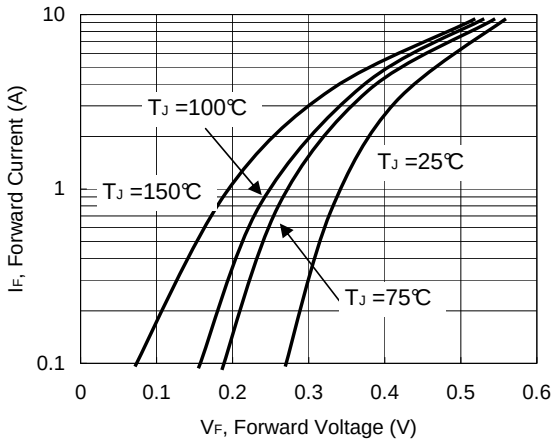

FIG. 2- Typical Forward Characteristics
100V

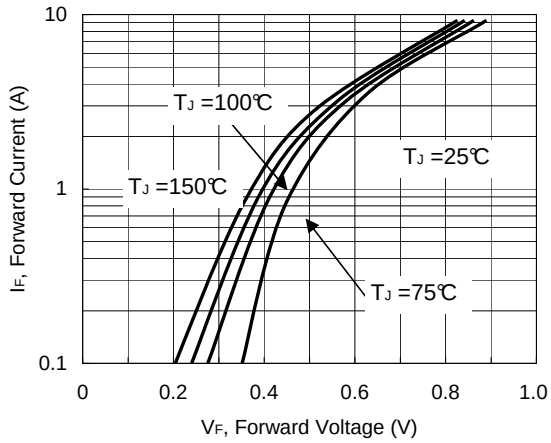

FIG. 3-Typical Reverse Characterstics

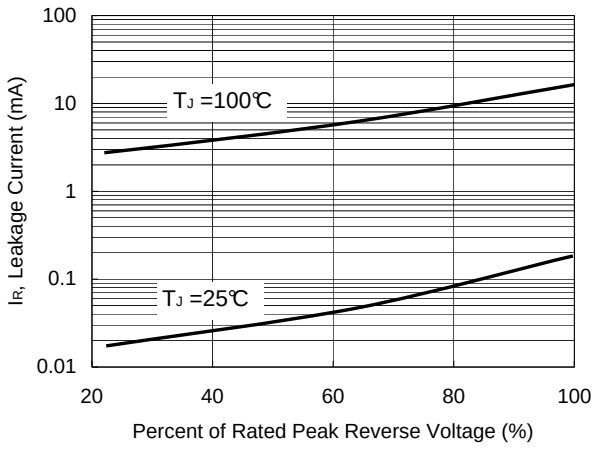

FIG. 4-Forward Current Derating Curve

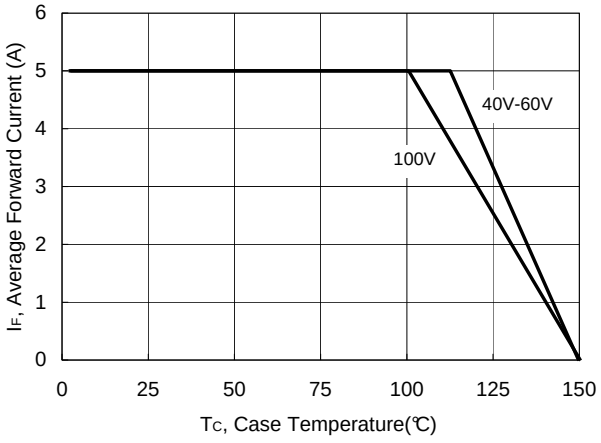

FIG. 5-Typical Junction Capacitance under Bias