SGM706
Low-Cost, Microprocessor Supervisory Circuit

GENERAL DESCRIPTION

The SGM706 microprocessor supervisory circuit reduces the complexity and number of components required to monitor power-supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The SGM706 provides power-supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with V_{CC} as low as 1V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.6 seconds.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply. An active-low manual-reset input ($\overline{MR}$) is also included.

The SGM706 is available in Green SOIC-8 package. The SGM706-S is available in both Green SOIC-8 and MSOP-8 packages. They operate over an ambient temperature range of -40℃ to +85℃.

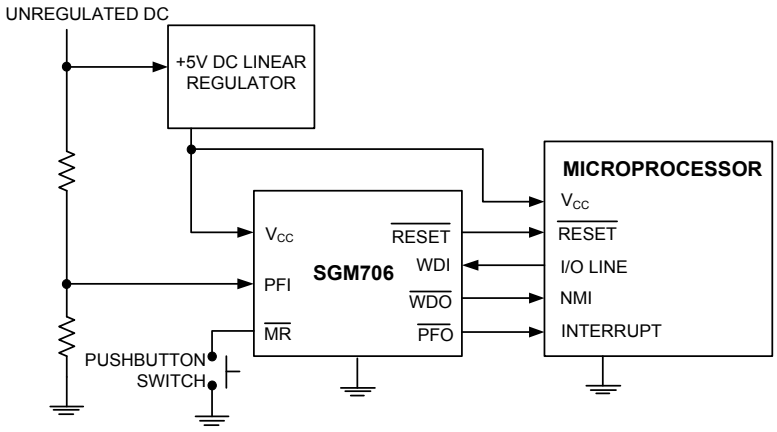
FEATURES

- **Precision Supply-Voltage Monitor**
  - **4.65V for SGM706-L**
  - **4.40V for SGM706-M**
  - **4.0V for SGM706-J**
  - **3.08V for SGM706-T**
  - **2.93V for SGM706-S**
  - **2.63V for SGM706-R**
- **Guaranteed $\overline{RESET}$ Valid at V_{CC} = 1V**
- **200ms Reset Pulse Width**
- **Debounced TTL/CMOS-Compatible Manual-Reset Input**
- **Independent Watchdog Timer (1.6sec) Timeout**
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **-40℃ to +85℃ Operating Temperature Range**
- **SGM706 is Available in Green SOIC-8 Package**
- **SGM706-S is Available in both Green SOIC-8 and MSOP-8 Packages**

APPLICATIONS

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

TYPICAL APPLICATION



PACKAGE/ORDERING INFORMATION

MODEL	RESET THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM706	4.65	SOIC-8	SGM706-LYS8G/TR	SGM706-LYS8 XXXXX	Tape and Reel, 4000
	4.40	SOIC-8	SGM706-MYS8G/TR	SGM706-MYS8 XXXXX	Tape and Reel, 4000
	4.0	SOIC-8	SGM706-JYS8G/TR	SGM706-JYS8 XXXXX	Tape and Reel, 4000
	3.08	SOIC-8	SGM706-TYS8G/TR	SGM706-TYS8 XXXXX	Tape and Reel, 4000
	2.93	SOIC-8	SGM706-SYS8G/TR	SGM706-SYS8 XXXXX	Tape and Reel, 4000
	2.93	MSOP-8	SGM706-SYMS8G/TR	SGM706S YMS8 XXXXX	Tape and Reel, 4000
	2.63	SOIC-8	SGM706-RYS8G/TR	SGM706-RYS8 XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

(Typical values are at T_A = +25℃, unless otherwise noted.)

Terminal Voltage (with respect to GND)

V_{CC} ..... -0.3V to 6.0V

All Other Inputs ..... -0.3V to (V_{CC} + 0.3V)

Input Current, V_{CC} 20mA

GND 20mA

Output Current, (all outputs) 20mA

Operating Temperature Range ..... -40℃ to +85℃

Junction Temperature ..... 150℃

Storage Temperature ..... -65℃ to +150℃

Lead Temperature (Soldering, 10sec) ..... 260℃

ESD Susceptibility

HBM 4000V

MM 300V

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

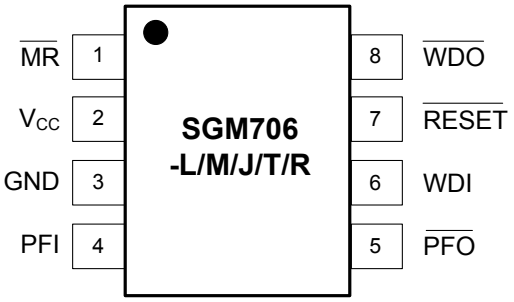
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

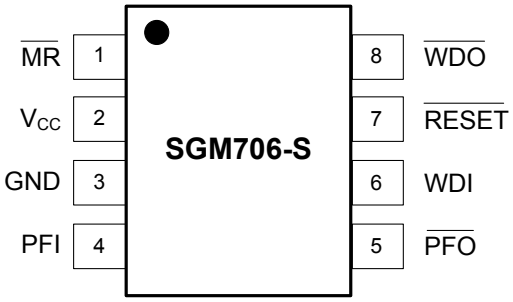
PIN CONFIGURATIONS

SGM706-L/M/J/T/R (TOP VIEW)



SOIC-8

SGM706-S (TOP VIEW)



SOIC-8/MSOP-8

PIN DESCRIPTION

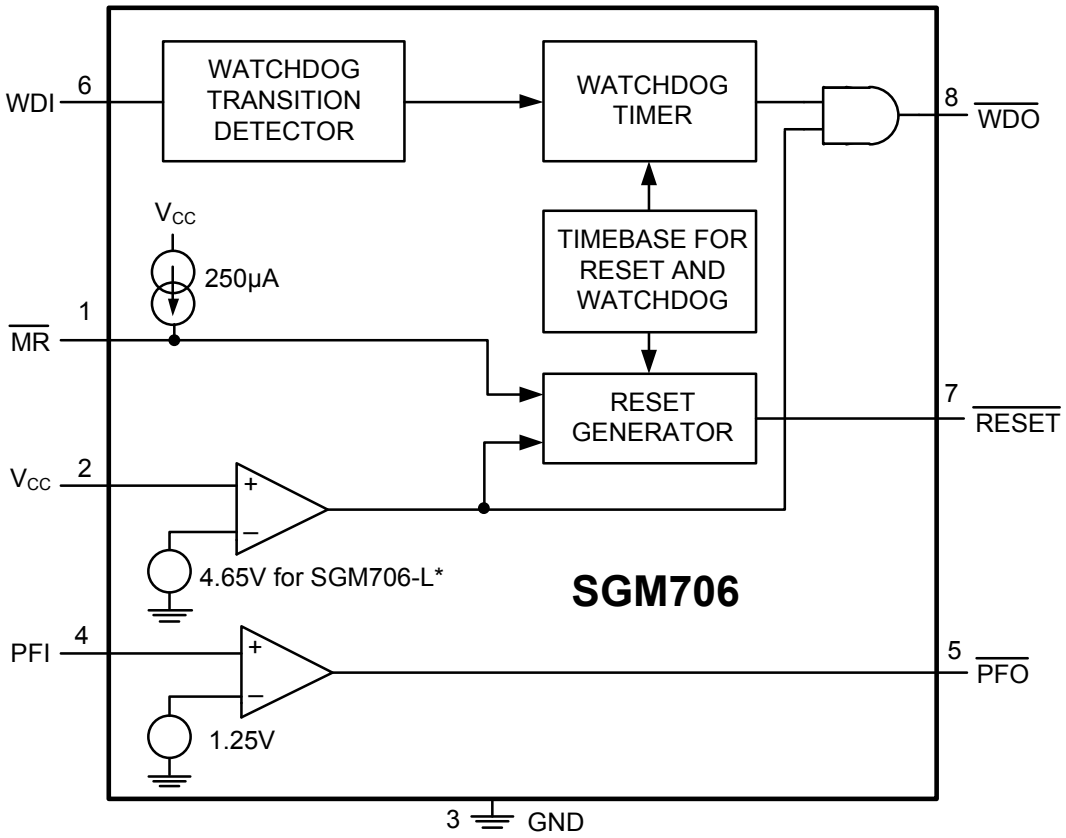
PIN	NAME	FUNCTION
1	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250μA (V_{CC} = +5V) pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	V_{CC}	Power Supply Voltage that is monitored.
3	GND	0V Ground Reference for all signals.
4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (BLOCK DIAGRAM). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
7	$\overline{RESET}$	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (4.65V for SGM706-L, 4.4V for SGM706-M, 4.0V for SGM706-J, 3.08V for SGM706-T and 2.93V for SGM706-S, 2.63V for SGM706-R). It remains low for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V for SGM706-L; V_{CC} = 4.5V to 5.5V for SGM706-M; V_{CC} = 4.07V to 5.5V for SGM706-J; V_{CC} = 3.14V to 5.5V for SGM706-T; V_{CC} = 2.95V to 5.5V for SGM706-S; V_{CC} = 2.68V to 5.5V for SGM706-R; T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range (V_{CC})			1.0		5.5	V
Supply Current (I_{SUPPLY})				50	150	μA
Reset Threshold (V_{RT})		SGM706-L	4.5	4.65	4.75	V
		SGM706-M	4.25	4.4	4.5	
		SGM706-J	3.91	4.0	4.07	
		SGM706-T	3.02	3.08	3.14	
		SGM706-S (SOIC-8)	2.85	2.93	2.95	
		SGM706-S (MSOP-8)	2.82	2.93	2.95	
		SGM706-R	2.56	2.63	2.68	
Reset Threshold Hysteresis		SGM706-L, SGM706-M		40		mV
		SGM706-J		34		
		SGM706-T, SGM706-S		25		
		SGM706-R		22		
Reset Pulse Width (t_{RS})			120	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800μA	V_{CC} - 1.5			V
		I_{sink} = 3.2mA			0.4	
		V_{CC} = 1V, I_{sink} = 50μA			0.3	
Watchdog Timeout Period (t_{WD})			1.0	1.6	2.25	sec
WDI Pulse Width (t_{WP})		V_{IL} = 0.4V, V_{IH} = V_{CC}	70			ns
WDI Input Threshold	Low	V_{CC} = 5V			0.8	V
	High	V_{CC} = 5V	3.5			
	Low	$V_{RST(MAX)}$ < V_{CC} < 3.6V			0.8	
	High	$V_{RST(MAX)}$ < V_{CC} < 3.6V	0.7 × V_{CC}			
WDI Input Current		WDI = V_{CC}		50	150	μA
		WDI = 0V	-150	-50		
$\overline{WDO}$ Output Voltage		I_{SOURCE} = 800μA	V_{CC} - 1.5			V
		I_{sink} = 1.2mA			0.4	
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ = 0V	100		600	μA
$\overline{MR}$ Pulse Width (t_{MR})			250			ns
$\overline{MR}$ Input Threshold	Low	T_A = +25℃			0.8	V
	High		2			
$\overline{MR}$ to Reset Out Delay (t_{MD})					350	ns
PFI Input Threshold		V_{CC} = 5V	1.18	1.25	1.3	V
PFI Input Current				0.2		nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800μA	V_{CC} - 1.5			V
		I_{sink} = 3.2mA			0.4	

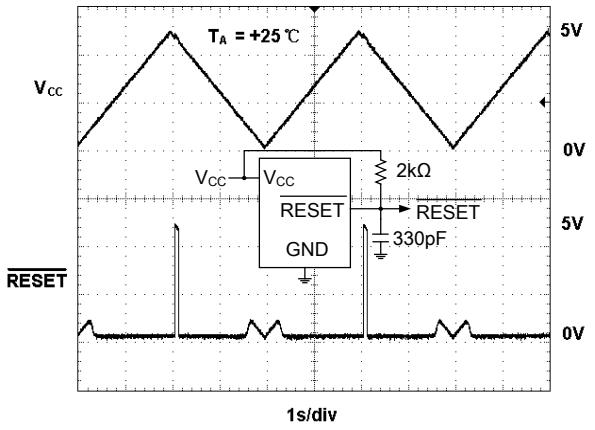
FUNCTIONAL BLOCK DIAGRAM



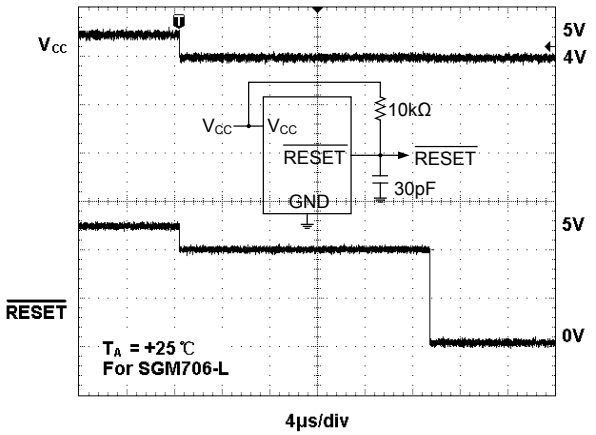
* 4.65V for SGM706-L
4.40V for SGM706-M
4.0V for SGM706-J
3.08V for SGM706-T
2.93V for SGM706-S
2.63V for SGM706-R

TYPICAL PERFORMANCE CHARACTERISTICS

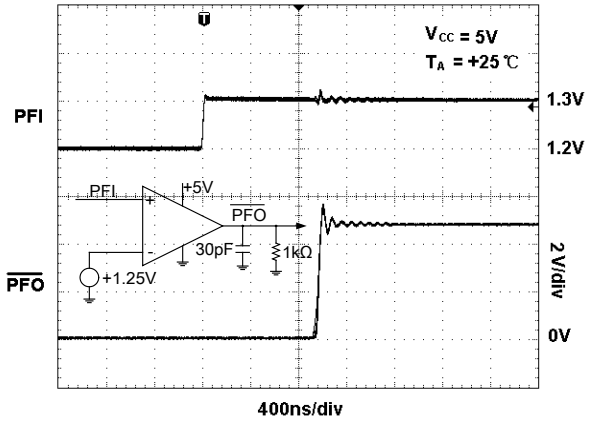
$\overline{RESET}$ Output Voltage vs. Supply Voltage



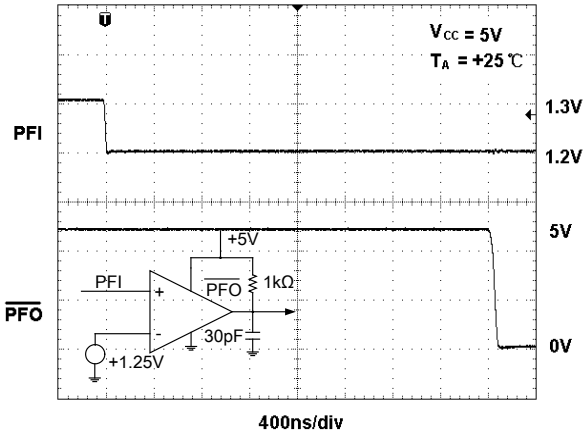
$\overline{RESET}$ Response Time



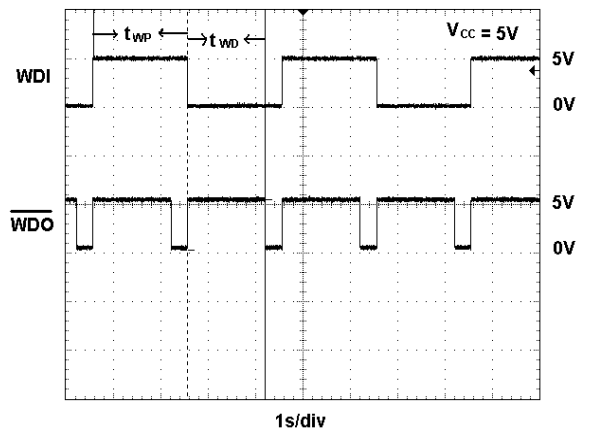
Power-Fall Comparator De-assertion Response Time



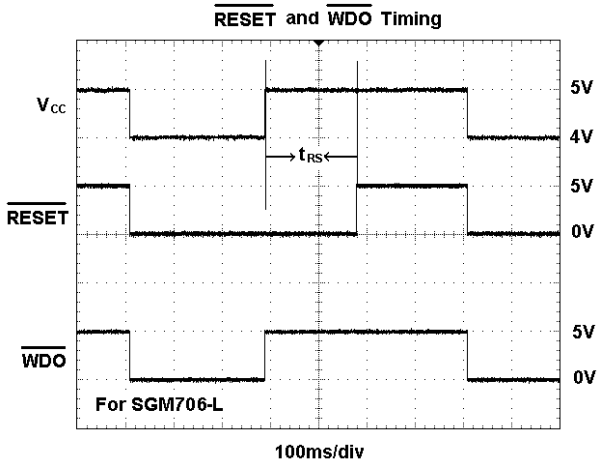
Power-Fall Comparator Assertion Response Time



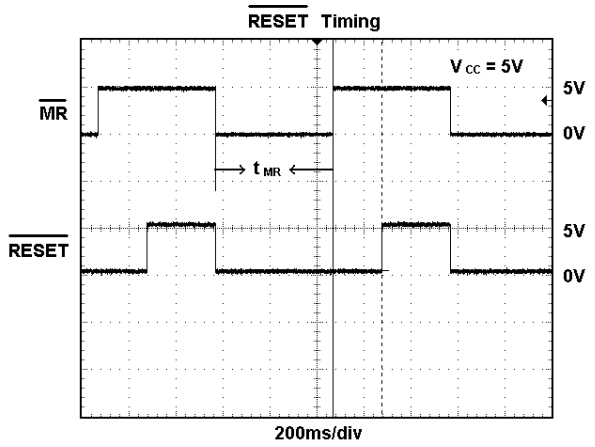
Watchdog Timing



$\overline{RESET}$ and $\overline{WDO}$ Timing



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



APPLICATION NOTES

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the SGM706 $\overline{\text{RESET}}$ output no longer sinks current-it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the $\overline{\text{RESET}}$ pin as shown in Figure 1, any stray charge or leakage currents will be drained to ground, holding $\overline{\text{RESET}}$ low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

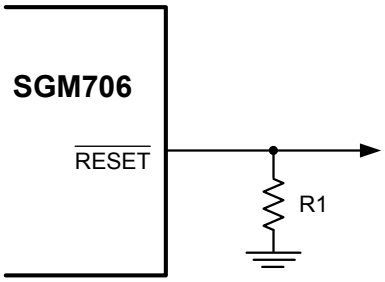


Figure 1. $\overline{\text{RESET}}$ Valid to Ground Circuit

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{\text{PFO}}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{\text{RESET}}$ can be asserted on other voltages in addition to the +5V V_{CC} line. Connect $\overline{\text{PFO}}$ to $\overline{\text{MR}}$ to initiate a $\overline{\text{RESET}}$ pulse when PFI drops below 1.25V. Figure 2 shows the SGM706 configured to assert $\overline{\text{RESET}}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

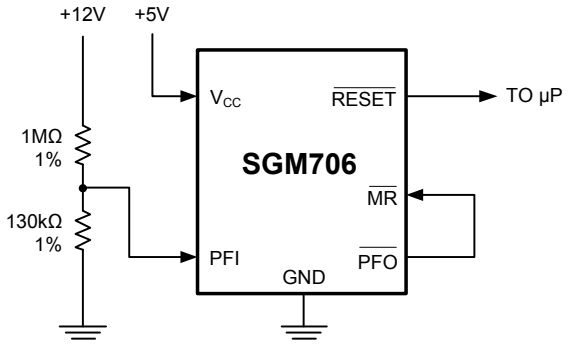
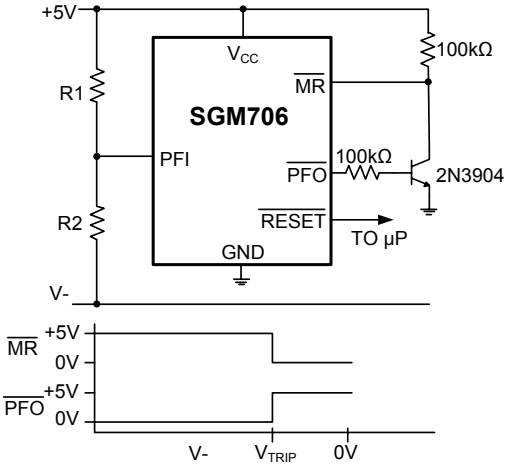


Figure 2. Monitoring Both +5V and +12V

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 3). When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{\text{PFO}}$ is high. By adding the resistors and transistor as shown, a high $\overline{\text{PFO}}$ triggers reset. As long as $\overline{\text{PFO}}$ remains high, the SGM706 will keep reset asserted ($\overline{\text{RESET}}$ = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.



$$\frac{5 - 1.25}{R1} = \frac{1.25 - V_{TRIP}}{R2} \qquad V_{TRIP} < 0$$

Figure 3. Monitoring a Negative Voltage

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the SGM706 $\overline{\text{RESET}}$ output. If, for example, the $\overline{\text{RESET}}$ output is driven high and the Microprocessor wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{\text{RESET}}$ output and the µP reset I/O, as in Figure 4. Buffer the $\overline{\text{RESET}}$ output to other system components.

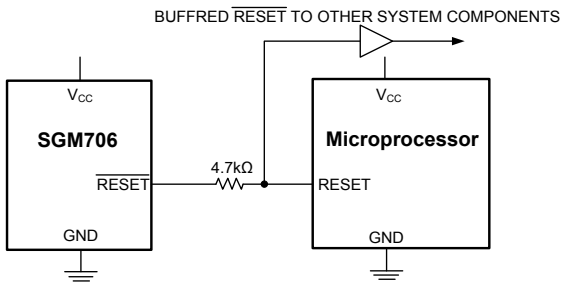


Figure 4. Interfacing to Microprocessors with Bidirectional Reset I/O

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2017 – REV.A.3 to REV.A.4

SGM706-S Added MSOP-8 Package ..... All

MARCH 2017 – REV.A.2 to REV.A.3

Changed Packing Option 2

JANUARY 2013 – REV.A.1 to REV.A.2

Added Recommended Land Pattern Information 10
Added Tape and Reel Information 11, 12

MAY 2011 – REV.A to REV.A.1

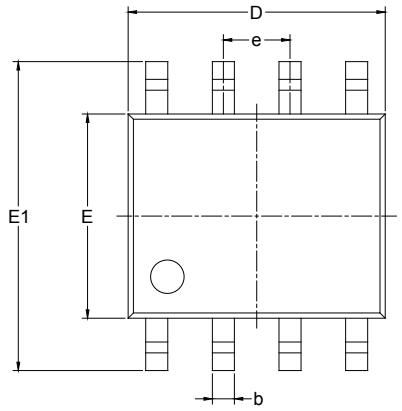
Updated Package Description ..... All

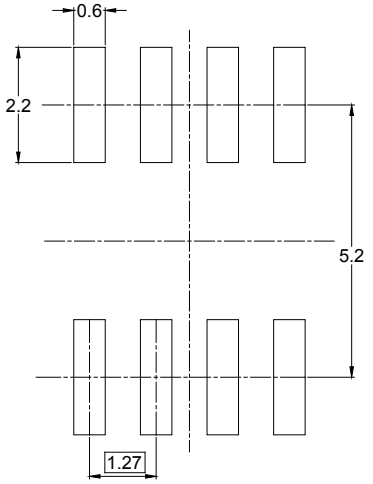
Changes from Original (APRIL 2010) to REV.A

Changed from product preview to production data ..... All

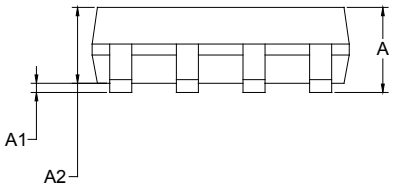
PACKAGE OUTLINE DIMENSIONS

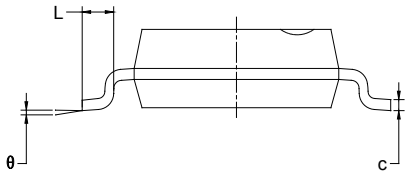
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

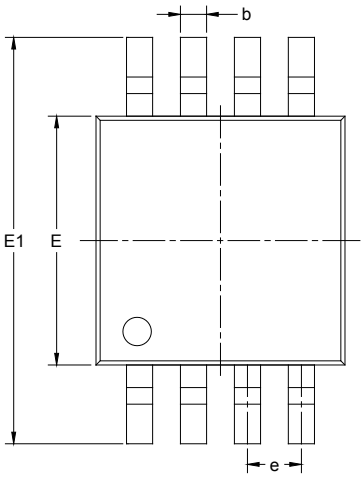


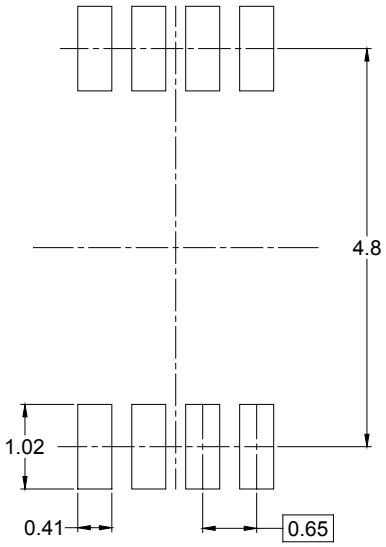


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

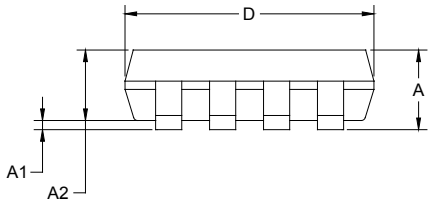
PACKAGE OUTLINE DIMENSIONS

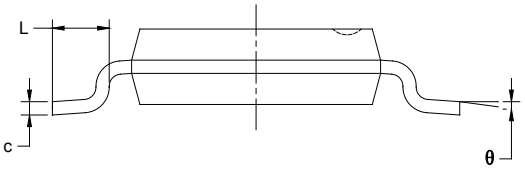
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

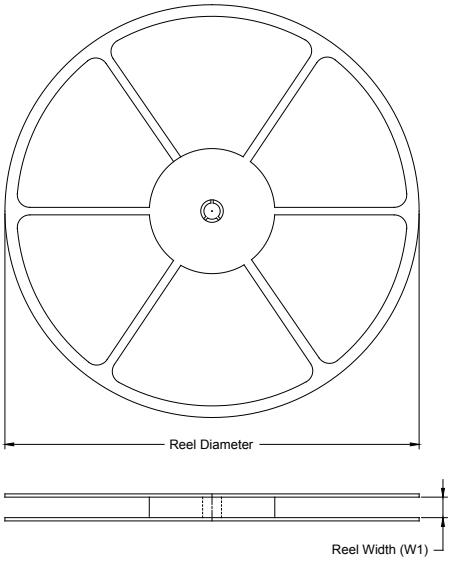




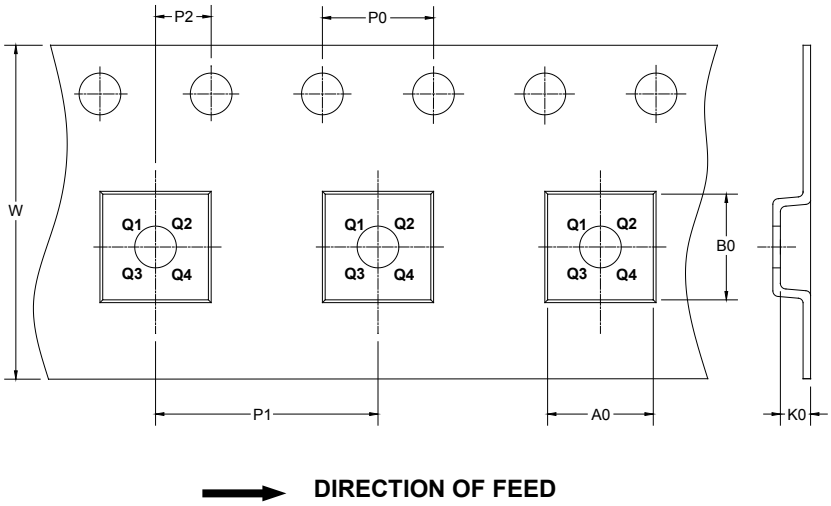
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



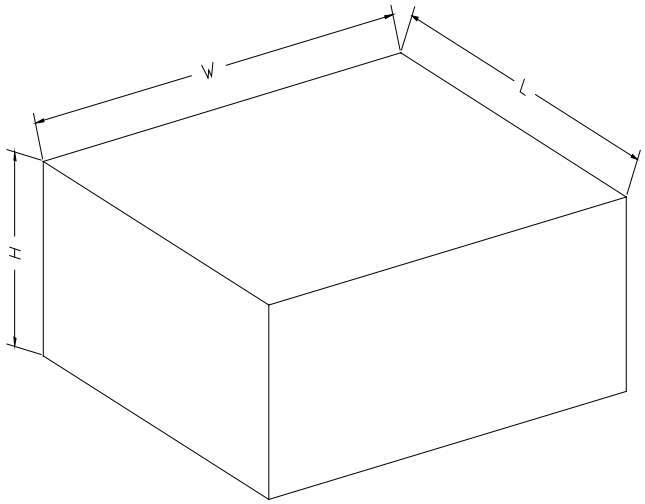
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002