SS54L~SS56L

SURFACE MOUNT SCHOTTKY BARRIER RECTIFIER

VOLTAGE 40~60 Volts **CURRENT** 5.0 Amperes

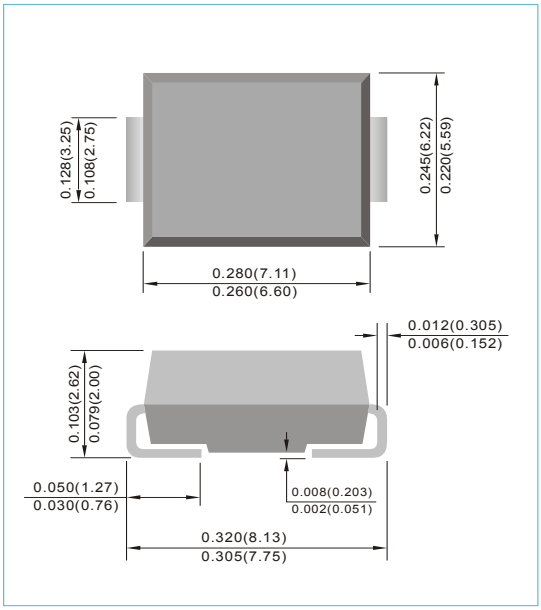
FEATURES

- Plastic package has Underwriters Laboratory Flammability Classification 94V-O
- For surface mounted applications
- Low profile package
- Built-in strain relief
- Metal to silicon rectifier. majority carrier conduction
- Low power loss,high efficiency
- High surge capacity
- For use in low voltage high frequency inverters, free wheeling, and polarity protection applications
- Lead free in comply with EU RoHS 2011/65/EU directives
- Green molding compound as per IEC61249 Std. . (Halogen Free)

MECHANICAL DATA

- Case: JEDEC DO-214AB molded plastic
- Terminals:Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity: Color band denotes cathode end
- Standard packaging: 16mm tape (EIA-481)
- Weight: 0.0082 ounce, 0.2325 gram

SMC / DO-214AB Unit : inch(mm)



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified. Resistive or inductive load.

PARAMETER	SYMBOL	SS54	SS56L	UNITS
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	40	60	V
Maximum RMS Voltage	V_{RMS}	28	42	V
Maximum DC Blocking Voltage	V_{DC}	40	60	V
Maximum Average Forward Rectified Current at T_C=120°C	$I_{F(AV)}$	5.0		A
Peak Forward Surge Current : 8.3ms single half sine-wave superimposed on rated load (JEDEC method)	I_{FSM}	100		A
Maximum Forward Voltage at 5.0A (Note 1)	V_F	0.44	0.50	V
Maximum DC Reverse Current at Rated DC Blocking Voltage T_J=25°C T_J=100°C	I_R	0.5 50		mA
Typical Thermal Resistance (Note 2)	$R_{\theta JL}$	17.0		°C / W
Operating Junction Temperature Range	T_J	-55 to +150		°C
Storage Temperature Range	T_{STG}	-55 to +150		°C

NOTES:

1. Pulse Test with PW =300μsec, 1% Duty Cycle.
2. Mounted on P.C. Board with 14mm^2 (.013mm thick) copper pad areas.

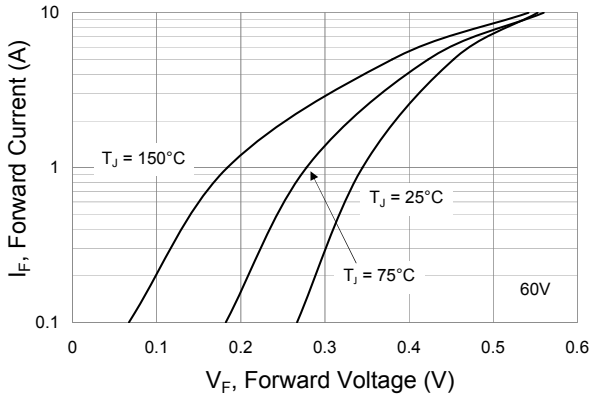


Fig.1 Typical Forward Characteristics

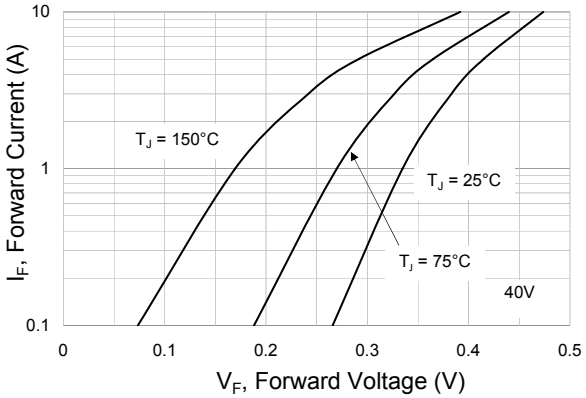


Fig.2 Typical Forward Characteristics

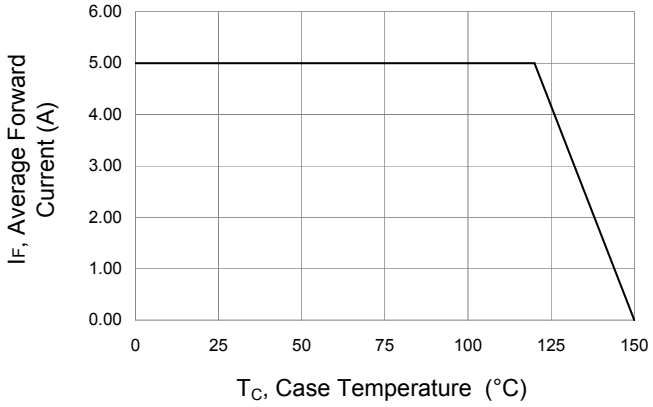


Fig.3 Forward Current Derating Curve

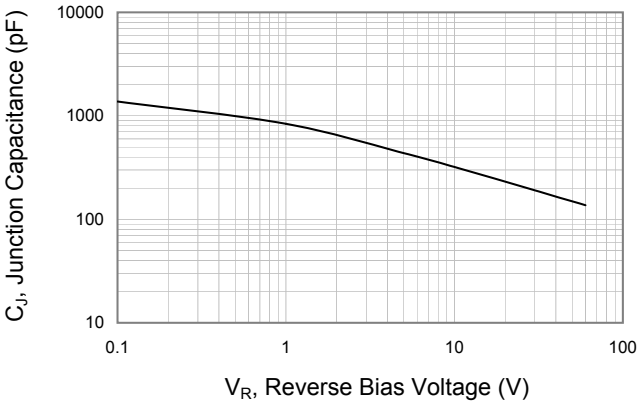


Fig.4 Typical Junction Capacitance under Bias

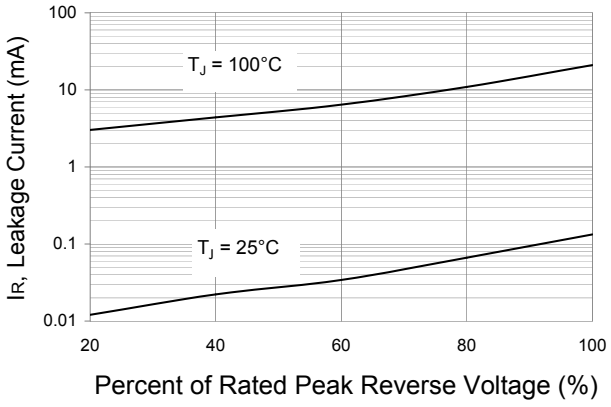


Fig.5 Typical Reverse Characteristics