

**SE9926**  
**N-Channel Enhancement Mode Field Effect Transistor**

Revision:B

**Features**

- $V_{DS} = 20V, I_D = 6A$   
 $R_{DS(ON)} < 37.5m\Omega @ V_{GS} = 2.5V$   
 $R_{DS(ON)} < 27.5m\Omega @ V_{GS} = 4.5V$
- High Power and current handling capability
- Lead free product is acquired
- Surface Mount Package

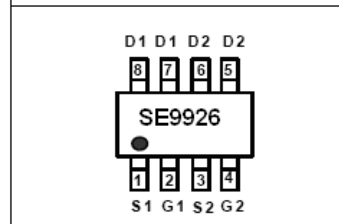
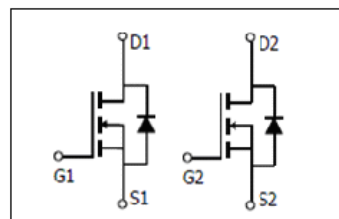
**Applications**

- Battery protection
- Load switch
- Power management

**Construction**

- Silicon epitaxial planer

**External Dimensions**



**Absolute maximum ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	$I_D$	6	A
	$I_{DM}$	25	A
Maximum Power Dissipation	$P_D$	1.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

**THERMAL CHARACTERISTICS**

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	83	°C/W
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**Electrical characteristics (Ta=25°C)**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			0.8	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS} = \pm 10V, V_{DS} = 0V$			$\pm 80$	nA

# SE9926

<b>ON CHARACTERISTICS (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.65	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=4.5A$		21	27.5	mΩ
		$V_{GS}=2.5V, I_D=3.5A$		30	37.5	mΩ
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=4.5A$	3			S
<b>DYNAMIC CHARACTERISTICS (Note4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=8V, V_{GS}=0V,$ $F=1.0MHz$		600		PF
Output Capacitance	$C_{oss}$			330		PF
Reverse Transfer Capacitance	$C_{rss}$			140		PF
<b>SWITCHING CHARACTERISTICS (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A$ $V_{GS}=4.5V, R_{GEN}=6\Omega$		10	20	nS
Turn-on Rise Time	$t_r$			11	25	nS
Turn-Off Delay Time	$t_{d(off)}$			35	70	nS
Turn-Off Fall Time	$t_f$			30	60	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=6A,$ $V=4.5V$		10	15	nC
Gate-Source Charge	$Q_{gs}$			2.3		nC
Gate-Drain Charge	$Q_{gd}$			3		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V=0V, I=1.7A$			1.2	V
Diode Forward Current (Note 2)	$I_S$			1.7		A

**NOTES:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production testing.

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

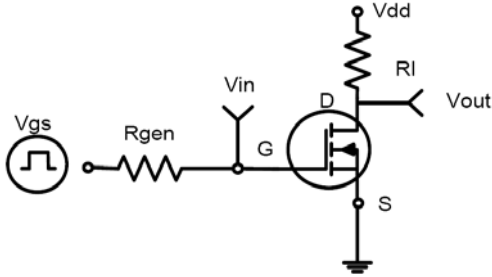


Figure 1: Switching Test Circuit

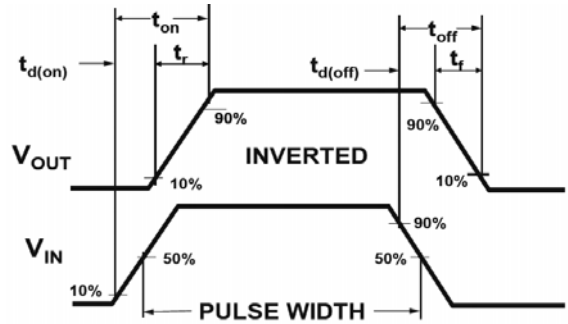


Figure 2: Switching Waveforms

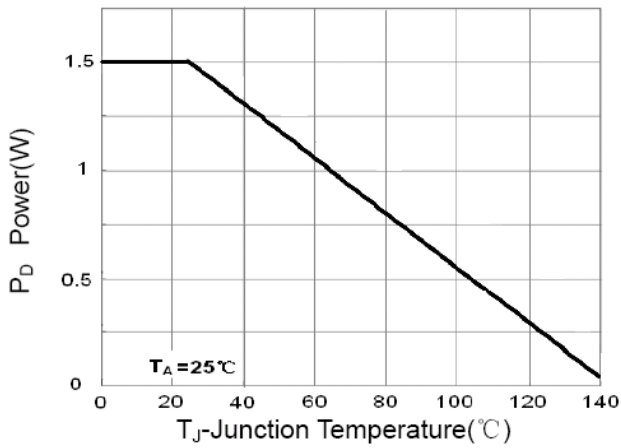


Figure 3 Power Dissipation

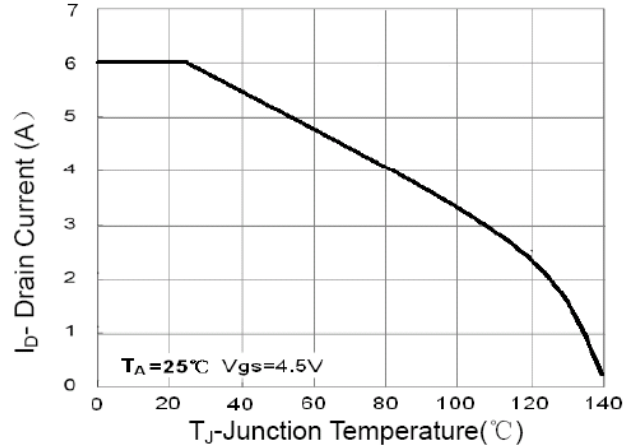


Figure 4 Drain Current

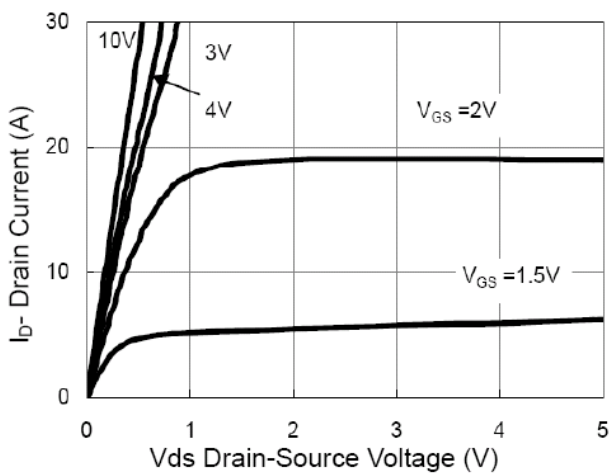


Figure 5 Output CHARACTERISTICS

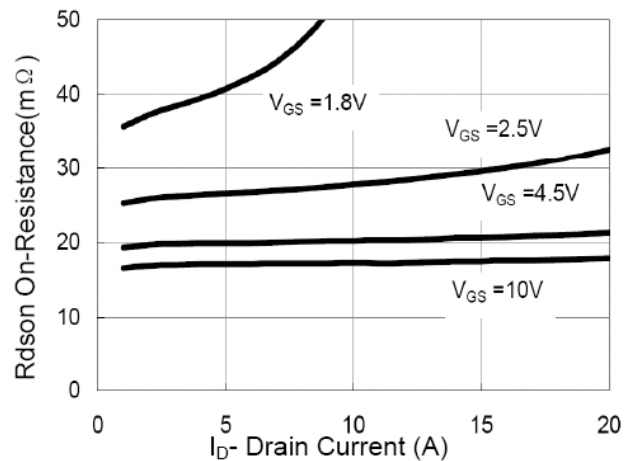


Figure 6 Drain-Source On-Resistance

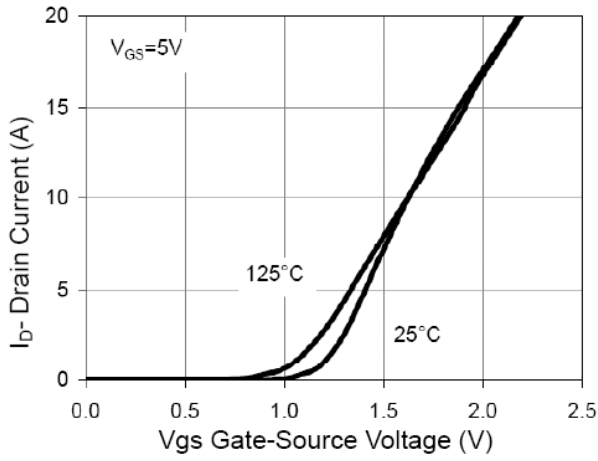


Figure 7 Transfer Characteristics

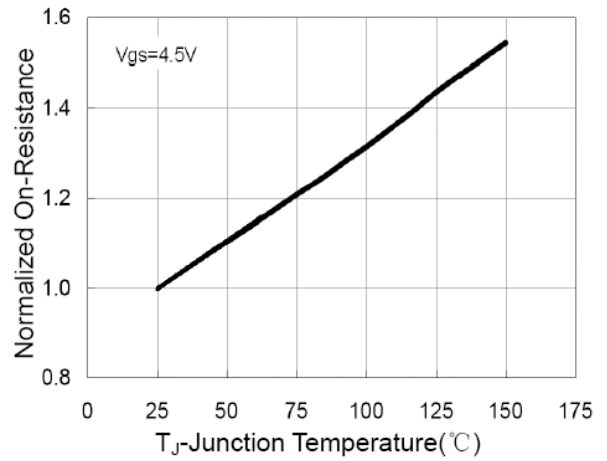


Figure 8 Drain-Source On-Resistance

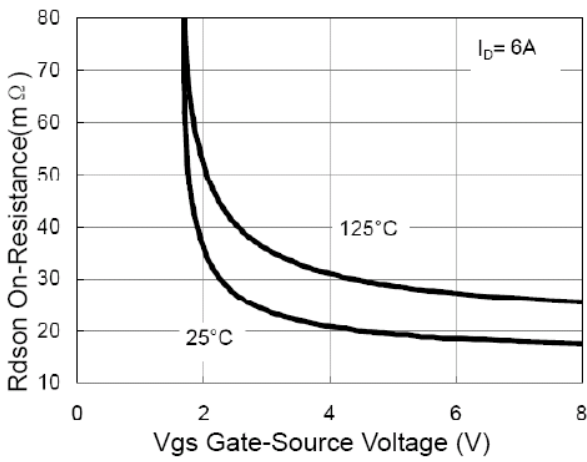


Figure 9  $R_{DS(on)}$  vs  $V_{GS}$

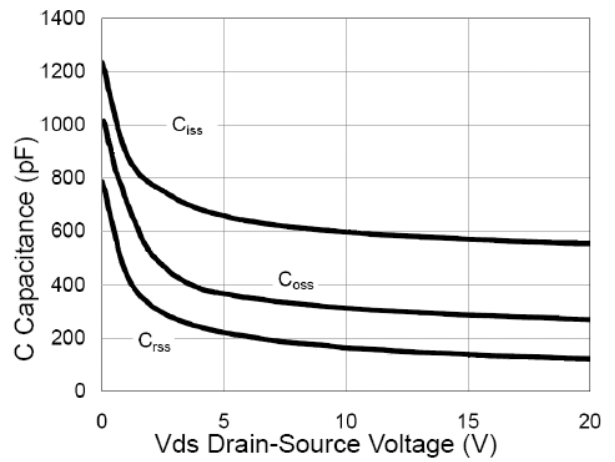


Figure 10 Capacitance vs  $V_{DS}$

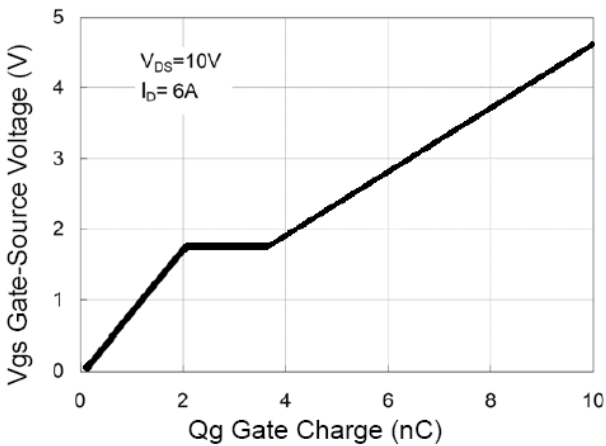


Figure 11 Gate Charge

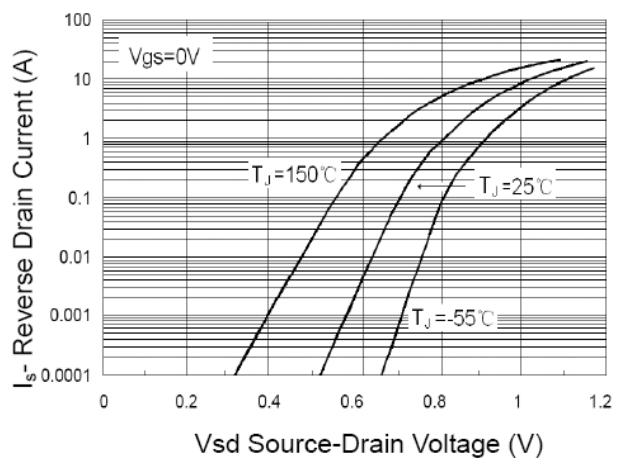


Figure 12 Source-Drain Diode Forward

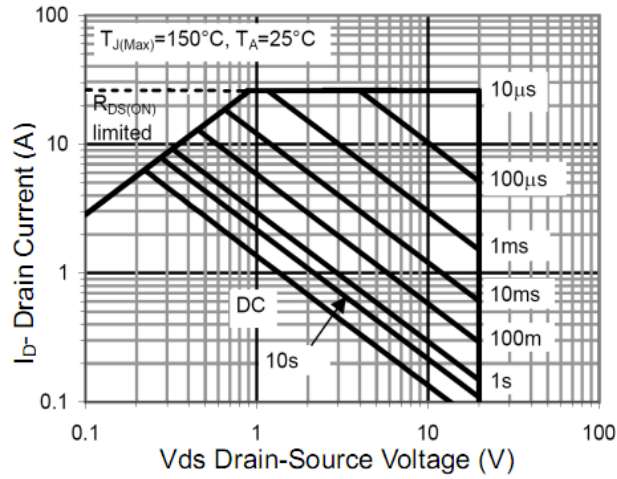


Figure 13 Safe Operation Area

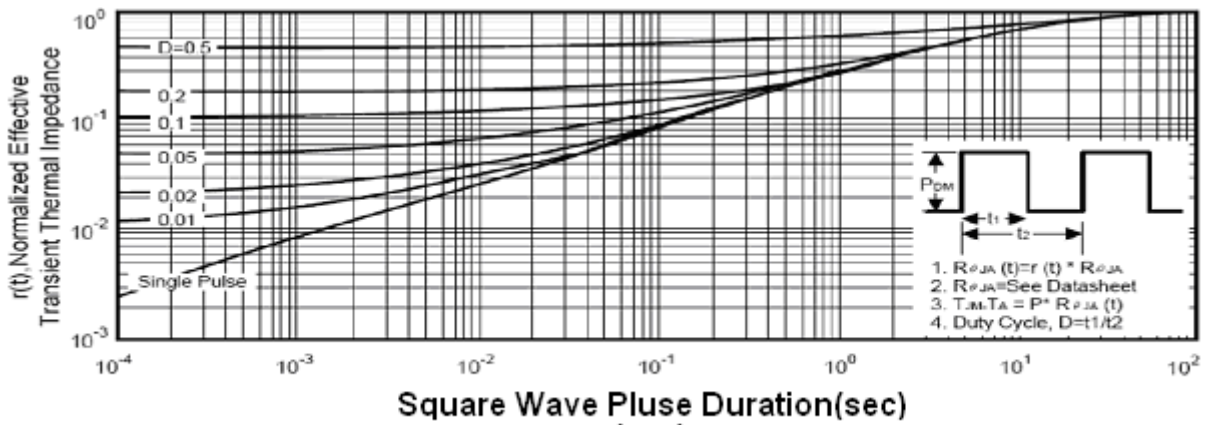
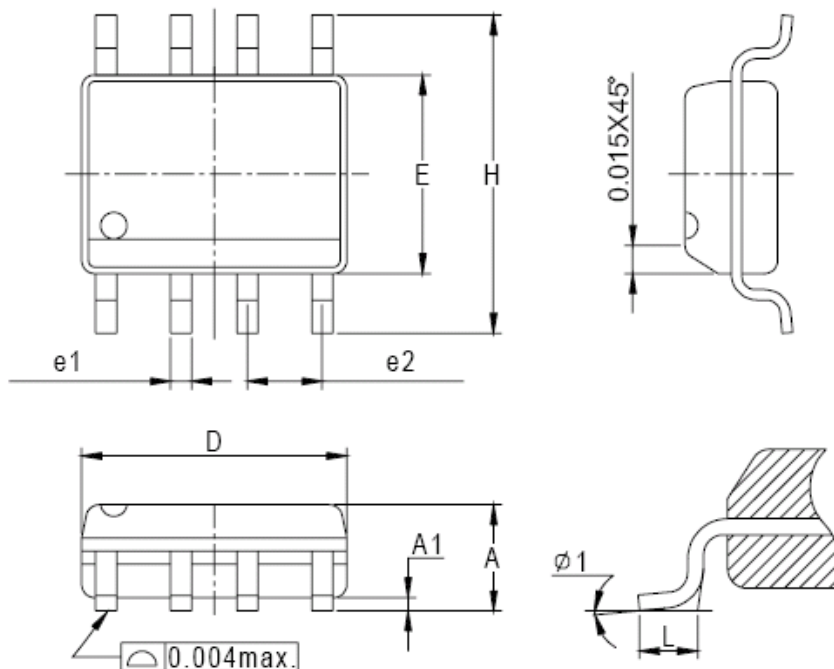


Figure 14: Normalized Maximum Transient Thermal Impedance

**Packaging Information**

SOP-8 pin



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
φ 1	8°		8°	

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