SHANGHAI SINO-IC MICROELECTRONICS CO., LTD.

Mar 2015

SED2145

P-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Advanced trench technology to provide excellent RDS(ON), low gate charge and low operation voltage. This device is suitable for using as a load switch or in PWM applications.

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

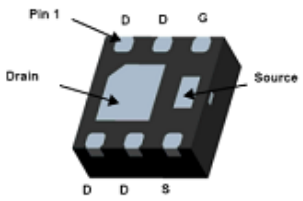
Features

For a single MOSFET

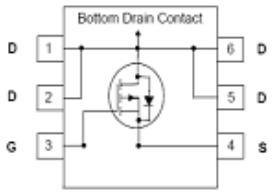
- V_{DS} = -12V
- $R_{DS(ON)}$ = 18.9mΩ @ V_{GS}=-4.5 @I_{DS}=-10A
- $R_{DS(ON)}$ = 26mΩ @ V_{GS}=-2.5 @I_{DS}=-8.9A

Pin configurations

See Diagram below



DFN2x2-6L Pin Assignment



Schematic diagram

Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	±8	V
Drain Current	Continuous	I_D	-12	A
	Pulsed		-28	
Total Power Dissipation	@TA=25℃	P_D	2.4	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

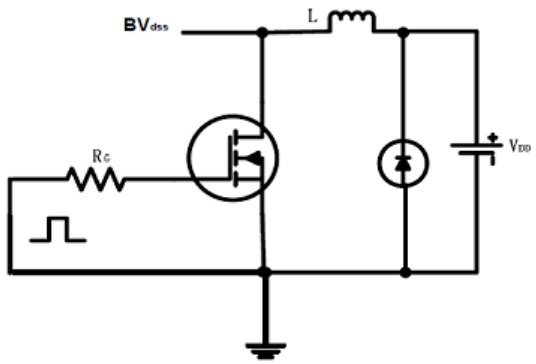
Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	-12			V
I_{DSS}	Drain to Source Leakage Current	V_{DS}= -12V, V_{GS}=0V			-1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}= 8V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	-0.4		-1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance [2]	V_{GS}=-4.5V, I_D=-10A	-	18.9	-	mΩ
		V_{GS}=-2.5V, I_D=-8.9A		26		
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-6V, f=1MHz	-	2138	-	pF
C_{oss}	Output Capacitance		-	685	-	pF
C_{rss}	Reverse Transfer Capacitance		-	650	-	pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge [2]	V_{GS}=-4.5V, V_{DS}=-6V, I_D=-10A	-	21	-	nC
Q_{gs}	Gate Source Charge		-	2.5	-	nC
Q_{gd}	Gate Drain Charge		-	6	-	nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=-4.5V, V_{DS}=-6V, R_{GEN}=6Ω, I_D=-10A		30		ns
$t_{d(off)}$	Turn-Off Delay Time			97		ns
$t_{d(r)}$	Turn-On Rise Time			48		ns
$t_{d(f)}$	Turn-Off Fall Time			65		ns

Thermal Resistance

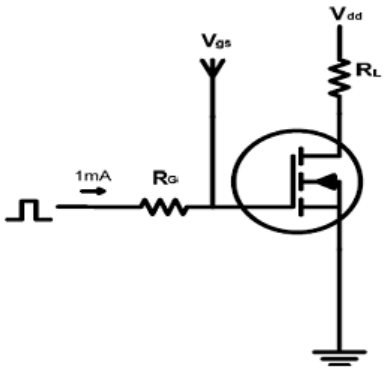
Symbol	**Parameter**	**Typ**	**Max**	**Units**
$R_{\theta JC}$	Junction to Case	6.9	8	℃/W
$R_{\theta JA}$	Junction to Ambient (t≦10s)	52	62.5	℃/W

Test Circuits and Waveform

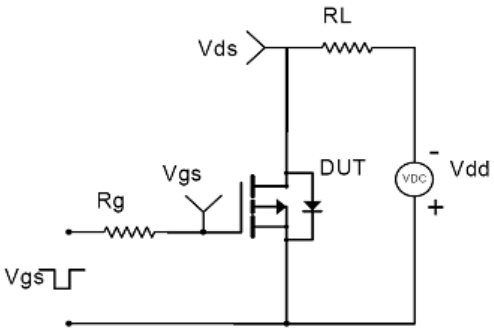
EAS test circuits:



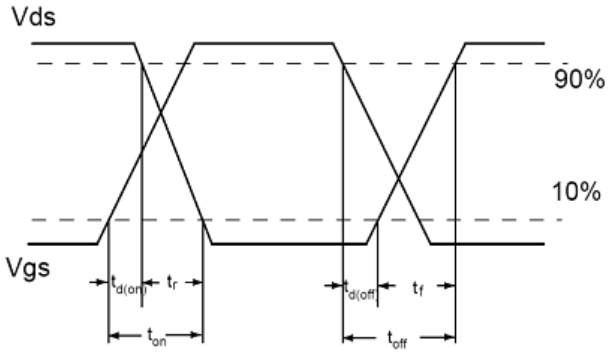
Gate charge test circuit:



Switch time test circuit:

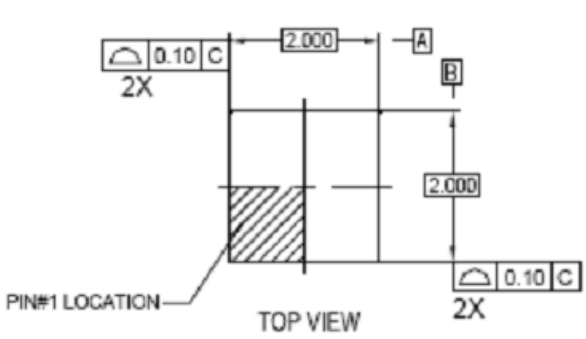


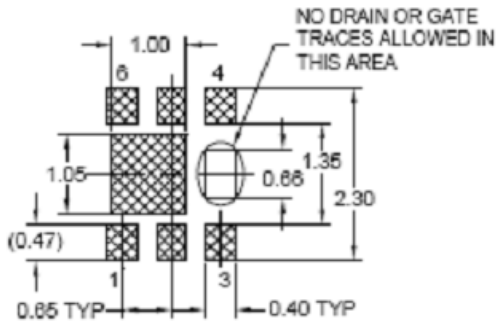
Switch Waveforms:



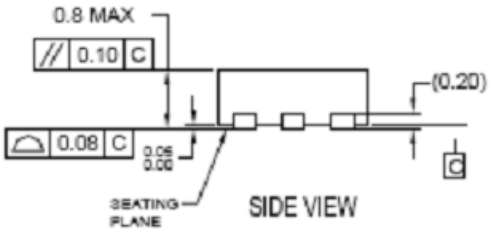
Package Outline Dimension

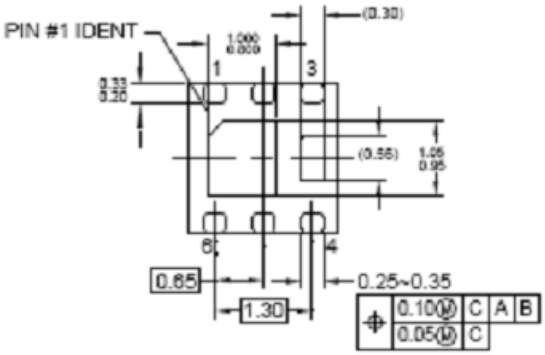
DFN2 × 2-6L

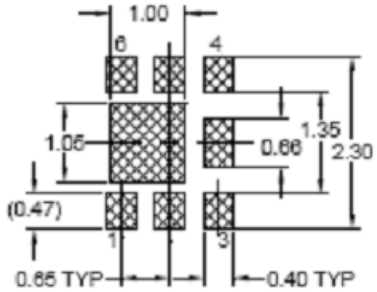




RECOMMENDED LAND PATTERN OPT 1







RECOMMENDED LAND PATTERN OPT 2

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