SHANGHAI SINO-IC
MICROELECTRONICS CO., LTD.

SE40300GTS

N-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

Features

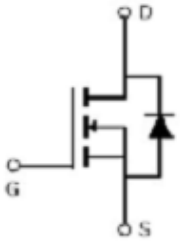
For a single MOSFET

- V_{DS} = 40V
- $R_{DS(ON)}$ = 1.7mΩ @ V_{GS}=10V

Pin configurations

See Diagram below

TO-247S



Absolute Maximum Ratings

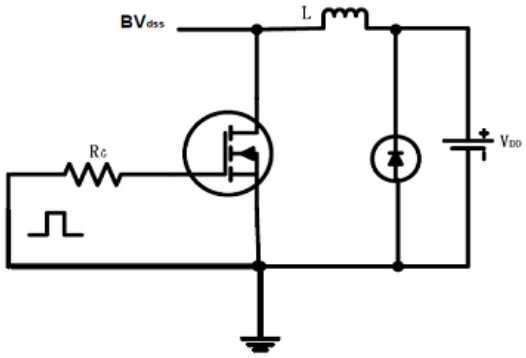
Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	288	A
	Pulsed		780	
Single Pulse Avalanche Energy		E_{AS}	1080	mJ
Peak Diode Recovery		dv/dt	5	V/ns
Total Power Dissipation	@TA=25℃	P_D	250	W
Operating Junction Temperature Range		T_J	-55 to 150	℃

Electrical Characteristics (TJ=25℃ unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	40			V
I_{DSS}	Drain to Source Leakage Current	V_{DS}= 120V, V_{GS}=0V			10	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=20 V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1.0	2.0	3.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance [2]	V_{GS}=10V, I_D=20A		1.7	2.0	mΩ
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		7500		pF
C_{oss}	Output Capacitance			1420		pF
C_{rss}	Reverse Transfer Capacitance			530		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge [2]	V_{GS}=10V, V_{DS}=80V, I_D=20A		96		nC
Q_{gs}	Gate Source Charge			22		nC
Q_{gd}	Gate Drain Charge			10		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=80V, R_{GEN}=3.9Ω I_D=20A		24		ns
$t_{d(off)}$	Turn-Off Delay Time			72		ns
$t_{d(r)}$	Turn-On Rise Time			26		ns
$t_{d(f)}$	Turn-Off Fall Time			31		ns

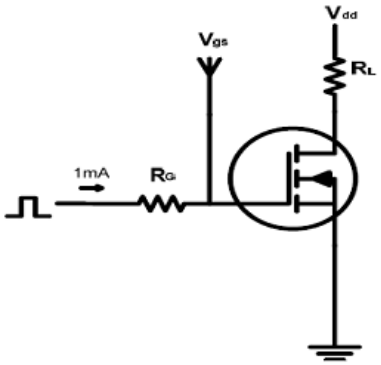
Thermal Resistance			
Symbol	**Parameter**	**TO-220**	**Units**
$R_{\theta JC}$	Junction to Case	0.6	℃/W
$R_{\theta JA}$	Junction to Ambient (t≦10s)	60	℃/W

Test Circuits and Waveform

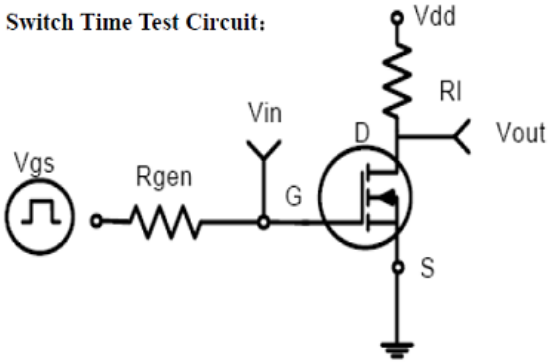
EAS test circuits:



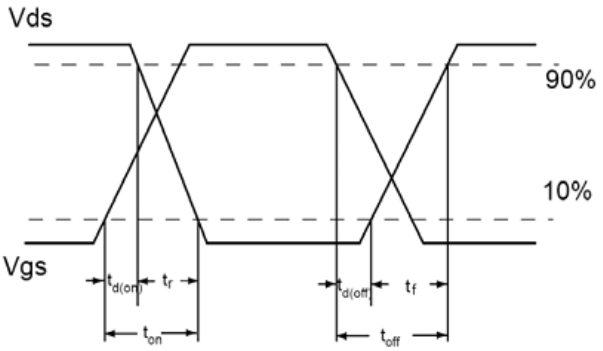
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Typical Characteristics

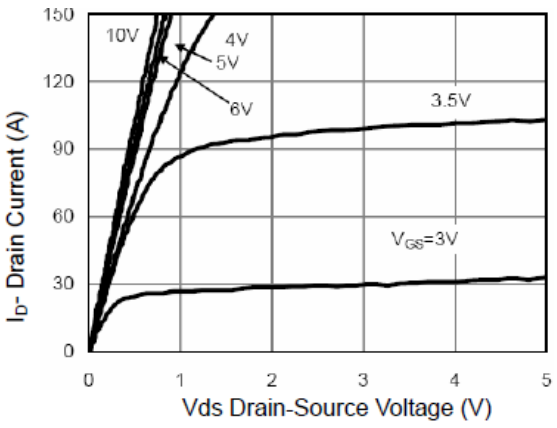


Figure 1 Output Characteristics

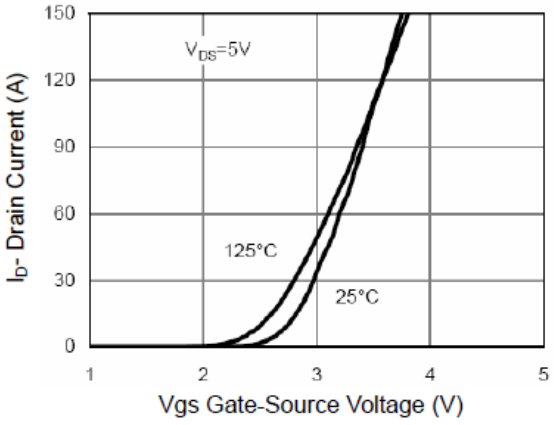


Figure 2 Transfer Characteristics

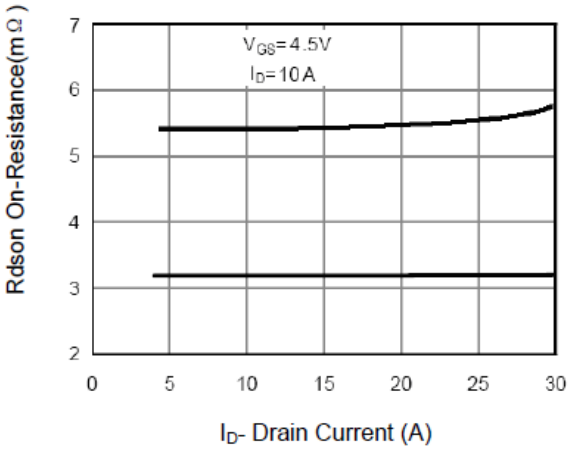


Figure 3 Rdson- Drain Current

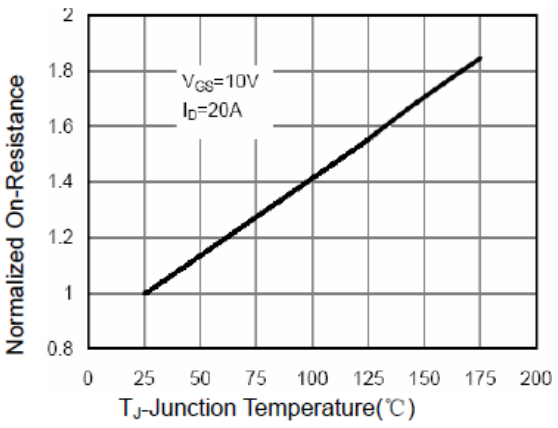


Figure 4 Rdson-JunctionTemperature

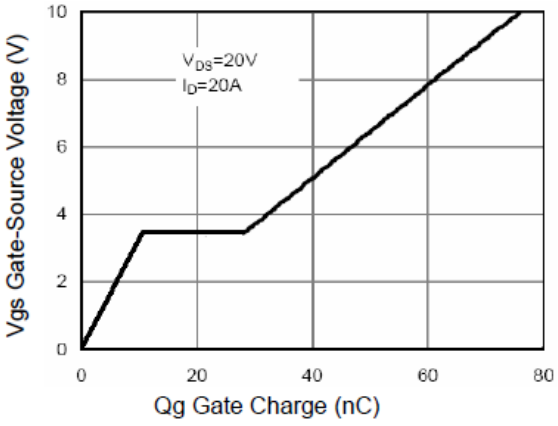


Figure 5 Gate Charge

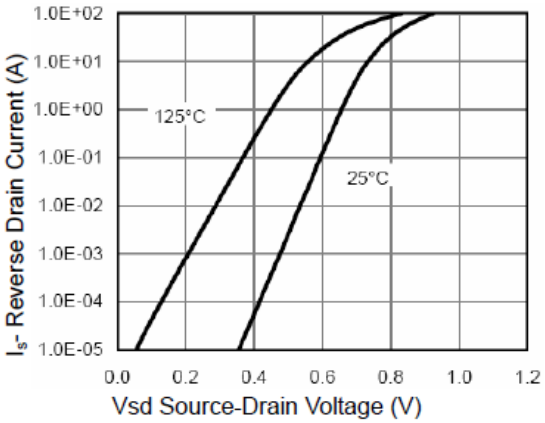


Figure 6 Source- Drain Diode Forward

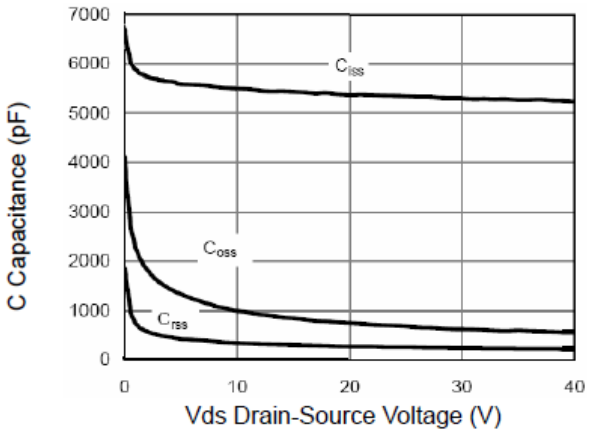


Figure 7 Capacitance vs Vds

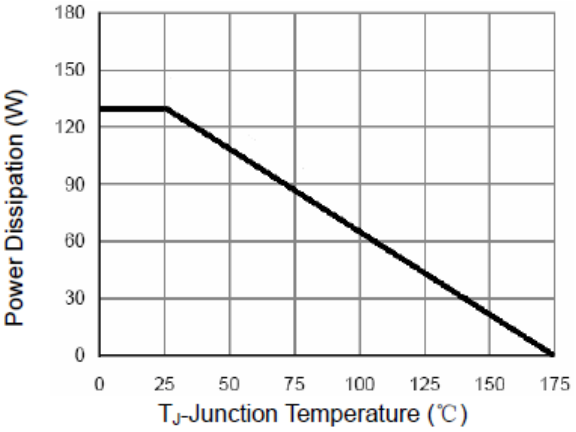


Figure 9 Power De-rating

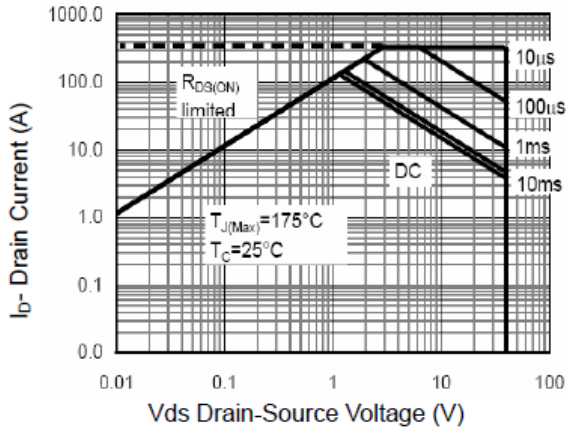


Figure 8 Safe Operation Area

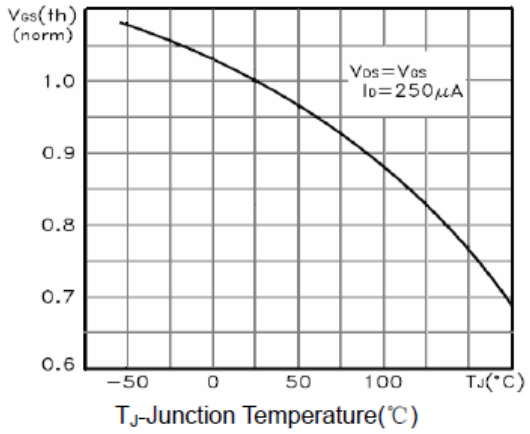


Figure 10 $V_{GS(th)}$ vs Junction Temperature

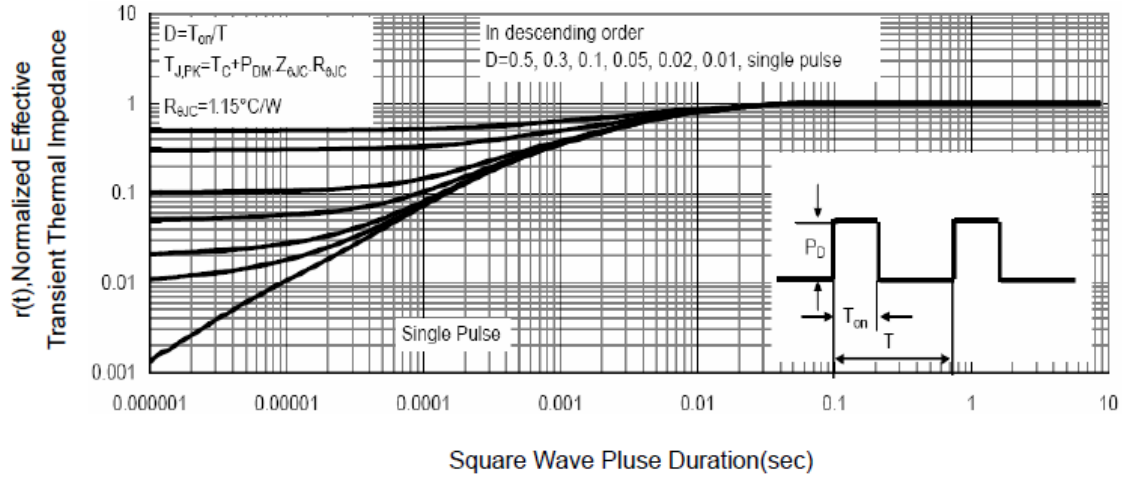
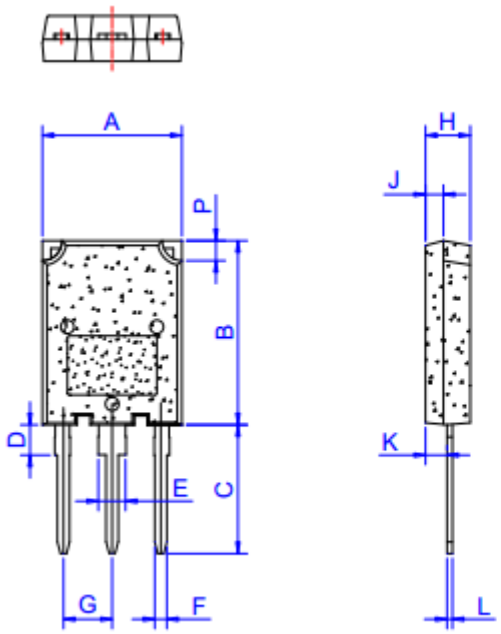


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Outline Dimension

TO-247S



TO-247S

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.1		16.1	0.594		0.634
B	19.8		20.8	0.78		0.819
C	13.8		14.8	0.543		0.583
D	3.00		4.00	0.118		0.157
E	2.75		3.35	0.108		0.132
F	1.30		1.50	0.051		0.059
G	5.10		5.80	0.201		0.228
H	4.50		5.50	0.177		0.217
J	1.45		2.15	0.057		0.085
K	1.90		2.80	0.075		0.110
L	0.55		0.80	0.022		0.031
P	2.00		2.40	0.079		0.094

SHANGHAI SINO-IC MICROELECTRONICS CO., LTD

Add: Building 3, Room 3401-03, No.200 Zhangheng Road,
ZhangJiang Hi-Tech Park, Pudong, Shanghai 201203, China
Phone: +86-21-33932402 33932403
33932405 33933508 33933608
Fax: +86-21-33932401
Email: webmaster@sino-ic.com
Website: http://www.sino-ic.com