

SE100P60
P-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Advanced trench technology to provide excellent RDS(ON), low gate charge and low operation voltage. This device is suitable for using as a load switch or in PWM applications.

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

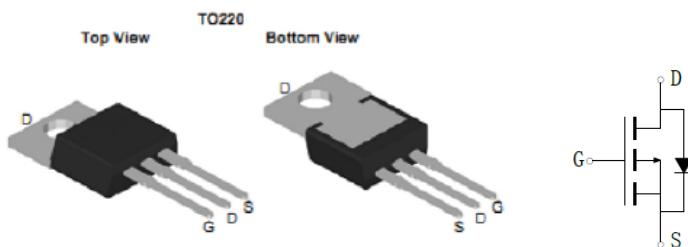
Features

For a single MOSFET

- $V_{DS} = -100V$
- $R_{DS(ON)} = 18m\Omega @ V_{GS}=-10V$

Pin configurations

See Diagram below



Absolute Maximum Ratings

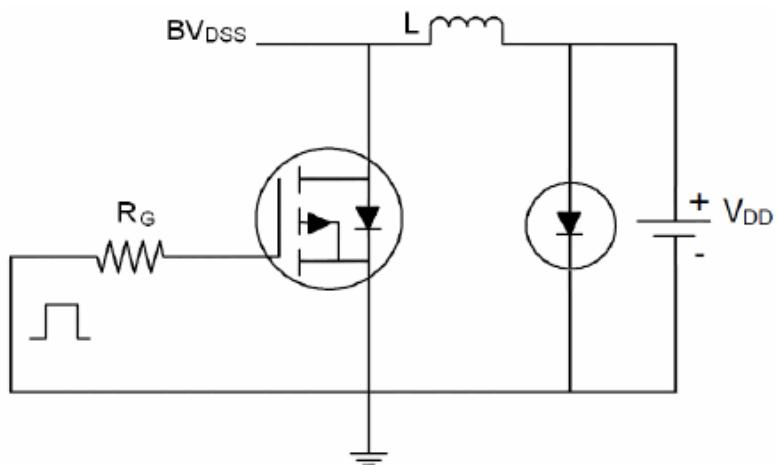
Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 25	V
Drain Current	Continuous	-60	A
	Pulsed	-240	
Total Power Dissipation @ $T_A=25^\circ C$	P_D	188	W
Operating Junction Temperature Range	T_J	-55 to 150	$^\circ C$

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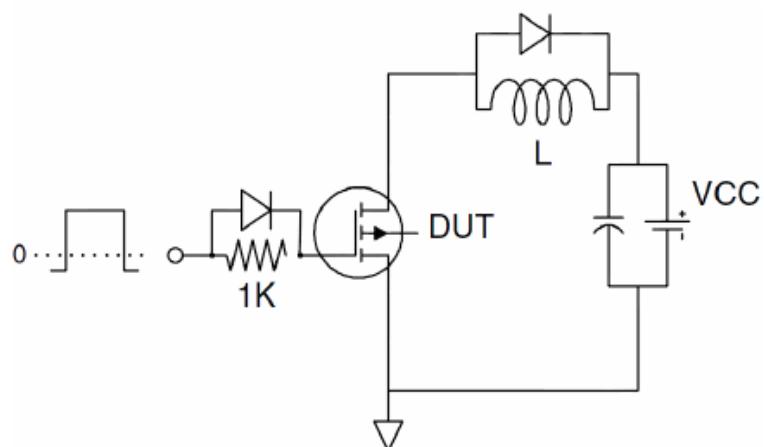
Electrical Characteristics (TJ=25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250µA, V _{GS} =0 V	-100			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = -100V, V _{GS} =0V			-1	µA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = 25V			100	µA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =-250µA	-2		-4	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-60A	-	18	25	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-50V, I _D =-10A	5			S
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-50V, f=1MHz		4200		pF
C _{oss}	Output Capacitance			615		pF
C _{rss}	Reverse Transfer Capacitance			380		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =-10V, V _{DS} =-80V, I _D =-60A		90		nC
Q _{gs}	Gate Source Charge			15		nC
Q _{gd}	Gate Drain Charge			35		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =-10V, V _{DS} =-50V, R _{GEN} =6Ω,		27		ns
t _{d(off)}	Turn-Off Delay Time			145		ns
t _{d(r)}	Turn-On Rise Time			83		ns
t _{d(f)}	Turn-Off Fall Time			40		ns
Thermal Resistance						
Symbol	Parameter		Typ	Max	Units	
R _{θJC}	Junction to Case		-	1.25		°C/W

Test Circuits and Waveform

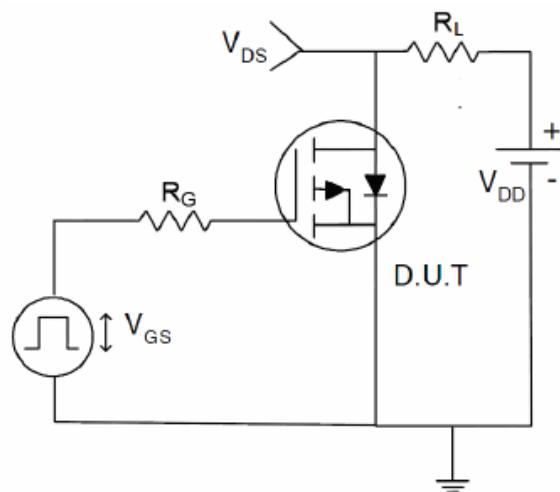
1) E_{AS} Test Circuit



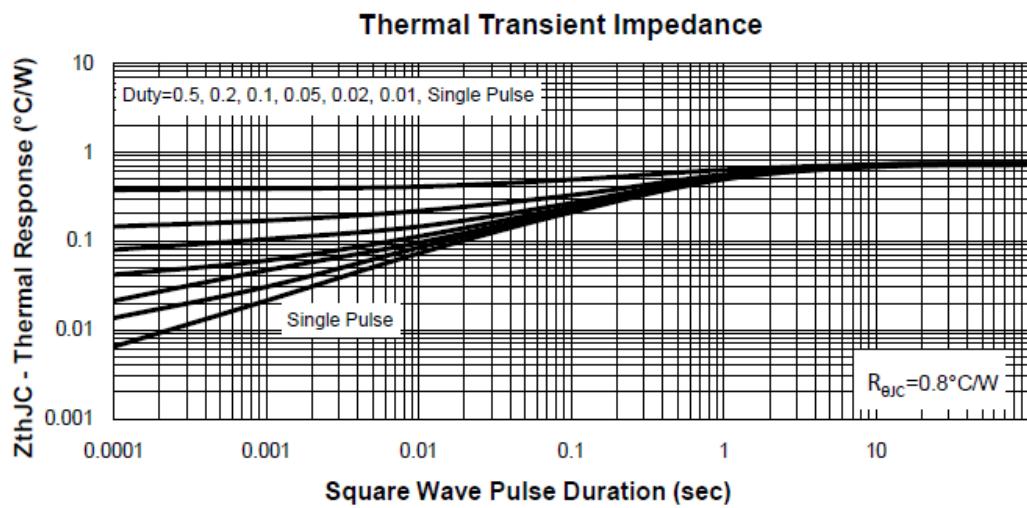
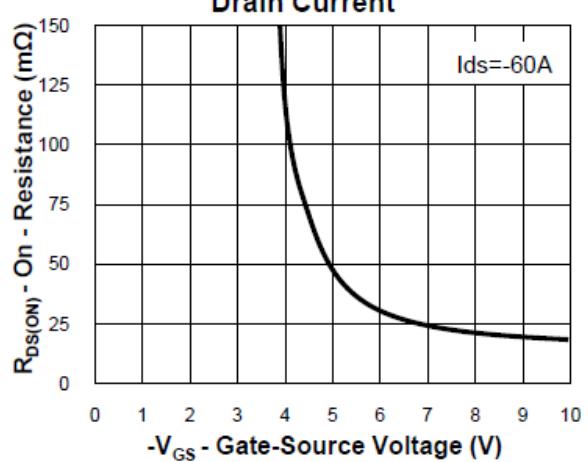
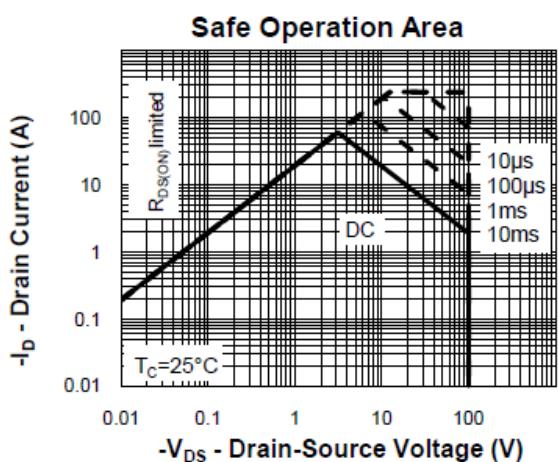
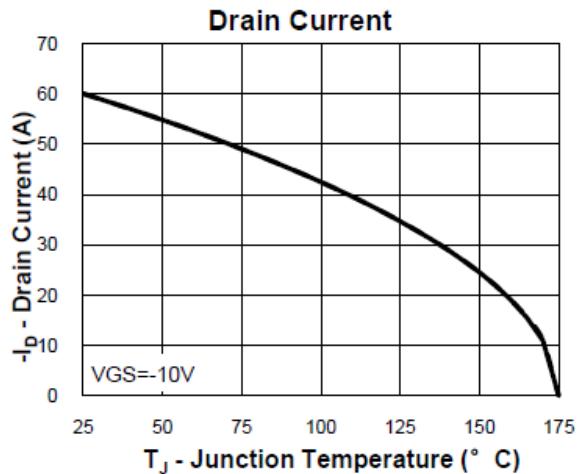
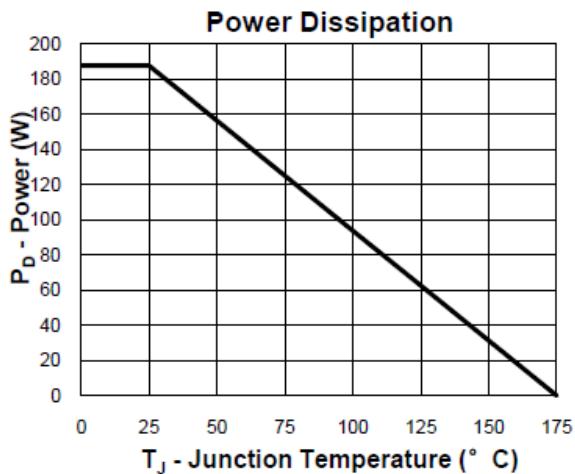
2) Gate Charge Test Circuit



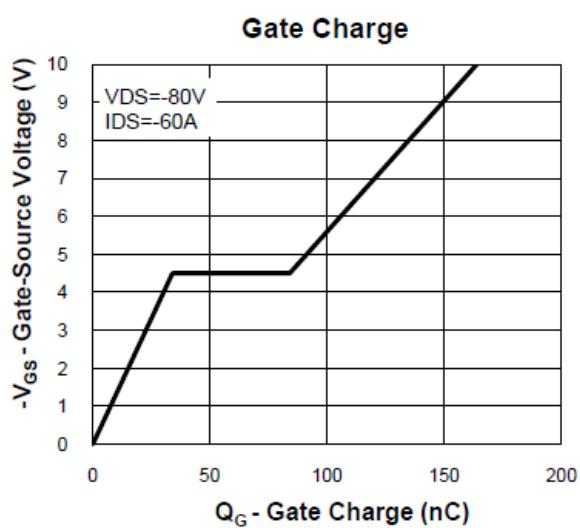
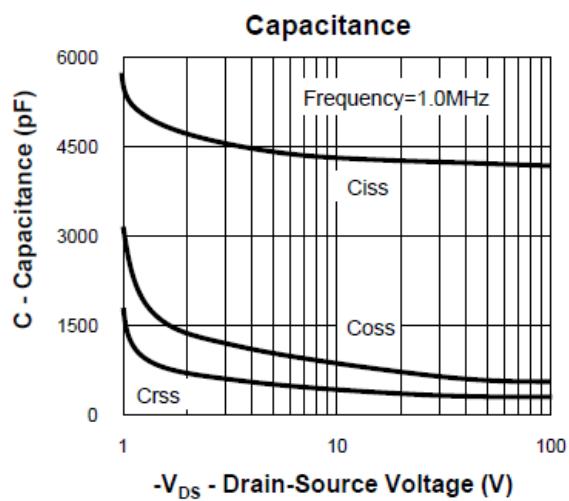
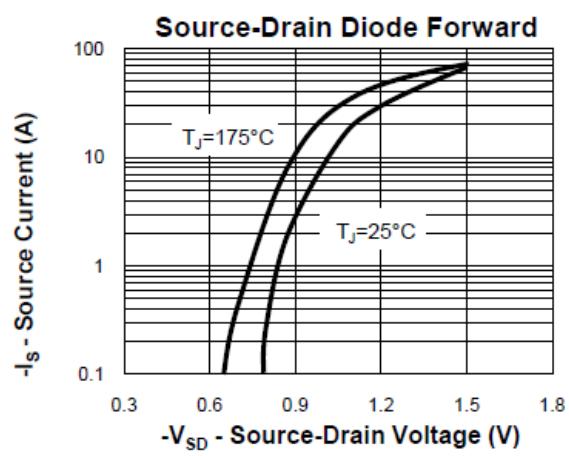
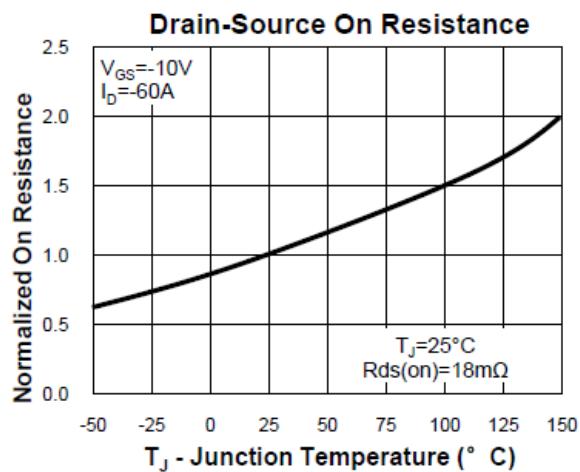
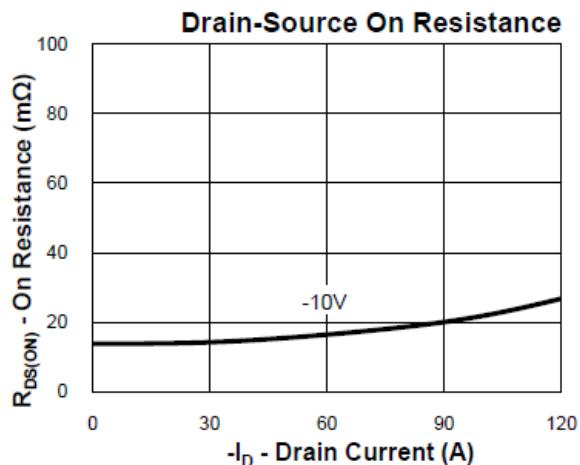
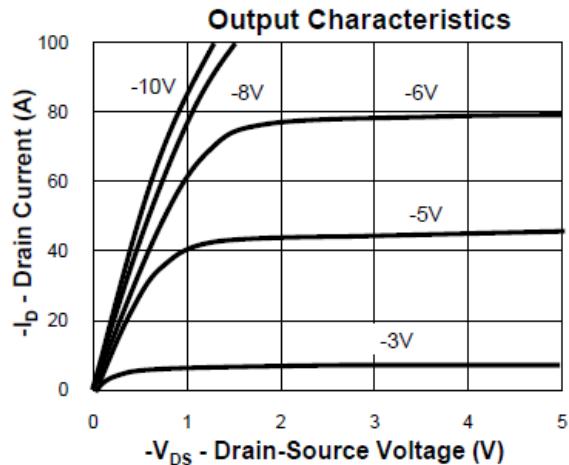
3) Switch Time Test Circuit



Typical Characteristics

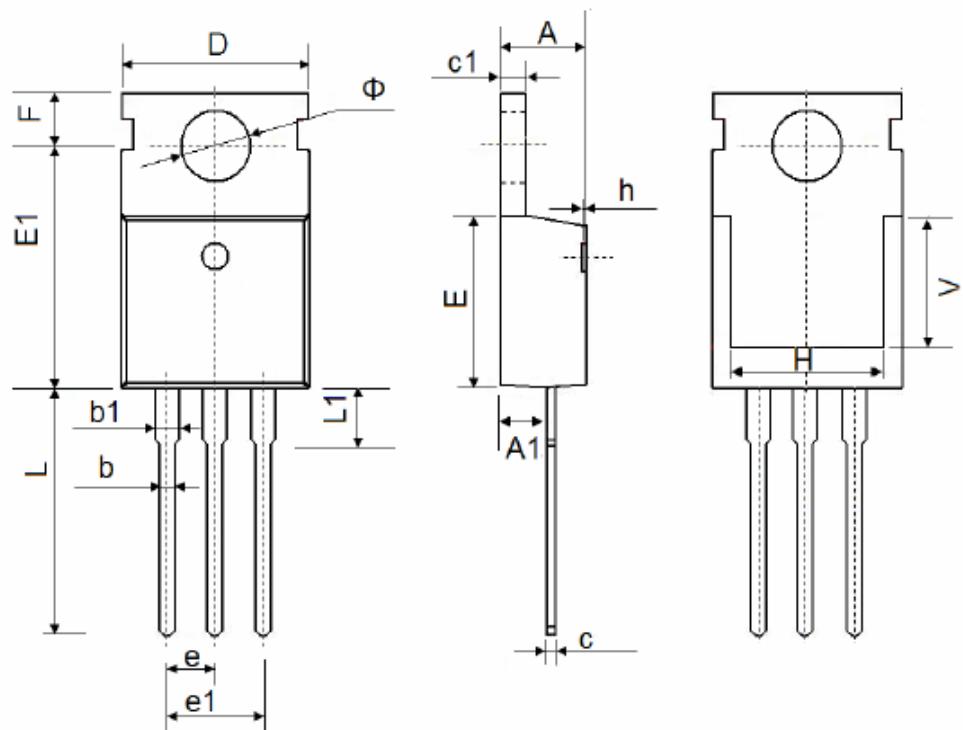


Typical Characteristics



Package Outline Dimension

TO-220



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150

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