10-LED Driver and GPIO Controller

FEATURES

- 10-channel LED constant-current driver, each channel can be used for GPIO
- OUT0~OUT5 support 2 intelligent breathing mode: BLINK and SMART-FADE, breathing time is adjustable
- Support 256 steps linearity dimming, I_{MAX} is 37mA
- Support GPIO input/output mode
- GPIO input mode, internal 8μs debounce
- Standard I²C interface
- I²C interface and GPIO can operate at 1.8V
- Support shutdown function, low level effective
- Simple Voltage Range VCC: 2.5V~5.5V
- TQFN 3mmX3mmX0.75mm-20L Package

APPLICATIONS

Mobile Phones/ Portable Media Player

Home Appliances

GENERAL DESCRIPTION

AW9110B is a 10-channel LED controller with I²C interface. Each channel can be used for GPIO. LED dimming combined with extended GPIO function, which can give full play to the application value of single chip.

AW9110B configures the current level to realize 256 steps linear dimming with I²C interface. The default I_{MAX} current is 37mA. AW9110B strengthens the dropout performance of low 6 channel LED driver and only 60mV current source voltage drop can provide 20mA LED current that can make it more suitable for the driver of LCD backlight.

When OUTx(x=0~9) works in a GPIO input mode, AW9110B detected input state to occur interrupt with internal 8μs debounce.

AW9110B supports two intelligent breathing modes: BLINK mode and SMART-FADE mode. BLINK mode allows LED automatic to flash periodically according the setting time parameter. OUT0~OUT5 support intelligent breathing mode.

AW9110B is available in TQFN3X3-20L package. The operating voltage range is 2.5V~5.5V.

TYPICAL APPLICATION CIRCUIT

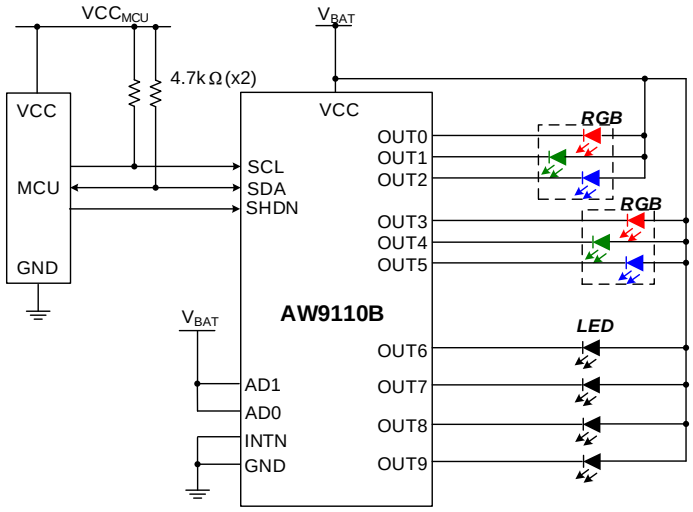

Figure 1 AW9110B Typical Application Circuit

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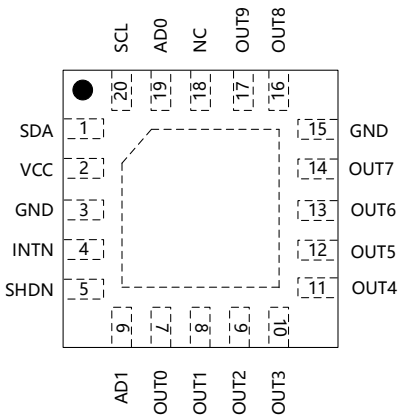
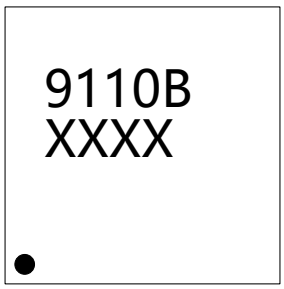
1 PIN CONFIGURATION AND TOP MARK

AW9110B TOP VIEW



AW9110B MARKING



9110B-AW9110BTQR
XXXX-Manufactory Trace No

2 PIN DEFINITION

NO	NAME	DESCRIPTION
1	SDA	Serial Data I/O for I^{2}C Interface
2	VCC	Power Supply
3	GND	Power Ground
4	INTN	Interrupt Output, Low Active
5	SHDN	Shutdown Pin, Low Active
6	AD1	I^{2}C Address Pin
7	OUT0	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
8	OUT1	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
9	OUT2	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
10	OUT3	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
11	OUT4	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
12	OUT5	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
13	OUT6	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
14	OUT7	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
15	GND	Power Ground
16	OUT8	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
17	OUT9	Defaults to GPIO, LED driver configurable. The default state after power on according to the level of AD1/AD0 PIN
18	NC	NC
19	AD0	I^{2}C Address Pin
20	SCL	Serial Clock Input for I^{2}C Interface

3 FUNCTIONAL BLOCK DIAGRAM

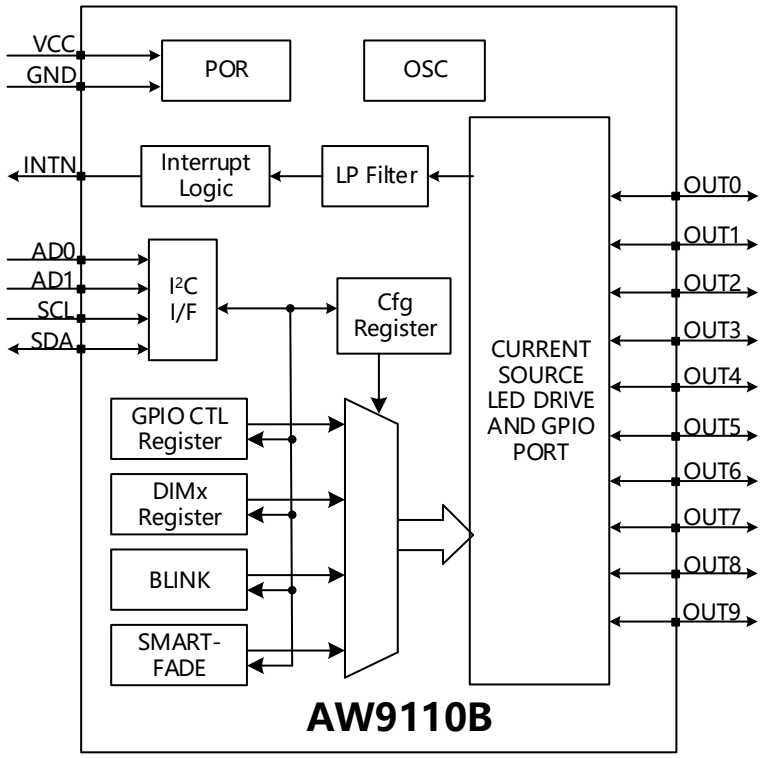
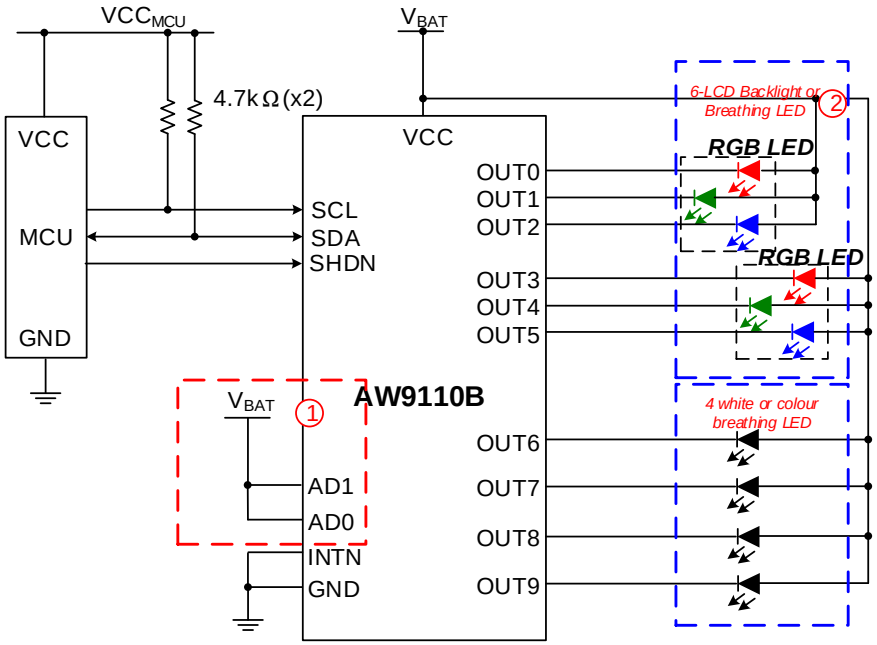


Figure 2 FUNCTIONAL BLOCK DIAGRAM

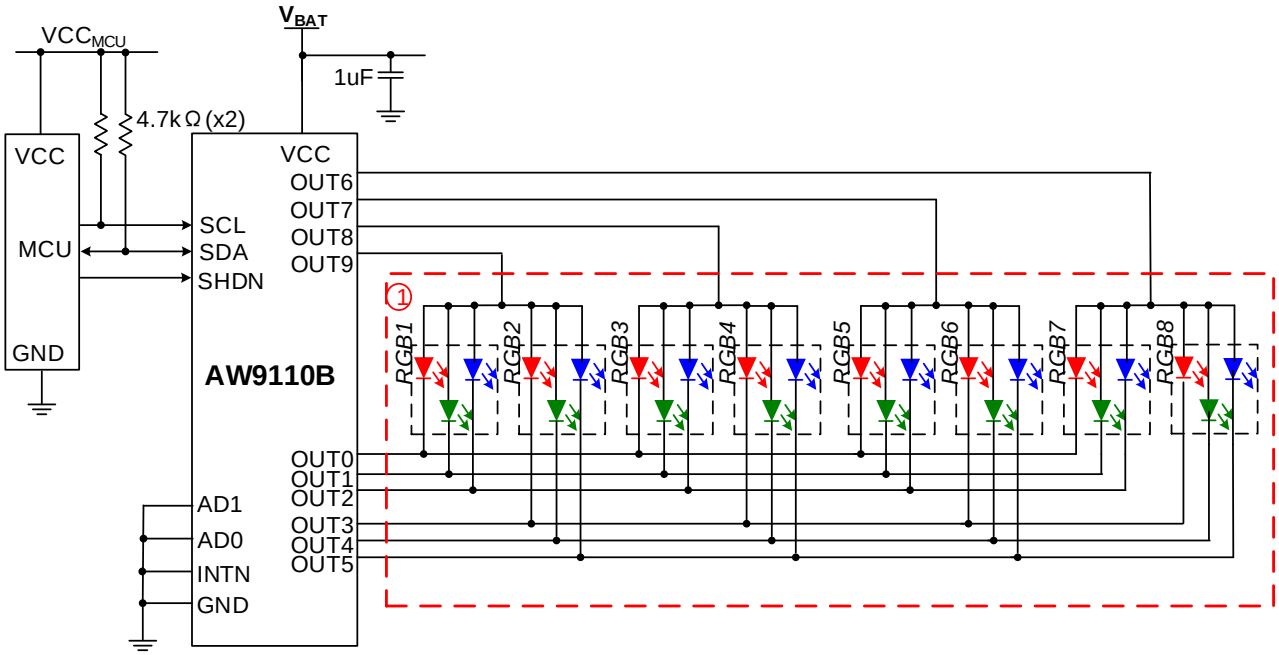
4 TYPICAL APPLICATION CIRCUITS

4.1 Using single chip to realize 10-LED breathing or 6 LCD backlight control



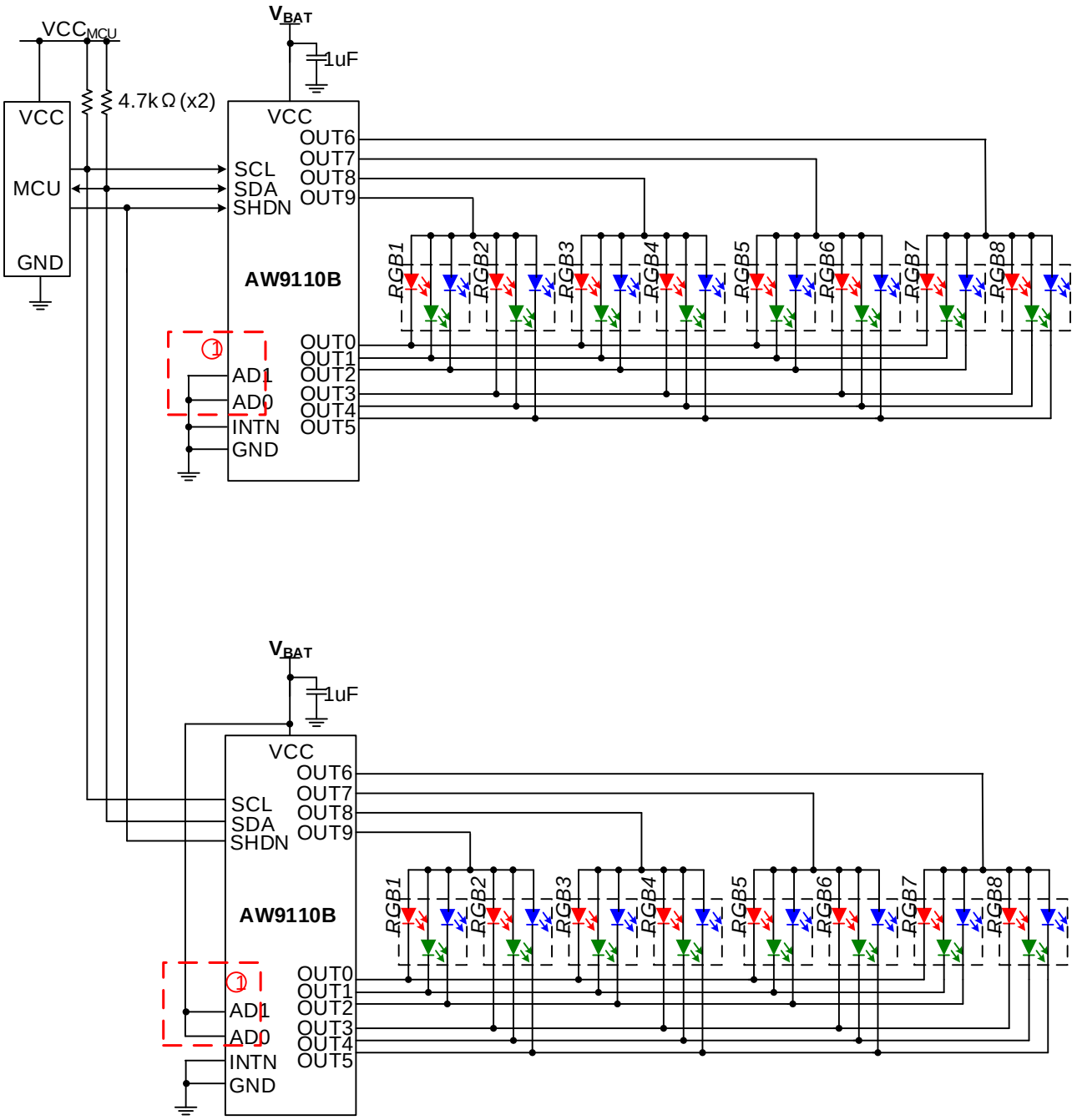
1. When the anode of LED is connected to VBAT, AD1/AD0 of the chip should be connected to VBAT to ensure the default electricity state of GPIO is high or high resistance and the LED will be off. The default electricity state of GPIO is decided by AD1/AD0 level.
2. In AW9110B, the dropout performance of low 6-leds are strengthened, we suggest these leds can be used when driving LCD backlight.

4.2 Using single chip to realize 8-RGB control



1.When choosing this application, we must pay attention to the restrictions of light effect. If we need the led turn on at the same time and they are different color type, the led cathode cannot be connected to the same OUTx pin. Because the Vf of RGB is different; When we turn on RGB1 and RGB4 at the same time, RGB2 and RGB3 will be turned on. Because the anode and cathode of RGB1/2/3/4 are all on. So pay attention to the lighting effects when designing the hardware.

4.3 Using two chips to realize driving more LED

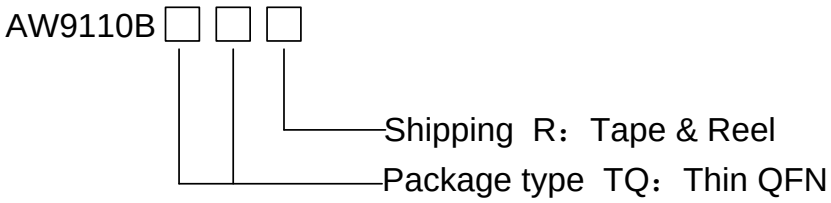


1. The AD configurations are different, so 2 AW9110B can share the same I²C bus.

2. When configuring the connection of AD1/AD0, the default electricity state of OUTx pin must be considered to avoid led on directly after AW9110B power on.

5 ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW9110BTQR	-40℃～85℃	3mm×3mm×0.75mm	AW9110B	MSL3	ROHS+HF	6000 units/ Tape and Reel



6 ABSOLUTE MAXIMUM RATINGS(NOTE 1)

Parameter	Range
Supply Voltage range VCC	-0.3V to 6 V
SCL,SDA,AD0,AD1,INTN,SHDN,OUT0-9 PINS voltage range	-0.3V to VCC
Max power dissipation (PDmax,package@ TA=25℃)	3.2 W
Package thermal resistance θ_{JA}	49℃/W
Maximum Junction temperature T_{Jmax}	125℃
Storage temperature range	-65℃ to 150℃
Lead temperature (Sodering 10 Seconds)	260℃
ESD(2)	
HBM(All Pins)	8000V
Latch-up	
Test Condition：JEDEC STANDARD NO.78A FEBURARY 2006	+IT：＋450mA -IT：-450mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

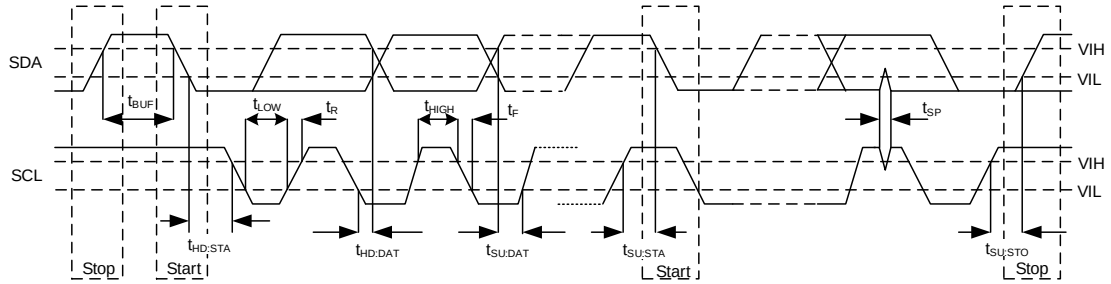
7 ELECTRICAL CHARACTERISTICS

V_{CC}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYPE	MAX	UNIT
Power supply voltage and current						
VCC	Input voltage	T_A=-40℃~85℃	2.4		5.5	V
V_{POR}	Power on reset voltage	T_A=-40℃~85℃		1.8	2.3	V
$I_{SHUTDOWN}$	Current in Shutdown mode	SHDN=0V,VIO=0V		0.1	2	μA
		SHDN=0V,VIO=1.8V		8.5		uA
$I_{STANDBY}$	Current in Standby mode	SHDN=1.8V,VIO=1.8V		80		μA
I_{ACTIVE}	Current in GPIO mode	GPMD_A=0x3F, GPMD_B=0x0F, GPIO_CFG_A=0x3F, GPIO_CFG_B=0x0F, AD1=AD2=1.8V		80		μA
		GPMD_A=0x3F, GPMD_B=0x0F, GPIO_CFG_A=0x00, GPIO_CFG_B=0x00, GPIO_OUTPUT_A=0x3F, GPIO_OUTPUT_B=0x0F,		13		uA
	Current in LED mode	GPMD_A=0x00, GPMD_B=0x00 ISEL=3, DIMx=0xFF		2.1		mA
Digital output						
V_{OH}	Output high level(OUT0~9)	VCC=2.5V,I_{SOURCE}=10mA		VCC-170		mV
		VCC=3.6V,I_{SOURCE}=20mA		VCC-250		mV
		VCC=5V,I_{SOURCE}=20mA		VCC-200		mV
V_{OL}	Output low level(OUT0~9)	VCC=2.5V,I_{SINK}=20mA		90		mV
		VCC=3.6V,I_{SINK}=20mA		70		mV
		VCC=5V,I_{SINK}=20mA		60		mV
	Output low level (SDA,INTN)	VCC=2.5V,I_{SINK}=6mA		150		mV
		VCC=3.6V,I_{SINK}=6mA		100		mV
		VCC=5V,I_{SINK}=6mA		75		mV
Digital input						
V_{IH}	Logic high level (SCL,SDA,SHDN,AD0,AD1,OUT0~9)		1.4			V
V_{IL}	Logic low level (SCL,SDA,SHDN,AD0,AD1,OUT0~9)				0.4	V
I_{IH},I_{IL}	Input current (SCL,SDA,AD0,AD1,OUT0~9)	V_I=VCC or GND	-0.2		+0.2	μA
$R_{\_SHDN}$	Resistant of shutdown pin			100k		Ω
C_I	Input capacitor (SCL,SDA,SHDN,AD0,AD1,OUT0~9)	V_I=VCC or GND		3		pF
t_{SP_SHDN}	Low burr pulse width	SHDN=VCC		10		μs
LED driver						
I_{LED}	Current Source	ISEL<1:0>=0,DIMx=FFH		37		mA
V_{drop1}	Low-6(OUT0~5)output voltage drop	I_{OUT}=21mA,ISEL<1:0>=01,DIMx=C0H		60	200	mV
V_{drop2}	High-4(OUT6~9)output voltage drop	I_{OUT}=21mA,ISEL<1:0>=01,DIMx=C0H		80	250	mV

8 I²C INTERFACE TIMING

Parameter	Symbol	MIN	TYP	MAX	UNIT
Interface Clock frequency	f_{SCL}			400	kHz
(Repeat-start) Start condition hold time	$t_{HD:STA}$	0.6			μS
Low level width of SCL	t_{LOW}	1.3			μS
High level width of SCL	t_{HIGH}	0.6			μS
(Repeat-start) Start condition setup time	$t_{SU:STA}$	0.6			μS
Data hold time	$t_{HD:DAT}$	0			μS
Data setup time	$t_{SU:DAT}$	0.1			μS
Rising time of SDA and SCL	t_R			0.3	μS
Falling time of SDA and SCL	t_F			0.3	μS
Stop condition setup time	$t_{SU:STO}$	0.6			μS
Time between start and stop condition	t_{BUF}	1.3			
Maximum width noise input filter out(burr)	t_{SP}	0		50	nS
Capacitor of the bus	C_b			400	pF



9 FUNCTIONAL DESCRIPTION

AW9110B is a 10 channel co-anode current breathing led driver. There is 256 current levels configurable via register CTL.ISEL. The maximum driver current I_{MAX} is 37mA.

The led drivers and GPIO functions can be switch with configuring register GPMD_A/GPMD_B. The default status of OUT0~OUT9 are used for GPIO function.

AW9110B supports two types of intelligent breathing modes: BLINK and SMART-FADE. In BLINK mode, AW9110B completes "fade-on" and "fade off" breathing periodically. In SMART-FADE mode, AW9110B runs "fade-on" and "fade off" independently with register GPIO_OUTPUT_A/GPIO_OUTPUT_B configuration.

9.1 SHUTDOWN AND RESET

AW9110B enters shutdown mode when SHDN is low level. When SHDN is pulled up from shutdown state, AW9110B enters standby mode and will be reset to the default state.

AW9110B offers two kinds of reset function：

- Power on reset -- 5ms after power on, the chip is reset to the default state.
- Hardware reset – keep SHDN low level over 20 μs, reset all internal circuit.
- Software reset -- write 00H to register 7FH, reset all internal circuit.

When AW9110B is reset, the default state of OUTx pin is GPIO.

9.2 LED DIMMING FUNCTION

AW9110B led driver uses co-anode current source. In default status, the maximum driving current I_{MAX} is 37mA.

After power on, OUTx(x=0~9) used for GPIO. AW9110B can switch OUTx to led driver mode with configuring GPMD_A and GPMD_B, shown in table 4&5.

AW9110B configures four dimming range by ISEL[1:0], 0~I_{MAX}(default), 0~(3/4)I_{MAX}, 0~(2/4)I_{MAX} or 0~(1/4)I_{MAX}, which means 256 steps dimming range: 0~37mA(default),0~27.75mA, 0~18.5mA or 0~9.25mA. ISEL[1:0] configuration is refer to table 3.

The dimming level of each channel is configured by DIMx(x=0~9) register. 8-bits DIMx can be configured to 256 levels, from 00H to FFH.

DIMx bit								Dimming level
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	1/255×I_{MAX}
0	0	0	0	0	0	1	0	2/255×I_{MAX}
……								……
1	1	1	1	1	1	0	1	253/255×I_{MAX}
1	1	1	1	1	1	1	0	254/255×I_{MAX}
1	1	1	1	1	1	1	1	255/255×I_{MAX}

9.3 GPIO FUNCTION

When AW9110B is used in GPIO, the direction of OUTx is configured by GPIO_CFG_A/GPIO_CFG_B (table14, 15). When OUTx is configured to output, write GPIO_OUTPUT_A or GPIO_OUTPUT_B register (table12, 13) driver high or low level.

The following table shows OUTx default output driving value after power on.

AD1	AD0	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
GND	GND	0	0	0	0	0	0	0	0	0	0
GND	VCC	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1	1	1	1
VCC	GND	Hi-Z	Hi-Z	0	0	0	0	0	0	0	0
VCC	VCC	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1	1	1	1

When OUTx is configured to input mode, the logic level of OUTx can be acquired with reading GPIO_INPUT_A or GPIO_INPUT_B register (table 10, 11). AW9110B can support 1.8V level logic.

OUT0~OUT3 are default to PUSH-PULL driver. OUT4~OUT9 are default to OPEN-DRAIN driver and can be configured as PUSH-PULL driver with GPOMD (table 3).

9.4 INTERRUPT FUNCTION

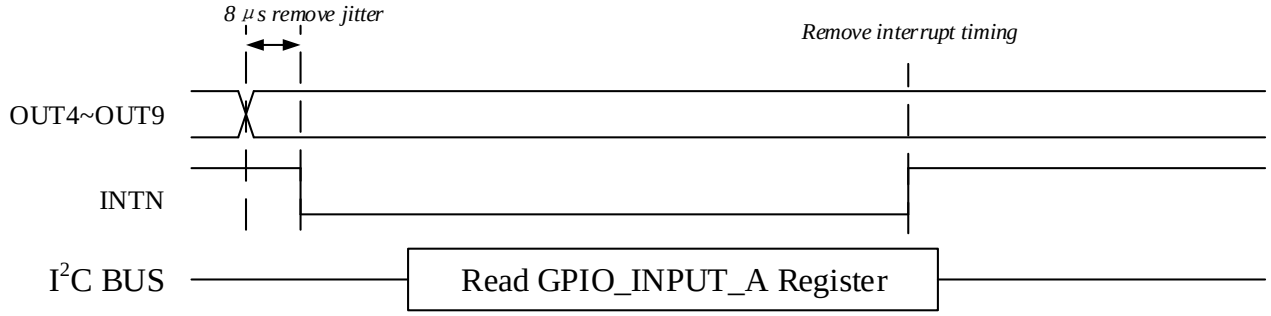
When OUTx is used for GPIO input, AW9110B detects the input state and produces interrupt request. Low level of INTN is active. INTN should be connected to pull-up resistor.

AW9110B has built-in debounce filter. The input state with 8μs low-pass filter will be steady. The interrupt request will not be produced when input state changes in 8μs.

In default status, GPIO interrupt is enabled (GPIO_INTN_A or GPIO_INTN_B setting, table16,17). Only enable interrupt function and configured to GPIO input mode, the interrupt will be produced on INTN.

Clear the interrupt by reading register GPIO_INPUT_A, GPIO_INPUT_B register. The interrupt of OUT4~OUT9 only be cleared by read GPIO_INPUT_A register. The interrupt of OUT0~OUT3 only be cleared by read GPIO_INPUT_B register. The interrupts status can't be cleared by the other group.

When AW9110B produces the interrupt request, the interrupt request will be reserved until reading GPIO_INPUT_A or GPIO_INPUT_B GPIO. The interrupt will be not cleared even if AW9110B switches to GPIO output, or disable GPIO interrupt function.



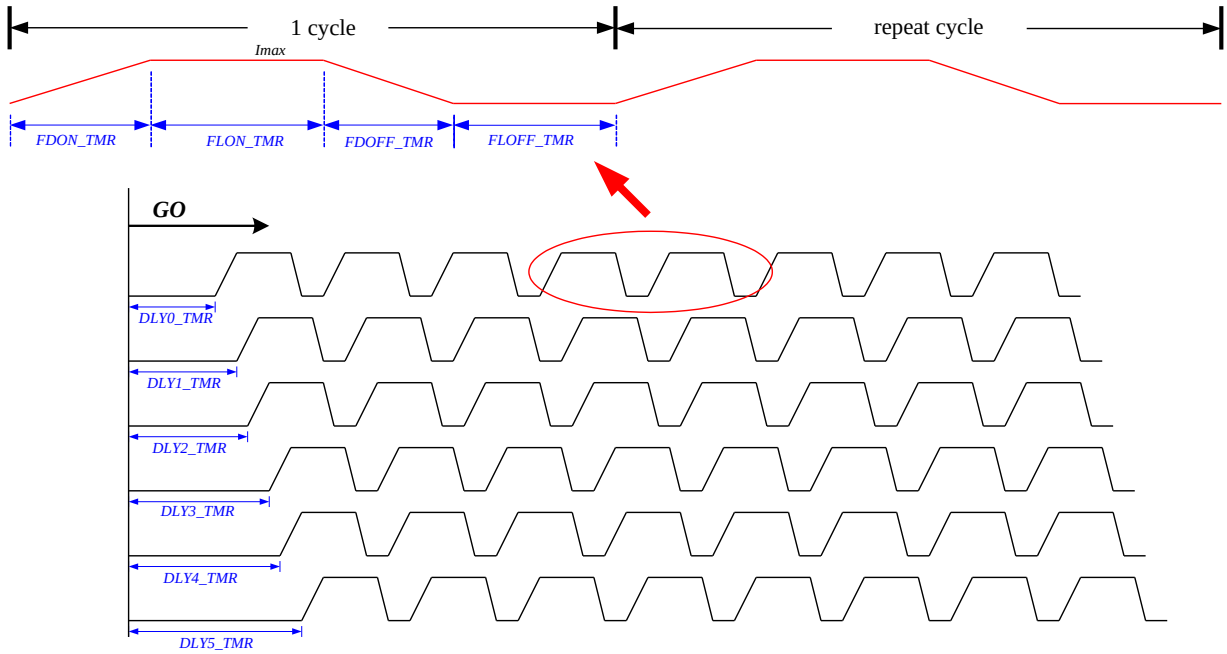
9.5 BLINK BREATHING MODE

OUT0~OUT5 of AW9110B supports BLINK breathing mode. In this mode, AW9110B will complete periodic blink effect automatically until exit the BLINK mode or close breathing function.

1. Configure OUTx to led driver mode. According to application situation, set register EN_BRE to enable breathing mode. Set GPIO_CFG_A/B (Table 14,15,pay attention to the switch of GPIO and breathing function) to open BLINK function.
2. Configure the timing parameter for BLINK breathing effects:
   - Blink delay——DLY_TMR(Table 9). When enable the BLINK mode, leds start blink after DLY_TMR time.
   - Fade-on process——FDON_TMR(Table 7). The time of fade-on effect has 6 kinds of choice (0ms~5040ms). The fade-on has 64 step dimming level and led turns on gradually from dark.
   - Full on process——FLON_TMR(Table 8). Full on state has 8 kinds of choice(0ms~20160ms). the led driving current of this period is decided by ISEL[1:0].
   - Fade-off process——FDOFF_TMR(Table 7). The time of fade-off effect has 6 kinds of choice (0ms~5040ms). The fade-off has 64 step dimming level and led turns off gradually from bright.
   - Full off process——FLOFF_TMR(Table 8). Full off state has 8 kinds of choice(0ms~20160ms). The led driving current is 0 in this period.
3. After setting blinking parameter, enable GO control bit and the led in BLINK mode starts blink periodically and automatically.

DLY_BRE of 6 channel, the parameter of BLINK mode, is independent configuration, which can make led be opened in turn. The fade-on/ fade-off/ full-on/ full-off parameter are same and can be modified at any time. The new configuration will be adjusted in the next breathing period.

AW9110B exits BLINK mode by disable GPIO_CFG_A/B corresponding bit or disable EN_BRE setting. The difference is AW9110B will exit BLINK immediately by disable EN_BRE, but we must wait it complete breathing period by another one.



9.6 SMART-FADE MODE

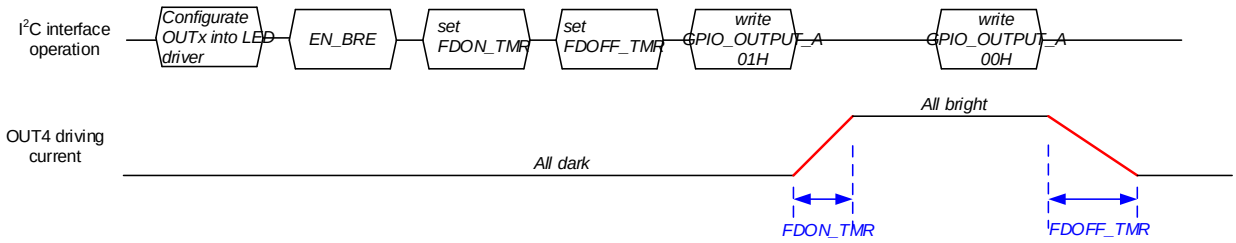
The SMART-FADE mode of AW9110B is semi-automatic breathing, which will simplify 64 steps fade-on and fade-off interface operation into 1bit writing operation: Writing ’1’ means fade-on process and remaining all bright; Writing ’0’ means fade-off process and remaining all dark.

Configure SMART-FADE mode:

1. Set EN_BRE register and open breathing mode according to the application;
2. Set GPIO_CFG_A/B (View table 14,15, pay attention to the switch of GPIO and breathing function), SMART-FADE mode is default;
3. Set GPIO_OUTPUT_A/B bit to complete fade-on or fade-off (View table 12,13, pay attention to the switch of GPIO and breathing function).

The time of fade-on and fade-out in SMART-FADE mode is controlled by FDON_TMR and FDOFF_TMR.

AW9110B exits SMART-FADE mode by disable EN_BRE.



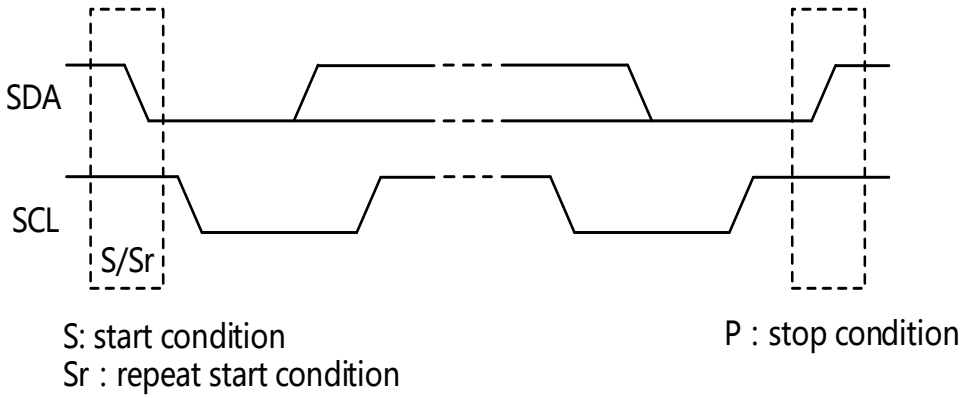
10 I²C INTERFACE

AW9110B supports the I²C serial bus and data transmission protocol in fast mode at 400 KHz. AW9110B operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW9110B can support different high level (1.8V~3.3V) of this I²C interface.

10.1 Start and Stop Condition

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

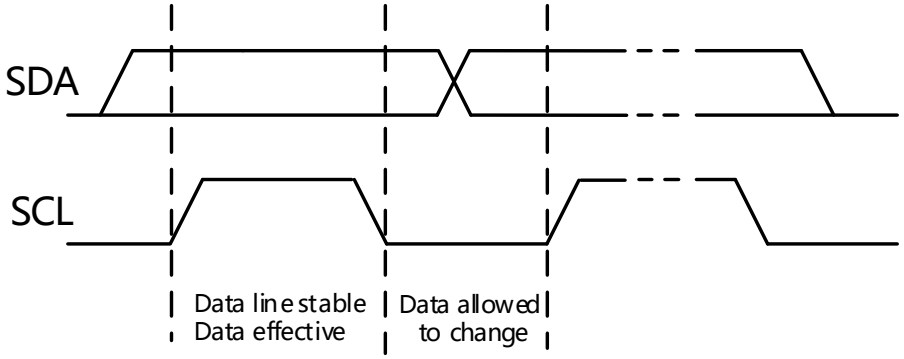


10.2 Data Transmission

After the start condition, I²C bus sent an address of slave. AW9110B wait to receive slave address When receiving start condition. If the address from I²C bus is same as the address of AW9110B, the slave pull SDA to acknowledge.

10.3 Data Validity

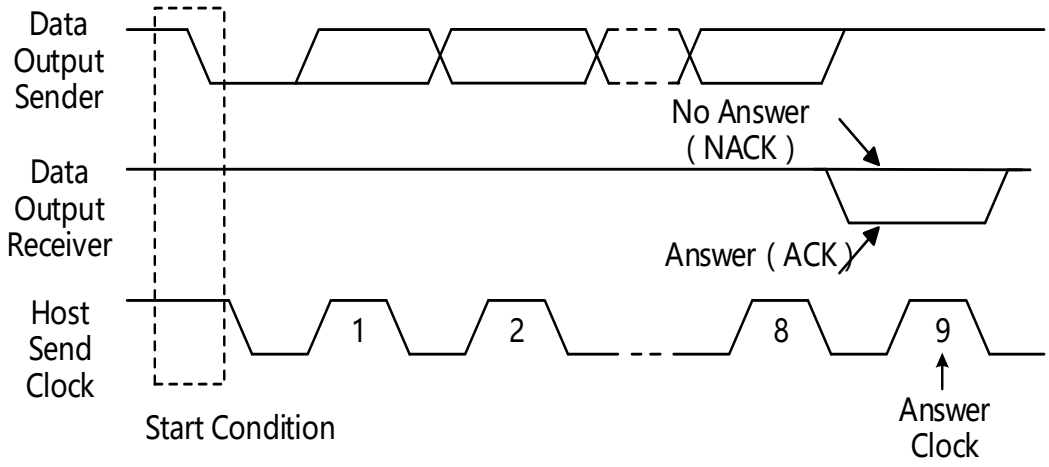
When SCL is in high level, SDA must remain one level stationary .Except start condition and stop condition, SDA level can change just in low level of SCL.



10.4 Acknowledge

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.



10.5 Address

AW9110B supply two address pins AD1,AD0. This allows single I²C bus can use four AW9110B at the same time. The high five bit of slave address is “10110”, the bit2 is AD1, and the bit1 is AD0. The bit0(LSB) is writing and reading flag bit, which define the next operation writing or reading. ‘1’ is read and ‘0’ is write.

1	0	1	1	0	AD1	AD0	R/$\overline{W}$

(The value of AD1 and AD0 is same as AD1 and AD0 PIN)

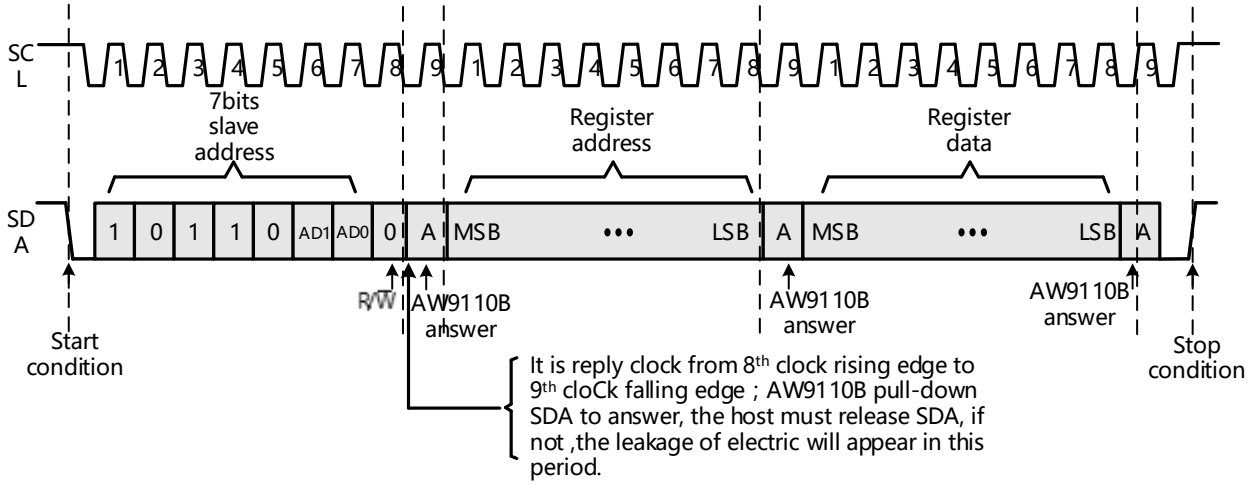
10.6 Writing Operation

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit firstly. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

1) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
2) Master device sends slave address (7-bit) and the data direction bit (w = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master sends 8Bit data to be written to the addressed register
7) Slave sends acknowledge signal
8) Master generates STOP condition to indicate write cycle end



10.7 Reading Operation

In a read cycle, the following steps should be followed:

1) Master device generates START condition
2) Master device sends slave address (7-bit) and the data direction bit (w = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master generates STOP condition followed with START condition or REPEAT START condition
7) Master device sends slave address (7-bit) and the data direction bit (r = 1).

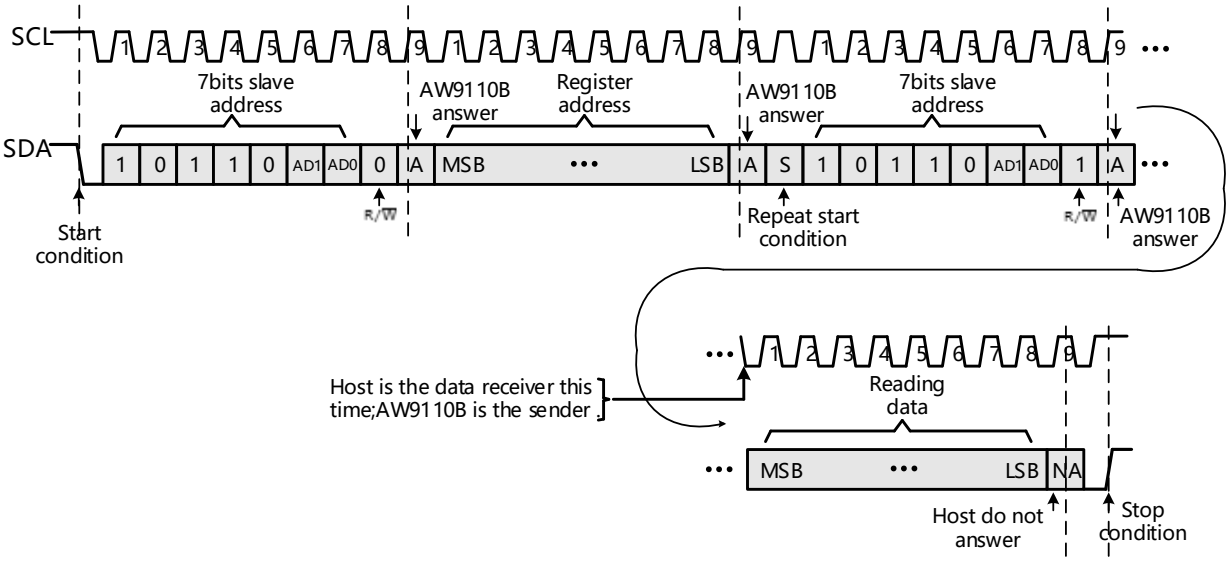
8) Slave device sends acknowledge signal if the slave address is correct.

9) Slave sends 8Bit data from addressed register.

10) Master sends acknowledge signal

11) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. If master sends no acknowledge signal, the slave device stop to send data and wait for STOP condition.

12) If the master device generates STOP condition, the read cycle is ended.



11 REGISTER DESCRIPTION

11.1 REGISTER OVERVIEW

Table 1. AW9110B registers list

Addr (HEX)	W/R	Defaut Value (HEX)	Function	Description
00H	R	xxH	GPIO_INPUT_A	OUT4～OUT9 port GPIO input state
01H	R	xxH	GPIO_INPUT_B	OUT0～OUT3 port GPIO input state
02H	W/R	Depend on AD1/ AD0	GPIO_OUTPUT_A	OUT4～OUT9 port GPIO output state; In SMART-FADE mode, OUT4~OUT5 can be used for “fade-on” and “fade-off” dimming control.
03H	W/R	Depend on AD1/ AD0	GPIO_OUTPUT_B	OUT0～OUT3 port GPIO output state; In SMART-FADE mode, OUT0~OUT3 can be used for “fade-on” and “fade-off” dimming control.
04H	W/R	00H	GPIO_CFG_A	OUT4～OUT9 port GPIO input and output direction control;

				In breathing mode, control OUT4~OUT5 to enter into BLINK mode or SMART-FADE mode.
05H	W/R	00H	GPIO_CFG_B	OUT0～OUT3 port GPIO input and output direction control; In breathing mode, control OUT0～OUT3 to enter into BLINK mode or SMART-FADE mode.
06H	W/R	00H	GPIO_INTN_A	OUT4～OUT9 enable interrupt function
07H	W/R	00H	GPIO_INTN_B	OUT0～OUT3 enable interrupt function
08H~10H	-	-	-	Reserved
11H	W/R	00H	CTL	Global Control
12H	W/R	FFH	GPMD_A	Switch OUT4～OUT9 LED driver mode or GPIO mode
13H	W/R	FFH	GPMD_B	Switch OUT0～OUT3 LED driver mode or GPIO mode
14H	W/R	00H	EN_BRE	Enable LED breathing mode
15H	W/R	00H	FADE_TMR	In BLINK or SMART-FADE mode, LED “fade-on” or “fade-off” time parameter
16H	W/R	00H	FULL_TMR	In BLINK mode, LED light all on or all off time parameter
17H	W/R	00H	DLY0_BRE	In BLINK mode,OUT0 blink delay time before start
18H	W/R	00H	DLY1_BRE	In BLINK mode,OUT1 blink delay time before start
19H	W/R	00H	DLY2_BRE	In BLINK mode,OUT2 blink delay time before start
1AH	W/R	00H	DLY3_BRE	In BLINK mode,OUT3 blink delay time before start
1BH	W/R	00H	DLY4_BRE	In BLINK mode,OUT4 blink delay time before start
1CH	W/R	00H	DLY5_BRE	In BLINK mode,OUT5 blink delay timer before start
1DH~1FH	-	-	-	Reserve
20H	W	00H	DIM0	OUT0 port 256 steps dimming control
21H	W	00H	DIM1	OUT1 port 256 steps dimming control
22H	W	00H	DIM2	OUT2 port 256 steps dimming control
23H	W	00H	DIM3	OUT3 port 256 steps dimming control
24H	W	00H	DIM4	OUT4 port 256 steps dimming control
25H	W	00H	DIM5	OUT5 port 256 steps dimming control
26H	W	00H	DIM6	OUT6 port 256 steps dimming control
27H	W	00H	DIM7	OUT7 port 256 steps dimming control
28H	W	00H	DIM8	OUT8 port 256 steps dimming control

29H	W	00H	DIM9	OUT9 port 256 steps dimming control
2AH~7EH	-	-	-	Reserve
7FH	W	00H	RESET	Write 00H,reset by software

11.2 REGISTER DETAIL

Table 2. DIM0~DIM9(20H~29H),256 steps dimming configuration register

Bit	Symbol	Description	Default
D[7:0]	DIM	256 steps dimming level choice 20H~29H corresponding to OUT0~OUT9 dimmer instruction; D[7:0] code from 0 to 255 corresponding to the current 0~I_{MAX}	00H

Table 3. CTL(11H),Global control register

Bit	Symbol	Description	Default
D7	GO	Writing 1 to enable breathing in BLINK mode.	0
D[6:5]	-	-	Remain
D4	GPOMD	OUT4～OUT9 driver option in GPIO application： 0：OPEN-DRAIN 1：PUSH-PULL	0
D[3:2]	-	-	Remain
D[1:0]	ISEL	256 dimming range option 00：0～37mA 01：0～27.75mA 10：0～18.5mA 11：0～9.25mA	00

Table 4. GPMD_A(12H), GPIO control switch to LED driver register

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	GPMD_A5	OUT9 mode control 0：LED mode 1：GPIO mode	1
D4	GPMD_A4	OUT8 mode control 0：LED mode	1

		1：GPIO mode	
D3	GPMD_A3	OUT7 mode control 0：LED mode 1：GPIO mode	1
D2	GPMD_A2	OUT6 mode control 0：LED mode 1：GPIO mode	1
D1	GPMD_A1	OUT5 mode control 0：LED mode 1：GPIO mode	1
D0	GPMD_A0	OUT4 mode control 0：LED mode 1：GPIO mode	1

Table 5. GPMD_B(13H), GPIO control switch to LED driver register

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	GPMD_B3	OUT3 mode control 0：LED mode 1：GPIO mode	1
D2	GPMD_B2	OUT2 mode control 0：LED mode 1：GPIO mode	1
D1	GPMD_B1	OUT1 mode control 0：LED mode 1：GPIO mode	1
D0	GPMD_B0	OUT0 mode control 0：LED mode 1：GPIO mode	1

Table 6. EN_BRE(14H),EN_BREATHING REGISTER

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain

D5	EN_BRE5	OUT5 enable breath mode 0：disable 1：enable	0
D4	EN_BRE4	OUT4 enable breath mode 0：disable 1：enable	0
D3	EN_BRE3	OUT3 enable breath mode 0：disable 1：enable	0
D2	EN_BRE2	OUT2 enable breath mode 0：disable 1：enable	0
D1	EN_BRE1	OUT1 enable breath mode 0：disable 1：enable	0
D0	EN_BRE0	OUT0 enable breath mode 0：disable 1：enable	0

Table 7. FADE_TMR(15H),Fade-on or fade-off time setting register in BLINK or SMART-FADE

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D[5:3]	FDOFF_TMR	Fade-off time setting 000：0ms 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms 110/111：0ms	000
D[2:0]	FDON_TMR	Fade-on time setting 000：0ms 001：315ms 010：630ms	000

		011：1260ms 100：2520ms 101：5040ms 110/111：0ms	

Table 8. FULL_TMR(16H),All-on or all-off time setting register in BLINK mode.

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D[5:3]	FLOFF_TMR	All-off time setting 000：0ms 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms 110：10080ms 111：20160ms	000
D[2:0]	FLON_TMR	All-on time setting 000：0ms 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms 110：10080ms 111：20160ms	000

Table 9. DLY0_BRE~DLY5_BRE(17H~1CH),delay to breath time setting register in BLINK

Bit	Symbol	Description	Default
D[7:0]	DLY_TMR	Start time to delay breathing in BLINK mode 00H：0ms 01H：315ms …… FFH：80640ms (per 1 unit: 315ms)	00H

Table 10. GPIO_INPUT_A(00H),GPIO input state register

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	GPIO_INPUT_A5	OUT9 pin state 0：Low level 1：High level	x
D4	GPIO_INPUT_A4	OUT8 pin state 0：Low level 1：High level	x
D3	GPIO_INPUT_A3	OUT7 pin state 0：Low level 1：High level	x
D2	GPIO_INPUT_A2	OUT6 pin state 0：Low level 1：High level	
D1	GPIO_INPUT_A1	OUT5 pin state 0：Low level 1：High level	x
D0	GPIO_INPUT_A0	OUT4 pin state 0：Low level 1：High level	x

Table 11. GPIO_INPUT_B(01H),GPIO input state register

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	GPIO_INPUT_B3	OUT3 pin state 0：Low level 1：High level	x
D2	GPIO_INPUT_B2	OUT2 pin state 0：Low level 1：High level	x
D1	GPIO_INPUT_B1	OUT1 pin state 0：Low level	x

		1：High level	
D0	GPIO_INPUT_B0	OUT0 pin state 0：Low level 1：High level	x

Table 12. GPIO_OUTPUT_A(02H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	GPIO_OUTPUT_A5	Driving OUT9 pin state 0：Low level 1：High level	Decided to AD0 and AD1
D4	GPIO_OUTPUT_A4	Driving OUT8 pin state 0：Low level 1：High level	
D3	GPIO_OUTPUT_A3	Driving OUT7 pin state 0：Low level 1：High level	
D2	GPIO_OUTPUT_A2	Driving OUT6 pin state 0：Low level 1：High level	
D1	GPIO_OUTPUT_A1	GPMD_A1=1,as driving OUT5 pin state 0：Low level 1：High level GPMD_A1=0 & EN_BRE5=1, OUT5 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D0	GPIO_OUTPUT_A0	GPMD_A0=1,as OUT4 pin state 0：Low level 1：High level GPMD_A0=0 & EN_BRE4=1, OUT4 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	

Table 13. GPIO_OUTPUT_B(03H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	GPIO_OUTPUT_B3	GPMD_B3=1,as driving OUT3 pin state 0：Low level 1：High level GPMD_B3=0 & EN_BRE3=1,OUT3 in SMART-FADE mode 0->1：fade-on control 1->0：fade-off control	Decided to AD0 and AD1
D2	GPIO_OUTPUT_B2	GPMD_B2=1, as driving OUT2 pin state 0：low level 1：high level GPMD_B2=0 & EN_BRE2=1,OUT2 in SMART-FADE mode 0->1：fade-on control 1->0：fade-off control	
D1	GPIO_OUTPUT_B1	GPMD_B1=1, as driving OUT1 pin state 0：low level 1：high level GPMD_B1=0 & EN_BRE1=1,OUT1 in SMART-FADE mode 0->1：fade-on control 1->0：fade-off control	
D0	GPIO_OUTPUT_B0	GPMD_B0=1, as driving OUT0 pin state 0：low level 1：high level GPMD_B0=0 & EN_BRE0=1,OUT0 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	

Table 14. GPIO_CFG_A(04H),GPIO input or output select register or as BLINK,SMART-FADE Mode select

Bit	Symbol	Description	Default

D[7:6]	-	-	Remain
D5	GPIO_ CFG _A5	OUT9 input or output selection 0：output 1：input	0
D4	GPIO_ CFG _A4	OUT8 input or output selection 0：output 1：input	0
D3	GPIO_ CFG _A3	OUT7 input or output selection 0：output 1：input	0
D2	GPIO_ CFG _A2	OUT6 input or output selection 0：output 1：input	0
D1	GPIO_ CFG _A1	GPMD_A1=1, OUT5 input or output choice 0：output 1：input GPMD_A1=0 & EN_BRE5=1, OUT5 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D0	GPIO_ CFG _A0	GPMD_A0=1, OUT4 input or output choice 0：output 1：input GPMD_A0=0 & EN_BRE4=1, OUT4 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0

Table 15. GPIO_CFG_B(05H),GPIO input or output selection register, or used for BLINK,SMART-FADE mode choice

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	GPIO_ CFG _B3	GPMD_B3=1 , OUT3 input or output choice 0：output	0

		1：input GPMD_B3=0 & EN_BRE3=1, OUT3 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	
D2	GPIO_ CFG _B2	GPMD_B2=1, OUT2 input or output choice 0：output 1：input GPMD_B2=0 & EN_BRE2=1, OUT2 BLINK or SMART-FADE mode choice 0：SMART-FADE 1：BLINK	0
D1	GPIO_ CFG _B1	GPMD_B1=1, OUT1 input or output choice 0：output 1：input GPMD_B1=0 & EN_BRE1=1, OUT1 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D0	GPIO_ CFG _B0	GPMD_B0=1, OUT0 input or output choice 0：output 1：input GPMD_B0=0 EN_BRE0=1, OUT0 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0

Table 16. GPIO_INTN_A(06H),GPIO Enable Interrupt Register

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	GPIO_ INTN _A5	OUT9 enable interrupt 0：enable 1：disable	0

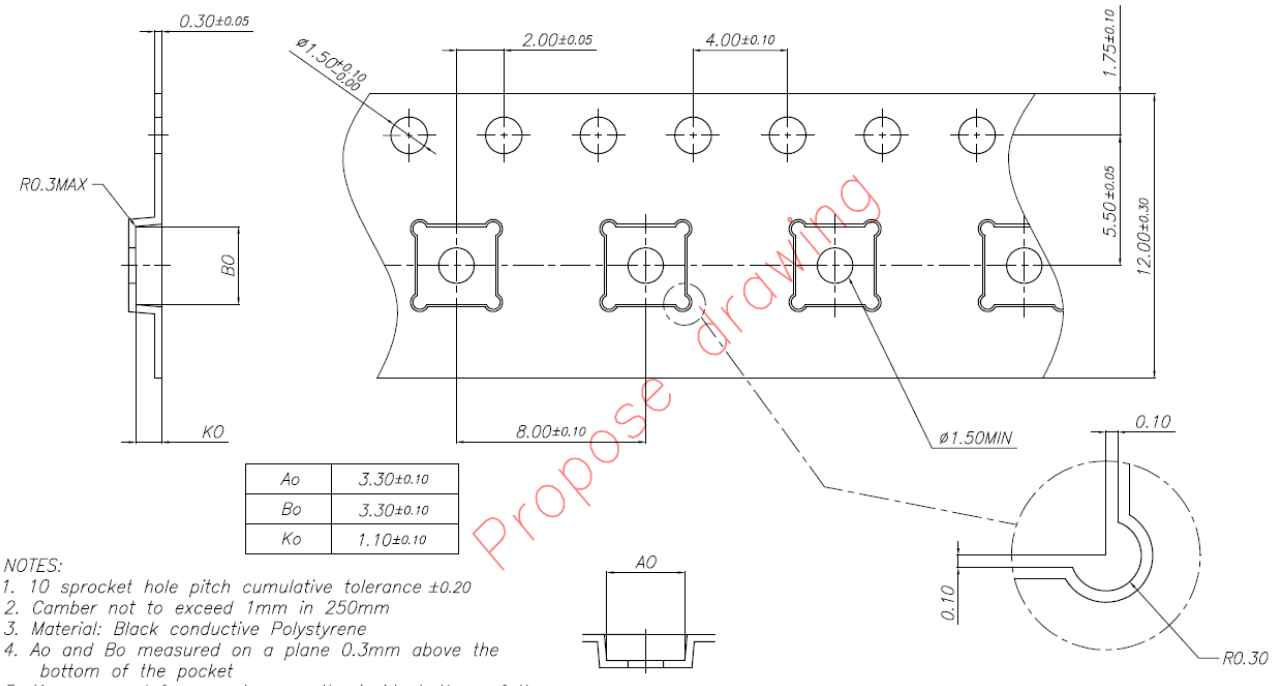
D4	GPIO_ INTN _A4	OUT8 enable interrupt 0：enable 1：disable	0
D3	GPIO_ INTN _A3	OUT7 enable interrupt 0：enable 1：disable	0
D2	GPIO_ INTN _A2	OUT6 enable interrupt 0：enable 1：disable	0
D1	GPIO_ INTN _A1	OUT5 enable interrupt 0：enable 1：disable	0
D0	GPIO_ INTN _A0	OUT4 enable interrupt 0：enable 1：disable	0

Table 17. GPIO_INTN_B(07H),GPIO Enable Interrupt Register

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	GPIO_ INTN _B3	OUT3 enable interrupt 0：enable 1：disable	0
D2	GPIO_ INTN _B2	OUT2 enable interrupt 0：enable 1：disable	0
D1	GPIO_ INTN _B1	OUT1 enable interrupt 0：enable 1：disable	0
D0	GPIO_ INTN _B0	OUT0 enable interrupt 0：enable 1：disable	0

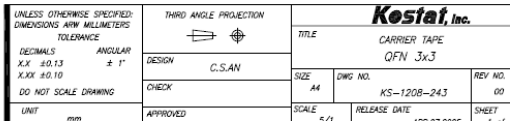
12 TAPE AND REEL INFORMATION

12.1 Carrier Tape

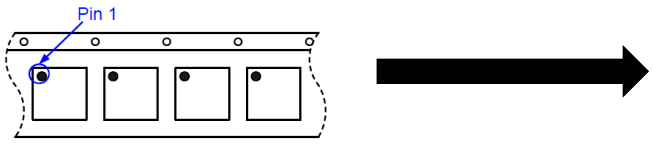


Ao	3.30±0.10
Bo	3.30±0.10
Ko	1.10±0.10

NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.20
2. Camber not to exceed 1mm in 250mm
3. Material: Black conductive Polystyrene
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be same position.

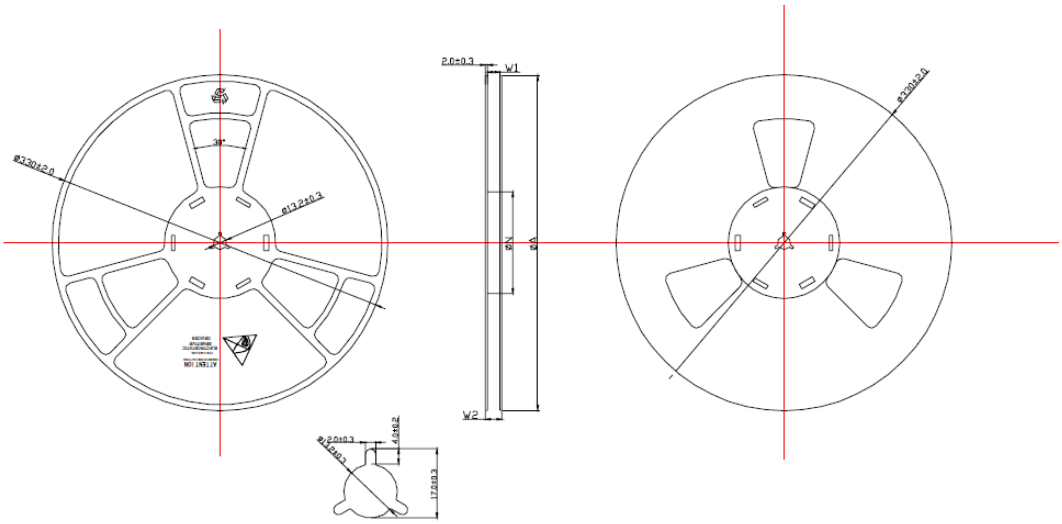


12.2 PIN1 Direction



User Direction of Feed

12.3 Reel

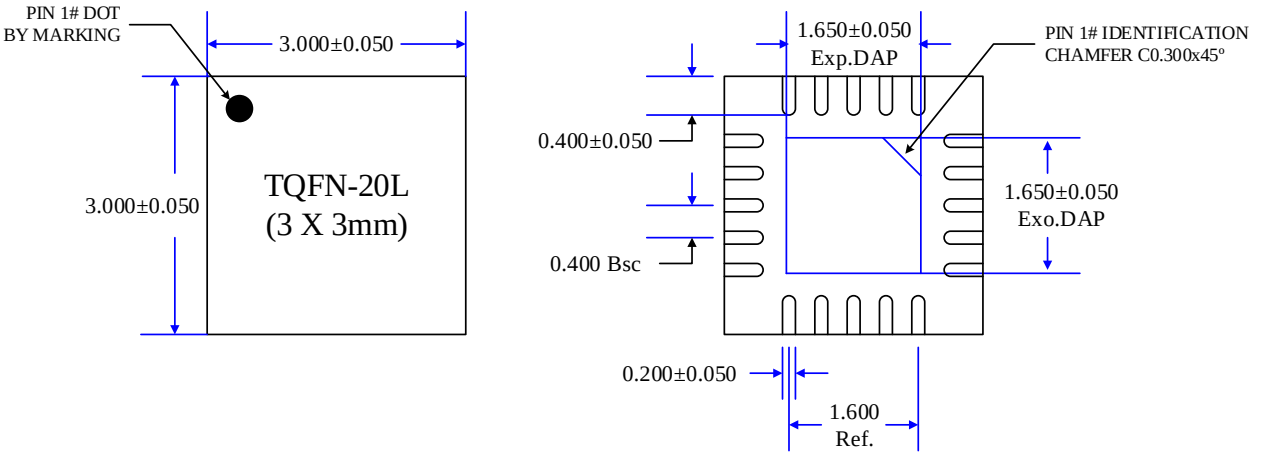


PRODUCT SPECIFICATIONS							
TYPE WIDTH	∅A	∅N	W1 (Min)	W2 (Max)	DRN. : ZHD	2005. 06. 25	TITLE:Platic Reel
12MM	330±2.0	100±1.0	12.4	19.4			
16mm	330±2.0	100±1.0	16.4	23.4	CHK. : RPP	2005. 06. 26	13''Inch(Dia)×4''Inch(HUB)
24MM	330±2.0	100±1.0	24.4	31.4			
32MM	330±2.0	100±1.0	32.4	39.4	RPP. : XGM	2005. 06. 30	Dwg NO.:CM-REEL-03
44MM	330±2.0	100±1.0	44.4	51.4			

Notes:

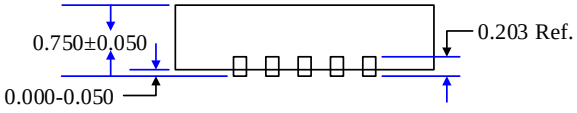
1. Material: polystyrene
2. Flatness: maximum permissible 3mm
3. All dimensions are in millimeters
4. Surface resistivity: 10^5 to 10^{11} ohms/sq or less
5. All unmarked tolerance: ±0.5

13 PACKAGE DESCRIPTION



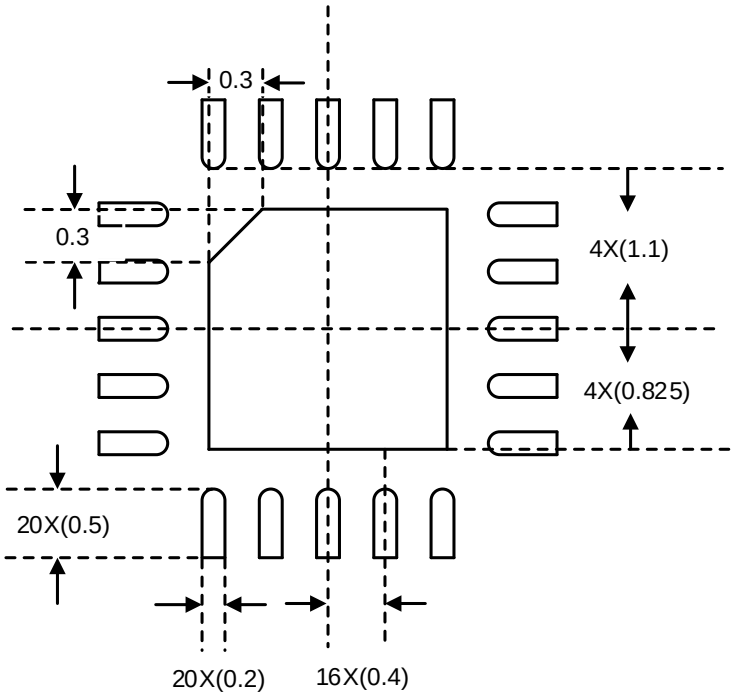
TOP VIEW

BOTTOM VIEW



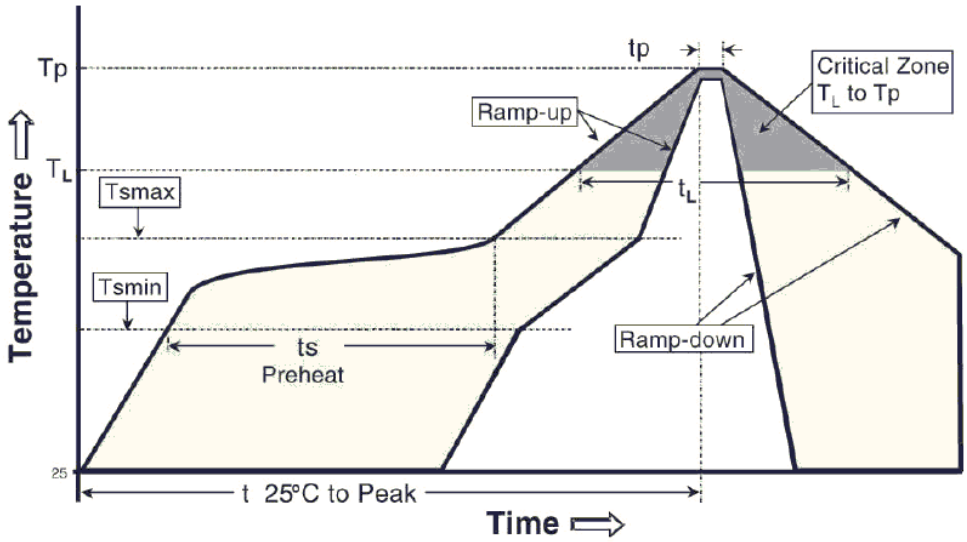
SIDE VIEW

14 RECOMMENDED LAND PATTERN



TOP VIEW

15 REFLOW



Reflow profile

Figure 17 Package Reflow Oven Thermal Profile

Reflow condition	Sn-Pb eutectic assembly		Pb-Free assembly	
	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3 °C/second max.		3 °C/second max.	
Preheat - Temperature Min ($T_{s(min)}$) - Temperature Max ($T_{s(max)}$) - Time (min to max) (t_s)	100 °C 150 °C 60-120 seconds		150 °C 200 °C 60-180 seconds	
$T_{s(max)}$ to T_L - Ramp-up Rate			3 °C/second max.	
Time maintained above: - Temperature (T_L) - Time (t_L)	183 °C 60-150 seconds		217 °C 60-150 seconds	
Peak Temperature (T_p)	225 +0/-5 °C	240 +0/-5 °C	245 +0/-5 °C	250 +0/-5 °C
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second max.		6 °C/second max.	
Time 25 °C to Peak Temperature	6 minutes max.		8 minutes max.	

Parameters for classification reflow profile

Note: 1. All of the temperature parameters are measured from the top of package;

2、AW9817 is suitable for Pb-Free assembly.

16 REVISION HISTORY

Vision	Date	Revision Record
V1.0	March 2017	First officially release
V1.1	Nov. 2017	Update the electrical characteristics Update the ordering information Add the recommended land pattern

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