SC8903 High Efficiency, Synchronous, Bi-Directional Buck-Boost Converter with Four Integrated MOSFET

1 Description

SC8903 is a synchronous 4-switch buck-boost converter with four integrated switches. It is able to effectively output voltage no matter it is higher, lower or equal to the input voltage.

SC8903 supports very wide input and output voltage range. It can support applications from 2.7V to 22V input range and 2.7V to 22V output range. It employs current-mode control and supports input current limit, output current limit, dynamic output voltage adjustment, internal current limit, output short protection and over temperature protections to ensure safety under different abnormal conditions.

The SC8903 is in a 40 pin 6x6 QFN package.

2 Features

- Integrated Four Switches
- Wide VIN Range: 2.7 V to 24V
- Wide VOUT Range: 2.7 V to 24V
- High Efficiency Buck-Boost Conversion
- Dynamic Output Voltage Control
- Adjustable Switching Frequency
- Programmable Input and Output Current Limit
- Input and Output Current Monitor
- Small Current Indication
- Under Voltage Protection, Over Voltage Protection, Over Current Protection
- Short Protection
- Thermal Shutdown Protection
- QFN-40 Package

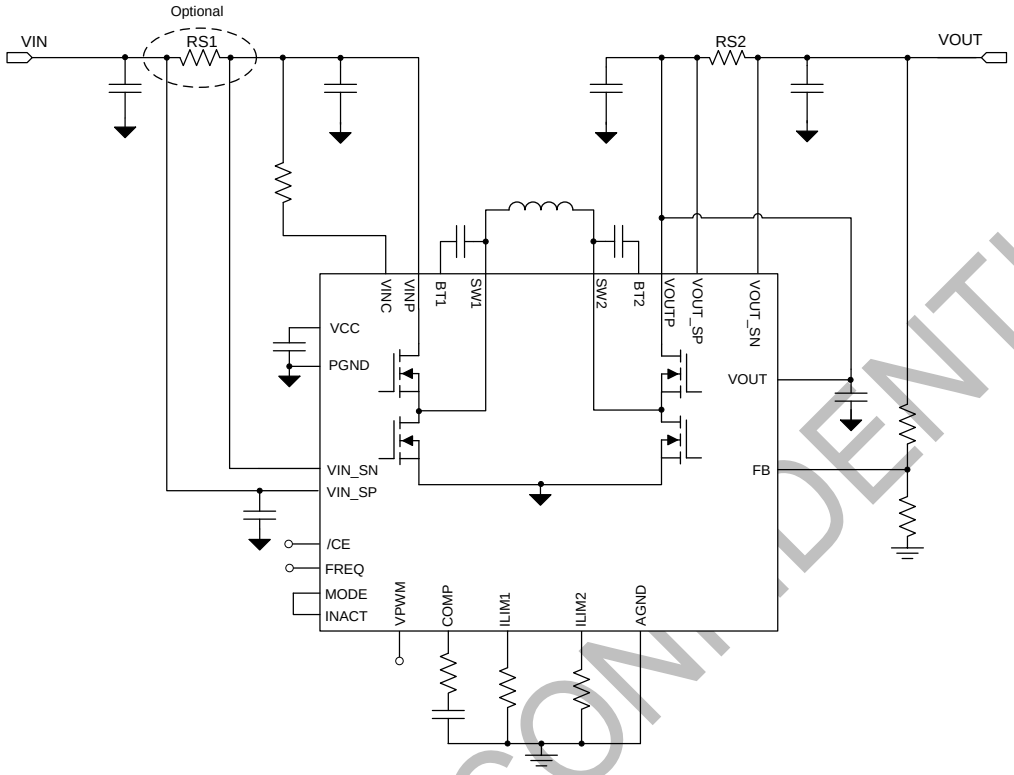
3 Applications

- Wall Adapter
- USB HUB
- USB Power Delivery
- Industrial Power Supplies

4 Device Information

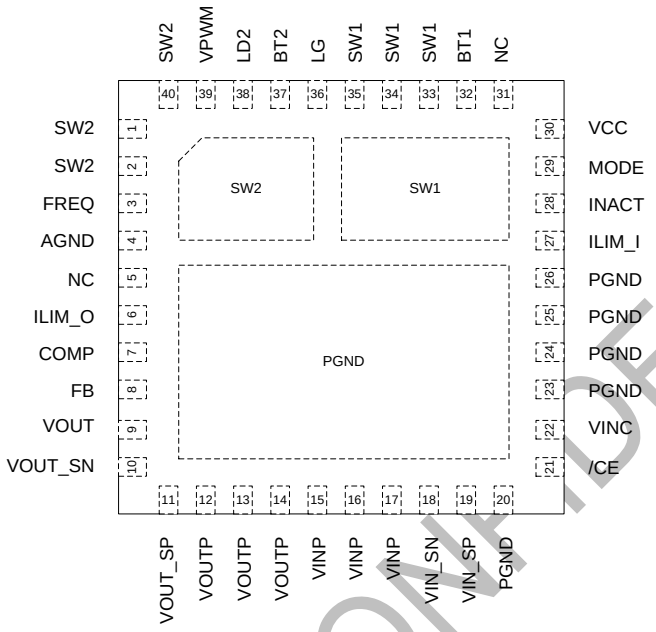
Part Number	Package	Dimension
SC8903QDHR	40 pin QFN	6.0mm x 6.0mm x 0.75mm

5 Typical Application Circuit



6 Terminal Configuration and Functions

Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1, 2	SW2	I/O	Switching Node 2. Connect to inductor.
3	FREQ	I	Use this pin to set the switching frequency. Short to ground: 460kHz Float: 230kHz
4	AGND	I/O	Analog ground. Connect all AGND pins together, and connect PGND and AGND together at the thermal pad under IC.
5	NC		NC pin. Leave it floating.
6	ILIM_O	I	Connect a resistor RILIM_O from this pin to AGND to set the VOUT side current limit. The calculation equation is as below. $IOUT\_LIM = \frac{VLIM\_REF}{RILIM\_O} \times \frac{1000\,\Omega}{RSNS\_O}$ VLIM_REF equals to 1.2V. RILIM_O is the resistor connected at ILIM_O pin, RSNS_O is the current sense resistor connected between VOUT_SP and VOUT_SN pins.
7	COMP	I	Connect a RC network to compensate internal control loop.
8	FB	I	Feedback node of output voltage. Set the output voltage by the resistor divider connected at this

			pin as below: $$VOUT\_SET = VREF \times \left(1 + \frac{RUP}{RDOWN}\right)$$ VREF equals to 1.2V. RUP and RDOWN are the resistor value of the resistor divider.
9	VOUT	P	Connect to VOUTP node to provide power supply to the IC. Connect a 1 μF capacitor from this pin to PGND close to IC.
10	VOUT_SN	I	Negative input of an internal current sense amplifier. Connect a current sense resistor between VOUT_SP and VOUT_SN to sense the IBUS current.
11	VOUT_SP	I	Positive input of an internal current sense amplifier. Connect a current sense resistor between VOUT_SP and VOUT_SN to sense the IBUS current.
12 – 14	VOUTP	P	The power output node of the converter. Connect to the output bulk capacitors.
15 – 17	VINP	P	The power input node of the converter. Connect to the input bulk capacitors.
18	VIN_SN	I	Negative input of an internal current sense amplifier. If input current limit function is needed, connect a current sense resistor between VIN_SP and VIN_SN to sense the IBAT current; otherwise, tie VIN_SP and VIN_SN to VINP pins directly.
19	VIN_SP	I	Positive input of an internal current sense amplifier. If input current limit function is needed, connect a current sense resistor between VIN_SP and VIN_SN to sense the IBAT current; otherwise, tie VIN_SP and VIN_SN to VINP pins directly.
20	PGND	I/O	Power ground. Connect all PGND pins together, and connect PGND and AGND together at the thermal pad under IC.
21	/CE	I	Chip enable pin, active low. That is, pull this pin to logic low to enable the chip. This pin is internally pulled low.
22	VINC	I	Connect to input voltage rail through a 200k resistor.
23-26	PGND	I/O	Power ground. Connect all PGND pins together, and connect PGND and AGND together at the thermal pad under IC.
27	ILIM_I	I	Connect a resistor RILIM_I from this pin to AGND to set the input current limit as below. $$IIN\_LIM = \frac{VLIM\_REF}{RILIM\_I} \times \frac{1000\ \Omega}{RSNS\_I}$$ VLIM_REF equals to 1.2V. RILIM_I is the resistor connected at ILIM_I pin, RSNS_I is the current sense resistor connected between VIN_SP and VIN_SN pins. Short this pin to AGND if input current limit function is not needed.
28	INACT	O	Open drain output to indicate the inactive load condition. It outputs logic low when the load is higher than 50mA typically, and outputs high impedance when the load is lower than the threshold.
29	MODE	I	To control the PFM/PWM operation mode under light load condition. MODE = low, IC operates in PWM mode under light load condition MODE = high or floating, IC operates in PFM mode under light load condition

30	VCC	O	Output of an internal regulator. Connect a 1 μF ceramic capacitor from VCC to PGND pin close to the IC. The regulator provides supply for internal gate drivers.
31	NC		NC pin. Leave it floating.
32	BT1	I	Connect a 100nF ceramic capacitor between BT1 pin and SW1 pin to provide the boosted bias voltage for high side gate driver.
33 – 35	SW1	I/O	Switching Node 2. Connect to inductor.
36	LG	I	Gate input of the integrated low side MOSFET. Connect to LD2 pin with or without a driving resistor in between.
37	BT2	I	Connect a 100nF capacitor between BT2 pin and SW2 pin to provide the boosted bias voltage for high side gate driver.
38	LD2	O	Gate driver output to the integrated low side MOSFET. User can short LD2 pin and LG pin directly, or connect a driving resistor between LD2 and LG pins to limit the driver current.
39	VPWM	I	To adjust the VOUT output voltage in real time. If a logic high signal is applied to VPWM pin, the output voltage is VOUT_SET. If applying a PWM signal in the range of 20kHz~100kHz to VPWM pin, the output voltage is proportional to the PWM duty cycle as below equation shows. $VOUT = VOUT\_SET \times D$ This pin is internally pulled **HIGH.** If this dynamic VOUT control function is used, in order to prevent that the IC outputs the highest VOUT_SET voltage when the VPWM signal is fault or open, it is suggested to add a 200 kΩ pull down resistor at this pin.
40	SW2	I/O	Switching Node 2. Connect to inductor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VPWM, FREQ, ILIM1, COMP, ILIM2, MODE, VCC	-0.3	5.5	V
	FB, VOUT, VOUT_SP, VOUT_SN, VOUTP, VINP, VIN_SP, VIN_SN, VINC, /CE, INACT	-0.3	24	V
	SW1, SW2	-0.3	30	V
	BT1, BT2	-0.3	40	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VIN	VIN voltage range	2.7	24	V
VOUT	VOUT voltage range	2.7	24	V
C_{IN}, C_{OUT}	VINP capacitor, VOUTP capacitor	22		µF
L	Inductance	2.2	10	µH
$R_{SNS1/2}$	Current Sensing Resistor	0	10	mΩ
f_{PWM}	PWM signal frequency range	20	100	kHz
D_{PWM}	PWM signal duty cycle range	0	100	%
T_A	Operating ambient temperature	-40	85	°C
T_J	Operating junction temperature	-40	125	°C

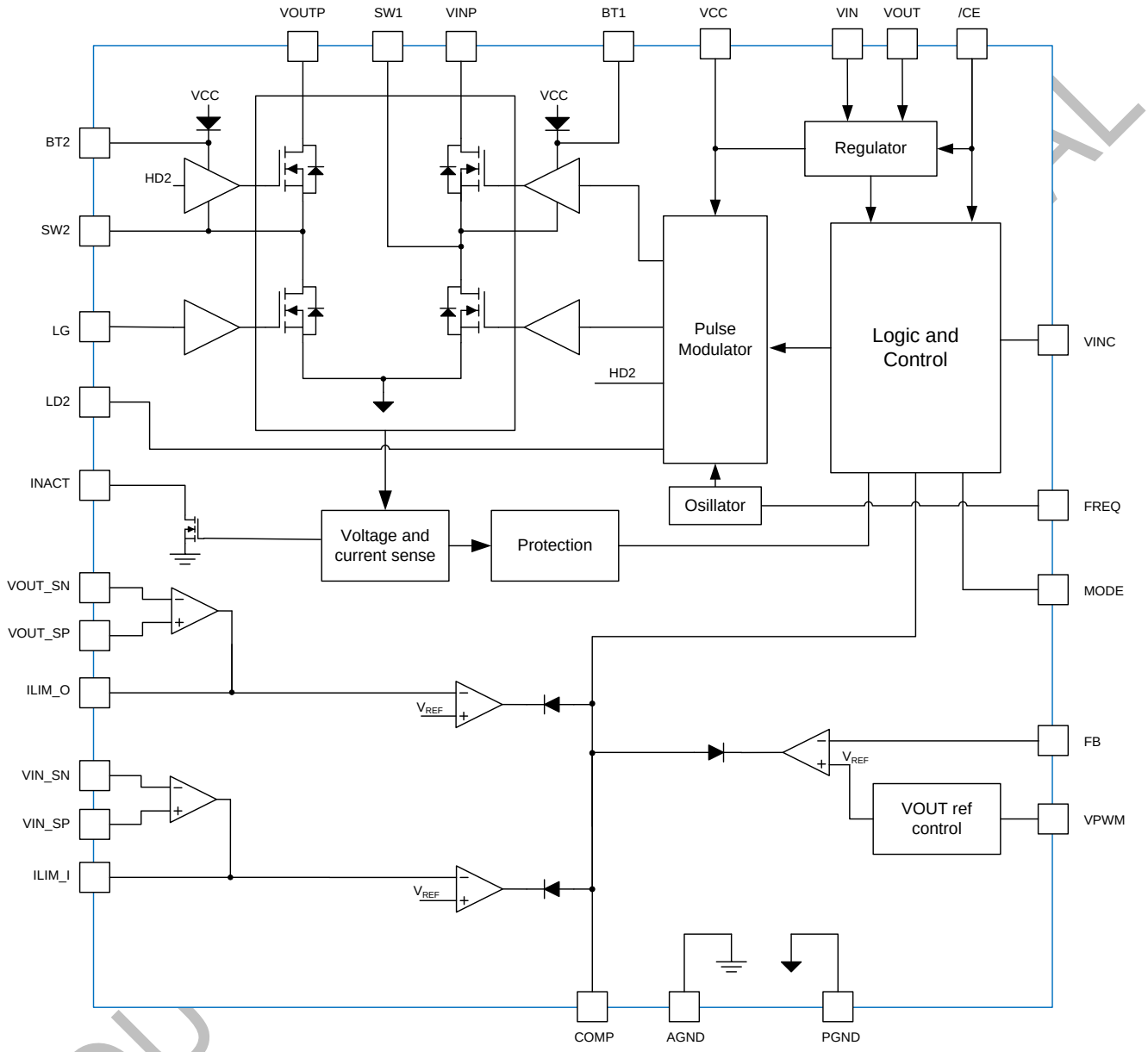
7.4 Electrical Characteristics

T_J= 25°C and V_{IN}= 5V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{UVLO}	VIN under-voltage lockout threshold	Rising edge		2.5	2.6	V
		Hysteresis		160		mV
I_Q	Quiescent current into VIN	VIN = 8V, VOUT = 5V /CE = L, non-switching		4		mA
		VIN = 8V, VOUT = 12V /CE = L, non-switching		1		mA
I_{SD}	Shutdown current into VIN	VIN = 8V /CE = H		5.5	15	μA
I_{LKG}	Leakage current into VINP pins	/CE = H, VINP = 8V			100	nA
VCC, DIRVER AND POWER SWITCH						
V_{CC}	VCC regulation voltage	VIN = 9V	5.2	5.35	5.45	V
		VIN = 5V, ICC = 30mA	4	4.1	4.2	V
I_{VCC_LIM}	VCC current limit	VIN = 9V, VCC = 4V	80	170	270	mA
R_{HS/LS_PU}	High/low side MOS driver pull up resistor			4.6		Ω
R_{HS/LS_PD}	High/low side MOS driver pull down resistor			0.7		Ω
R_{DSon_HS}	High side MOS on resistance			22		mΩ
R_{DSon_LS}	Low side MOS on resistance			8.5		mΩ
REFERENCE VOLTAGE						
V_{FB}	FB reference voltage		1.176	1.2	1.224	V
V_{FB_OVP}	FB OVP threshold, over FB target	Rising edge	107%	109.5%	112%	
		Hysteresis		2%		
V_{OUT_OVP}	Absolute VOUT OVP threshold		21.5	22	22.5	V
V_{SHORT}	Short circuit detection threshold			0.7		V
CURRENT LIMIT						
V_{LIM_REF}	ILIM_I / ILIM_O reference voltage		1.176	1.2	1.224	V
I_{OUT_LIM}	IOUT current limit accuracy	$I_{OUT} R_{SNS1} \geq 20mV$	-10%		10%	
I_{IN_LIM}	IIN current limit accuracy	$I_{IN\_LIM} R_{SNS1} \geq 20mV$	-25%		25%	
ERROR AMPLIFIER						
Gm_{EA}	Error amplifier gm			0.16		mS
R_{OUT}	Error amplifier output resistance			20		MΩ
I_{SINK_COMP}	COMP sink current			27		μA
I_{SRC_COMP}	COMP source current			16		μA

I_{BIAS_FB}	FB pin input bias current	FB in regulation			50	nA
SWITCHING						
f_{SW}	Switching frequency	FREQ = ground	420	470	520	kHz
		FREQ = float	200	230	260	kHz
INDICATION						
I_{SINK_INACT}	INACT pin sink current	V_{INACT} = 0.4V	3.4	4	4.6	mA
I_{COM}	Small load threshold		20	60	100	mA
LOGIC CONTROL						
R_{PD}	/CE pin internal pull down resistor			1.2		MΩ
	VPWM pin internal pull up resistor			0.9		MΩ
V_{IL}	/CE, VPWM and MODE pins input low voltage				0.4	V
V_{IH}	/CE, VPWM pins input high voltage		1.2			V
	MODE pin input high voltage		2			V
SOFTSTART						
t_{SS}	Internal soft-start time	From 10% to 90% VOUT		5		ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature (1)			165		°C
	Thermal shutdown hysteresis (1)			15		°C

8 Functional Block Diagram



9 Feature Description

The SC8903 is a synchronous buck-boost converter with four integrated power MOSFET. It supports a wide input/output voltage range from 2.7V to 22V, and can regulate the output at, above, below the input voltage. It features automatic smooth transition between buck mode and boost mode. The SC8903 can also offer input and output current limit functions, small output current detection function, and dynamic output voltage change to simplify power design.

9.1 Chip Enable

The SC8903 is enabled or disabled by /CE signal. When /CE input is logic low, the SC8701 is enabled; when /CE input is logic high, the SC8701 is disabled.

9.2 VOUT Voltage Setting

The SC8903 senses its output voltage through FB pin, so an external resistor divider shall connect from VOUT to FB to AGND. The SC8903 regulates the FB pin voltage to 1.2V to set the output, so the VOUT voltage can be calculated as:

$$V_{OUT\_SET} = V_{FB\_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

Where:

V_{FB_REF} = Internal reference voltage 1.2V

R_{UP} and R_{DWON} = Resistor divider at FB pin

9.3 Dynamic Output Control

The SC8903 supports dynamic output voltage control, which is controlled by VPWM input.

The VPWM pin accepts a PWM signal in the range of 20kHz to 50kHz, and its duty cycle controls the output voltage as below:

$$VOUT = V_{OUT\_SET} \times D$$

Where;

V_{OUT_SET} = VOUT voltage set by FB resistor divider,

D = Duty cycle of VPWM signal.

If VPWM input signal is logic high, which means 100% of duty cycle, the output voltage becomes the set value V_{OUT_SET}.

If VPWM input signal is logic low, which means 0% of duty cycle, the output voltage becomes off.

The VPWM signal is internally pulled high, so if this dynamic output control function is not required, user can leave VPWM pin floating, then the SC8903 outputs the set voltage V_{OUT_SET}.

If this dynamic output control function is used, in order to prevent that the IC outputs the VOUT_SET voltage directly when the VPWM signal is fault or open, it is suggested to add a 200 kΩ pull down resistor at this pin.

9.4 Small Load Current Indication

The SC8903 can indicate the output load condition through INACT pin. This pin is an open drain output, so a pull up resistor is required as below figure shows.

When the SC8903 detects its output current is lower than a threshold V_{ICOM}, it outputs high impedance at INACT pin. When output current is detected higher than V_{ICOM}, the IC pulls INACT pin to logic low internally.

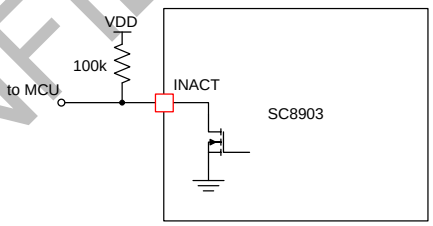


Figure 1 INACT pull up resistor

This indication function can report load status to a system controller, like an MCU. For example, it can be used to detect the load device removal for adapter applications.

9.5 Mode Selection

The SC8903 supports two operation modes: PWM mode and PFM mode. User can select the operation mode through MODE pin as below.

Table 1 Mode Selection

MODE Input	Operation Mode
Logic low	PWM mode
Logic high	PFM mode
Float	PFM mode

In PWM mode, the SC8903 always works with constant switching frequency for the whole load range. This helps achieve the best output voltage performance, but the efficiency is low at light load condition because of the high switching loss.

In PFM mode, the SC8903 still works with constant

switching frequency under heavy load condition, but under light load condition, the IC automatically changes to pulse frequency modulation operation to reduce the switching loss. The efficiency can be improved under light load condition while output voltage ripple will be a little larger compared with PWM operation. Below figure shows the output voltage behavior of PFM mode.

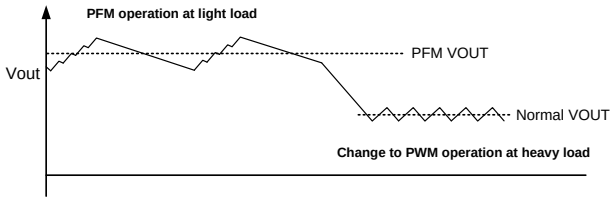


Figure 2 PFM operation

To balance the output ripple and efficiency, it is suggested to tie MODE pin with INACT pin. In this case, the PFM mode is only enabled after the small load current condition is detected.

9.6 Input /Output Current Limit

The SC8903 integrates two current sense amplifiers for input and output respectively. With external current sense resistor(s), it can provide input / output current limit functions. The IC monitors the voltage drop across the current sense resistor through the amplifier, and once the detected current exceeds the set limit value, the SC8903 reduces the switching duty cycle to regulate the current at the set limit.

User can set the current limit value at ILIM_I and ILIM_O pins through a resistor to ground as below:

$$IIN\_LIM = \frac{VLIM\_REF}{RILIM\_I} \times \frac{1000\ \Omega}{RSNS\_I}$$

$$IOUT\_LIM = \frac{VLIM\_REF}{RILIM\_O} \times \frac{1000\ \Omega}{RSNS\_O}$$

Where:

I_{IN_LIM} = Input current limit value

I_{OUT_LIM} = Output current limit value

V_{LIM_REF} = Internal reference voltage 1.2V

R_{ILIM_I} = Resistor from ILIM_I pin to ground

R_{ILIM_O} = Resistor from ILIM_O pin to ground

R_{SNS_I} = Current sense resistor between VIN_SP and VIN_SN pins

R_{SNS_O} = Current sense resistor between VOUT_SP and VOUT_SN pins

Normally a big current sense resistor like 10 mΩ or even 20 mΩ is helpful to achieve high current limit accuracy, but will reduce the power efficiency due to its high conduction loss ($P_{LOSS} = I^2R$). So the user should make a tradeoff between the accuracy and the efficiency according to design targets.

For the applications where the input current limit function is not required, the input current sense resistor can be removed. The user shall short both VIN_SP and VIN_SN pins to VINP pins, and also short ILIM_I pin to ground to disable the input current limit function.

The output current sense resistor is necessary for over current protection. Please see details in Over Current Protection section.

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

9.7 Input /Output Current Monitor

With the external current sense resistor at input / output, the ILIM_I / ILIM_O pin's voltage is proportional to input / output current, so the user can monitor the current through ILIM_I / ILIM_O pin as below:

$$IIN = \frac{VLIM\_I}{RILIM\_I} \times \frac{1000\ \Omega}{RSNS\_I}$$

$$IOUT = \frac{VLIM\_O}{RILIM\_O} \times \frac{1000\ \Omega}{RSNS\_O}$$

Where:

I_{IN} = input current

I_{OUT} = output current

V_{LIM_I} = voltage at ILIM_I pin

V_{LIM_O} = voltage at ILIM_O pin

R_{SNS_I} = Current sense resistor between VIN_SP and VIN_SN pins

R_{SNS_O} = Current sense resistor between VOUT_SP and VOUT_SN pins

To get a better voltage sense, a RC circuit as below is recommended to filter the voltage ripple on ILIM_I/O pins. If the RC filter is not added, the MCU itself should implement digital filter.

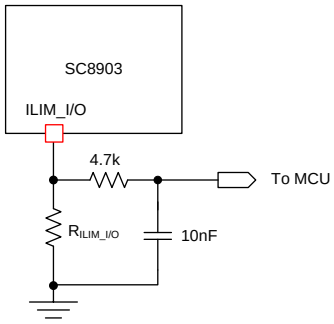


Figure 3 Circuit for ILIMx pin voltage monitor

9.8 Switching Frequency Setting

The SC8903 provides two switching frequency selection as below. Real-time setting change is not supported. New setting will be effective in next power on.

Table 2 Switching frequency setting

FREQ Input	Switching Frequency
Logic low	460kHz
Float	230kHz

9.9 Loop Compensation

The internal control loop should be compensated by the resistor and capacitor connected at COMP pin. 15 kΩ resistor and 15 nF capacitor are suggested for most applications. If faster response is required, the user can increase the resistor value but should keep R*C value unchanged. After changing the compensation, check and make sure the loop is stable under target conditions.

9.10 Soft Start

The SC8903 implements soft start feature to prevent inrush current during startup. After the SC8903 is enabled, the IC turns on VCC first, and then ramps up the internal reference voltage in around 6ms. The output voltage follows the reference so it starts up slowly. Meantime, the SC8903 ramps up the output current limit during the startup. If a heavy load is applied before the output voltage is established, the SC8903 may fail to start up due to the limit.

For the applications which require startup with load, below circuit is suggested. During startup, VCC voltage is turned on first, and V_B voltage is pulled up through C1 to turn on Q1. So R_{SU} and R_{ILIM_O} are parallel to set a higher output current limit. After V_B voltage drops below Q1's threshold, only R_{ILIM_O} is connected at ILIM_O pin, so the current limit recovers to original value.

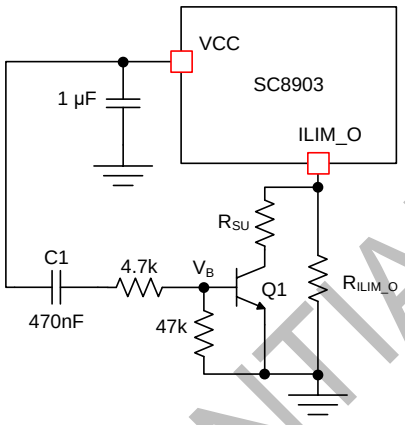


Figure 4 Circuit for startup with heavy load

The user can adjust the startup current capability by changing R_{SU} (even to 0 Ω) and adjust the recovery time by changing the C1 value.

9.11 Over Voltage Protection

The SC8903 supports two kinds of output over voltage protection.

The first protection is once the IC detects the VIN or VOUT voltage is higher than typical 22V, the IC stops switching until the voltage drops below the threshold.

The second protection is once the IC detects the VOUT voltage is higher than the setting target by typical 10%, the IC stops switching until the voltage drops below the threshold. This over voltage is still valid with dynamic voltage change function. For example, if the user sets the output voltage to 5V through VPMW signal, the IC can still stop switching once the VOUT is higher than 5.5V.

9.12 Over Current Protection

The SC8903 implements internal current limit at 10A. Once the IC detects the inductor current is higher than 10A, it reduces the switching duty cycle, and keeps the inductor current from increasing.

To realize a stronger over current protection, it is suggested to add a current sense resistor at VOUT to realize output current limit function, enhancing the protection schemes. For applications which don't require accurate output current limit, the user can use small resistor like 2 mΩ or even 1 mΩ and set the I_{OUT_LIM} to 20%~30% higher than the maximum load to realize the protection.

9.13 Short Circuit Protection

The SC8903 supports FB pin short circuit protection. During

power on, the IC monitors the FB pin status. Once it detects the FB pin is short to ground, it still starts up and limits the output voltage at 5V fixed voltage. This helps protect the circuits connected at VOUT pin from over voltage.

Besides FB short circuit protection, the SC8903 also monitors the output voltage all the time. Once it detects the VOUT voltage drops below short circuit protection threshold, typical 1V, the SC8903 reduces the input and output current limits to 1/10 of the original setting.

9.14 Over Temperature Protection

Once the SC8903 detects the chip junction temperature exceeds the threshold (160°C typical), the IC goes into thermal shutdown and stops switching. When the junction temperature falls below typical 145°C, the IC resumes operation.

10 Application Information

10.1 Input and Output Capacitor Selection

Since MLCC ceramic capacitor has good high frequency filtering and low ESR, X5R or X7R capacitors are recommended for input and output capacitors. Typically, three 22 μF ceramic input capacitors and three 22 μF ceramic output capacitors work for most applications. The input / output capacitors should be places as close to VINP / VOUTP pins as possible, and they should be also near the PGND pins or thermal pad.

Capacitors' derating effect under DC bias should be taken into account when selecting the capacitors. Ceramic capacitor normally loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate effective capacitance. For example, if the highest operating voltage is 12V, select 16V or 25V capacitor.

Besides this, high value electrolytic capacitor or tantalum capacitor is recommended to place in parallel with the ceramic capacitors at output to improve the load transient response.

10.2 Inductor Selection

Because the selection of inductor affects the loop stability and the power efficiency, inductor is one of the most important components for the DCDC design.

The SC8903 can work with inductors between 2.2 μH to 10 μH range for most applications. A higher value is suggested to keep the inductor current ripple ≤ 30% of the DC current.

Compared with high value inductor in the same package size, a lower value inductor normally has smaller DC resistance (DCR), so can reduce the conduction power loss, which can be calculated roughly as

$$PL\_DC = IL^2 \cdot DCR$$

IL is the average value of inductor current, and it equals to IIN or IOUT.

However, besides DCR, the core loss or AC loss of an inductor also affects the power efficiency a lot. The low value inductor causes large inductor current ripple, thus high core loss or AC loss, so it is not always the low value inductor supports the higher efficiency.

Since the core loss is related to the inductor material type, and normally the inductor vendors don't provide the core loss data, it is very difficult to suggest what inductor value can result in higher efficiency. As a rule of thumb, high value inductor like 4.7 μH to 10 μH is recommended for applications where the difference between input voltage and output voltage is big, such as 5V VIN and 20V VOUT; while for those applications where input voltage is close to output voltage but large current is on power path, low value inductor like 2.2 μH is suggested.

For applications where efficiency or thermal dissipation is very important, it is highly suggested that the user chooses the inductor in larger package size for lower DCR, and also tests the efficiency with different inductor values and different switching frequencies, so to find the best combination to achieve the highest efficiency.

The saturation current is another important parameter when selecting the inductor. The inductance can decrease 20% to 35% when the current approaches saturation level, so the user should make sure the saturation current is higher than the inductor peak current during the operation.

The inductor peak current can be calculated by below formula.

When VIN is lower than VOUT:

$$IL\_peak = IIN + \frac{VIN \cdot (VOUT - VIN \cdot \eta)}{2 \cdot VOUT \cdot L \cdot fsw}$$

When VIN is higher than VOUT:

$$IL\_peak = IOUT + \frac{VOUT \cdot (VIN - VOUT)}{2 \cdot VIN \cdot L \cdot fsw \cdot \eta}$$

IL_peak is the inductor peak current

fsw is the selected switching frequency

η is the power efficiency

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

10.3 Current Sense Resistor

The RS1 and RS2 in the typical application circuit are current sense resistors for current limit / monitor functions. The IC can work well without the two resistors, so the user can remove them if the limit / monitor functions are not needed. However, it is highly suggested to keep RS2 for enhanced over current protection.

If the current sense resistor is not used, the user should tie the sense input pins together and connect them to the relevant power node. For example, if RS1 is not used, user should tie VIN_SP and VIN_SN together and connect them to VINP pins.

If the current sense resistor is needed, a high resistor value can result in high current limit / monitor accuracy but causes high conductor loss. Typically 10 mΩ is recommended. But for applications where efficiency is more important than accuracy, lower value is suggested. For example, if VOUT current limit is required just for enhanced over current protection, user can use 2 mΩ or even 1 mΩ resistor and set the I_{OUT_LIM} 20%~30% higher than the maximum IOUT.

When selecting the current sense resistor, its power rating and temperature coefficient should also be considered.

The power dissipation can be roughly calculated as $P=I^2R$, where I is the highest current flowing through it. The power rating should be higher than the calculated value.

The resistor value varies with temperature and the variation is decided by its temperature coefficient. If high accuracy of limit or monitor is required, select as lower temperature coefficient as possible.

10.4 Snubber Circuit and Driver Resistor

The RC snubber circuits at SWx nodes as shown below can be used to suppress the switching spike so to improve the EMC performance. A typical snubber circuit is composed by a 2.2Ω resistor and 1nF capacitor. The user can reduce the resistance and increase the capacitance further to improve the EMC. However, because it often causes higher switching loss and results in lower efficiency, it is suggested not to add snubber circuits unless necessary.

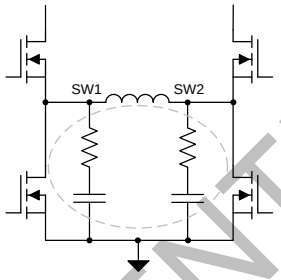


Figure 5 Snubber circuit at SWx nodes

The SC8903 also allows user adding a driver resistor for the low side MOSFET at VOUT side to slow down the switching, thus to reduce the switching spike improve the EMC performance. However, because the driver resistor also causes higher switching loss and thus lower efficiency, it is suggested not to add the driver resistor unless necessary.

If the driver resistor is needed, a 0603 resistor should be used, and it should be placed near the IC.

11 Layout Guide

For switching power supplies, the layout is an important step. If the layout is not carefully designed, the converter may suffer instability and noise issues.

1. The input bulk capacitors should be placed close to VINP and PGND pins, and the connection traces should be as short as possible. Put a 100nF capacitor parallel with the bulk capacitors to absorb high frequency noise. Since the trace will carry high current, wide copper are suggested. Similarly, the output bulk capacitors should be placed close to VOUTP and PGND pins, and keep the trace as wide and short as possible. It is suggested to put the input and output capacitors on the contrary layer to the IC, so the trace to PGND pad can be in the shortest way. Place sufficient vias to connect VINP or VOUTP pins to the capacitors. User can refer to below layout as an example.

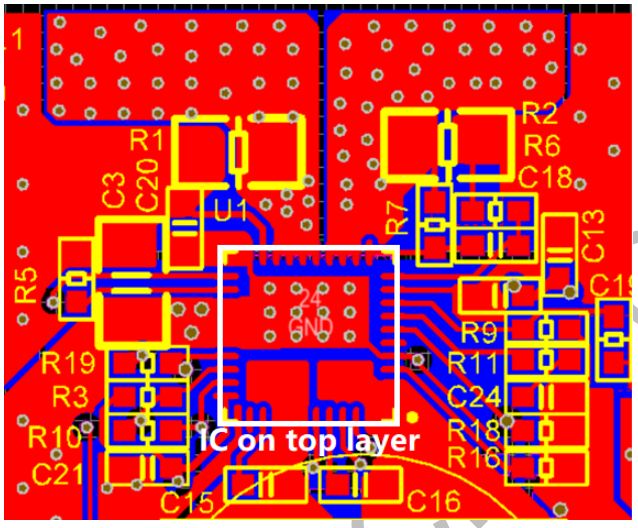


Figure 6 IC on top layer

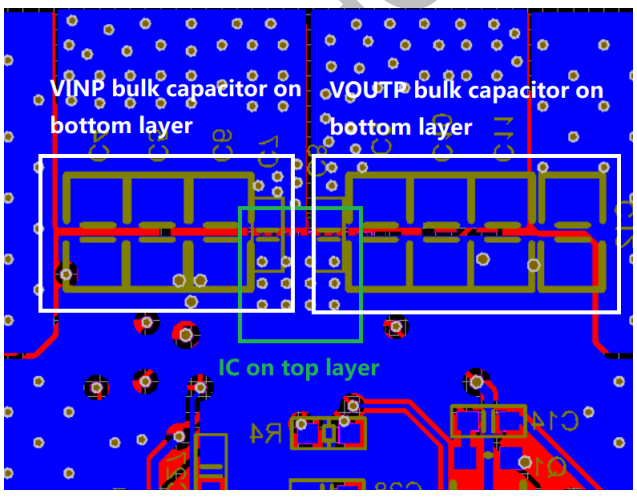


Figure 7 Bulk capacitors on bottom layer

2. Put the 1 μF bypass capacitor at VCC / VIN_SP / VOUT pins as close to the IC as possible. The ground trace of the capacitor to PGND pins should be as short as possible.
3. Put the inductor close to the SW1 and SW2 pins. Keep the SW1 and SW2 traces wide because they carry high current during operation. Connect SW1 pins to the SW1 thermal pad under IC, and connect SW2 pins to the SW2 thermal pad.
4. Put the boot strap capacitors between BTx and SWx pins and the driving resistor between LG and LD2 pins close to the IC.
5. If current sense resistor is used for current sense or limit function, how to connect the sensing trace to the sense resistor is very important for the accuracy. It is required to route as below: the sensing trace should be routed to the pads of the sense resistor instead of the copper trace. Bad connection way will introduce sense error.

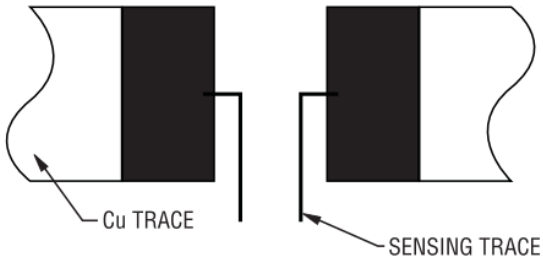


Figure 8 Sensing trace connection for current sense resistor

6. If it is for output current sense, differential resistors and capacitor close to the sense pins as below is needed to suppress the switching noise. The sense traces should be routed in differential way.

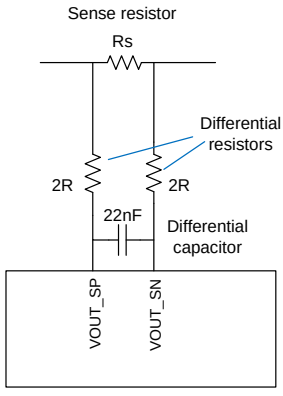
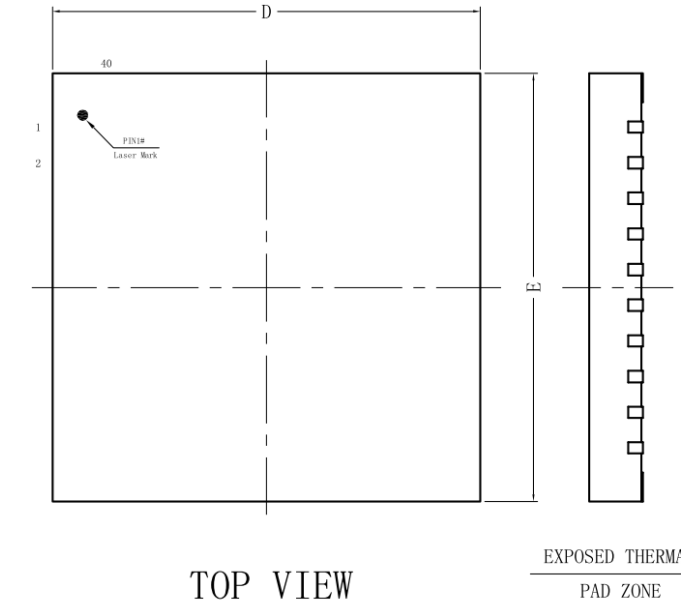


Figure 9 differential sense for current

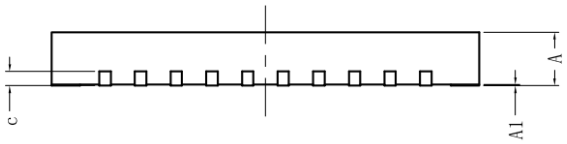
7. However, the differential resistors are not allowed for input current sense because there is operation current into VIN_SP pin and the differential resistor will lead to wrong sense. The FB resistor divider, ILIMx resistor and COMP components should be put close to the IC.
8. Separate the analog ground from power ground to avoid switching noise. The ground of the analog components like FB resistor, ILIM_I/O resistor, COMP components should be connect together, and the ground of the power components like the input/output bulk capacitor should be connect together. Then tie the analog ground and power ground at a single point, like at the ground thermal pad.
9. It is suggested to have a ground layer in the middle of PCB so the power ground can be complete. If only two layers are used, other signal traces should not block the ground return, and the power ground should be kept as wide and complete as possible.

MECHANICAL DATA

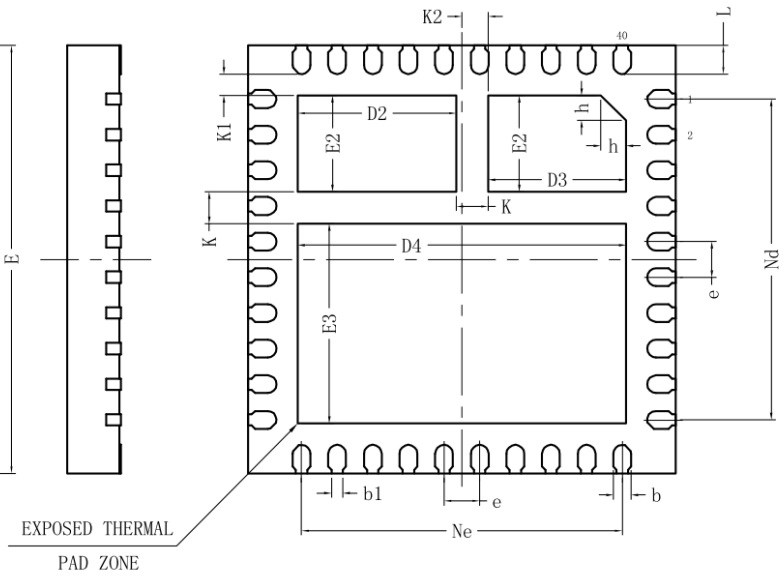
QFN40L(6x6x0.75)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
b1	0.16REF		
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	2.12	2.22	2.32
D3	1.83	1.93	2.03
D4	4.50	4.60	4.70
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	1.25	1.35	1.45
E3	2.70	2.80	2.90
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.40	0.45	0.50
K1	0.25	0.30	0.35
K2	0.32	0.37	0.42