



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issued	Sep.8. 2015
Rev. 1.1	Added <u>POWER UP INITIALIZATION</u> in page2 & <u>COMMAND TERMINATION</u> in page3	Dec.15. 2015
Rev. 1.2	Revised <u>QPI Mode : Write Operations(38h or 02h)</u> in page8 Revised Operating Temperature to (-25°C to 85°C)	Dec.25. 2015



FEATURES

- SPI compatible bus interface
 - Clock rate:
 - 33MHz(max) for normal read
 - 100MHz(max) for fast read
 - Mode: SPI/QPI
- **Low power consumption:**
Operating current: 20mA(TYP.)
- Single 1.8V power supply
- Unlimited read/write cycle
- Fast write time as minimum cycle time
- 4M x 8-bit organization
 - 1K byte per page
- High Reliability
- **Green package available**
- Package : 8-pin 150 mil SOP

GENERAL DESCRIPTION

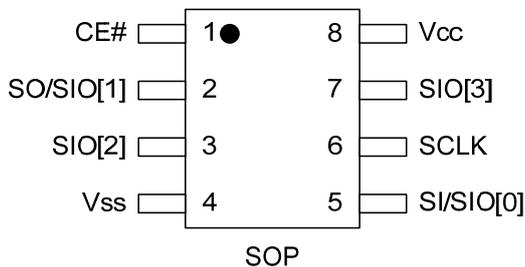
The LY68S3200 is a 32M-bit serial pseudo SRAM device organized as 4Mx8 bits. It is fabricated using very high performance, high reliability CMOS technology.

The LY68S3200 is accessed via a simple Serial Peripheral Interface(SPI) compatible serial bus. Additionally, Quad Peripheral Interface(QPI) is supported if your application needs faster data rates. This device also supports unlimited reads and writes to the memory array.

The LY68S3200 operates from a single power supply of 1.8V and can offer high data bandwidth at 100MHz clock rate and Serial Quad interface.

The LY68S3200 offers 8-lead SOP package.

Pin Configuration



PIN DESCRIPTION

SYMBOL	SPI MODE	SQI MODE
SI/SIO[0]	Serial Input	Serial I/O[0]
SO/SIO[1]	Serial Output	Serial I/O[1]
SIO[2]	-	Serial I/O[2]
SIO[3]	-	Serial I/O[3]
CE#	Chip Select Input	
SCLK	Clock Signal Input	
V _{CC}	Power Supply	
V _{SS}	Ground	

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 2.3	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	-25 to 85	°C
Storage Temperature	T _{STG}	-65 to 150	°C

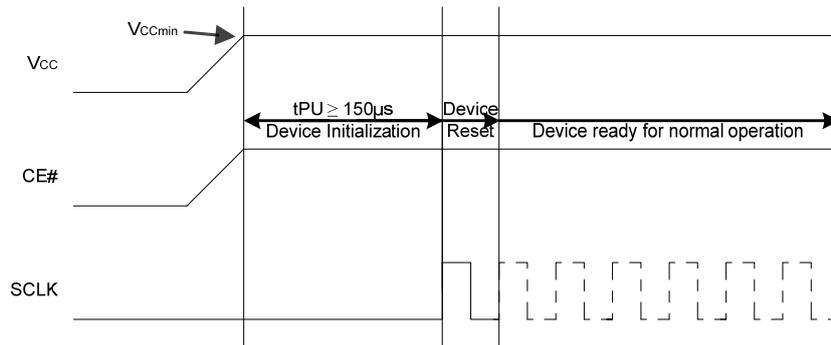
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



POWER-UP INITIALIZATION

The LY68S3200 includes an on-chip voltage sensor used to start the self-initialization process. When V_{CC} reaches a stable level at or above minimum V_{CC} , the device will require $150\mu s$ to complete its self-initialization process. From the beginning of power ramp to the end of the $150\mu s$ period, SCLK should remain LOW, CE# should remain HIGH(track V_{CC} within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the $150\mu s$ period, the device requires at least one clock during CE# high to properly reset the device, and then the device is ready for normal operation.



Command/Address Latching Truth Table

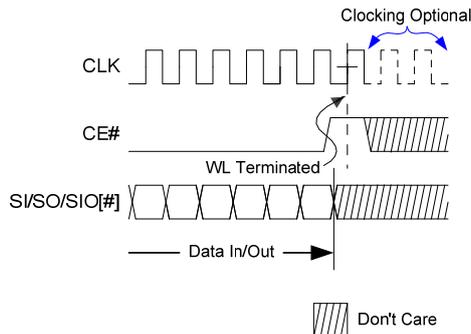
Command	Code	SPI Mode					QPI Mode				
		Cmd	Addr	Wait Cycle	DIO	Max Freq.	Cmd	Addr	Wait Cycle	DIO	Max Freq.
Read	03h	S	S	0	S	33	N/A				
Fast Read	0Bh	S	S	8	S	100	N/A				
Quad Read	EBh	S	Q	6	Q	100	Q	Q	6	Q	100
Write	02h	S	S	0	S	100	Q	Q	0	Q	100
Quad Write	38h	S	Q	0	Q	100	Q	Q	0	Q	100
Enter QPI Mode	35h	S	-	-	-	100	N/A				
Exit QPI Mode	F5h	N/A					Q	-	-	-	100

Note: S = Serial IO, Q = Quad IO



COMMAND TERMINATION

All Reads & Writes must be completed by a clock pulse of CE# high immediately afterwards in order to terminate the active read/write wordline and set the device into standby. Not doing so will block internal refresh operations until the device sees the read/write wordline terminated.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*1}	MAX.	UNIT	
Supply Voltage	V _{CC}		1.65	1.8	1.95	V	
Input High Voltage	V _{IH}		V _{CC} -0.4	-	V _{CC} +0.2	V	
Input Low Voltage	V _{IL}		- 0.2	-	0.4	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -0.2mA	0.8*V _{CC}	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = +0.2mA	-	-	0.2*V _{CC}	V	
Average Operating Power Supply Current	I _{CC1}	CE# ≤ 0.2, Others at 0.2V or V _{CC} -0.2V I _{I/O} = 0mA;f=max	SPI@33MHz	-	6	15	mA
			QPI@100MHz	-	20	30	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V, Others at 0.2V or V _{CC} - 0.2V	-	-	150	μA	

Notes:

1. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

**CAPACITANCE** ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC}-0.2V$
Input Rise and Fall Times	1.5ns
Input and Output Timing Reference Levels	$V_{CC}/2$
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -0.2\text{mA}/+0.2\text{mA}$

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	LY68S3200		UNIT
		MIN.	MAX.	
Clock Cycle Time	$t_{CLK@33\text{MHz}}$	30	-	ns
	$t_{CLK@100\text{MHz}}$	10	-	ns
Clock low width	t_{CL}	0.45	0.55	t_{CLK}
Clock high width	t_{CH}	0.45	0.55	t_{CLK}
Clock rise time	t_R	-	1.5	ns
Clock fall time	t_F	-	1.5	ns
CE# setup time to CLK rising edge	t_{CSP}	2.5	-	ns
Setup time to active CLK edge	t_S	2.5	-	ns
Hold time from active CLK edge	t_H	2	-	ns
Chip disable to DQ output high-Z	t_{HZ}	-	7	ns
CLK falling to output valid	t_{ACLK}	-	7	ns
Output Hold from Clock falling	t_{OH}	1.5	-	ns
CE# low pulse width	t_{CEM}	-	5	us



SPI MODE OPERATIONS

The device powers up into SPI mode by default, but can also be switched into QPI mode.

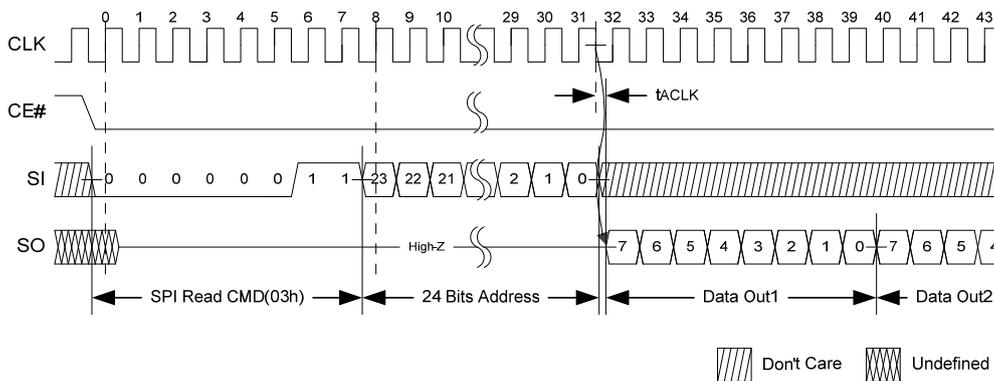
1. SPI Mode : Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

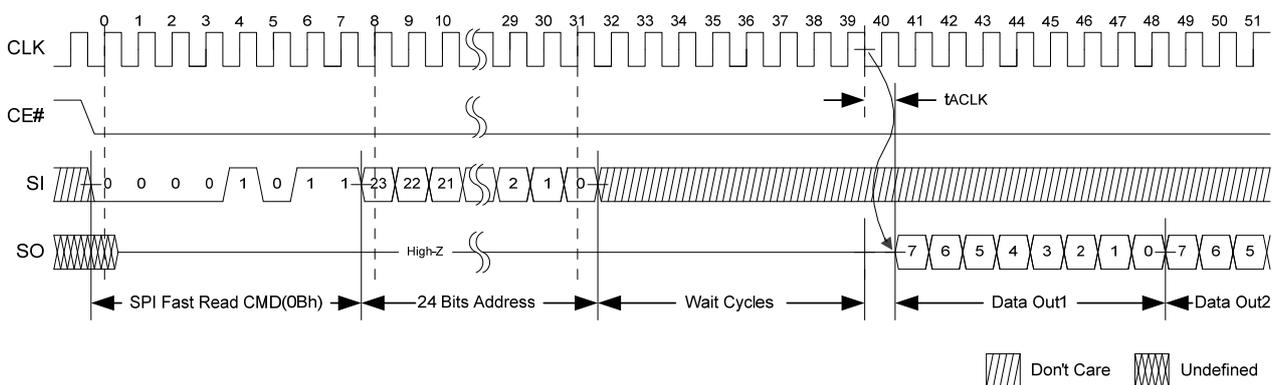
SPI Reads can be done in three ways:

- 1.1. 03h : Serial CMD, Serial IO, slow frequency
- 1.2. 0Bh : Serial CMD, Serial IO, fast frequency
- 1.3. EBh : Serial CMD, Quad IO, fast frequency

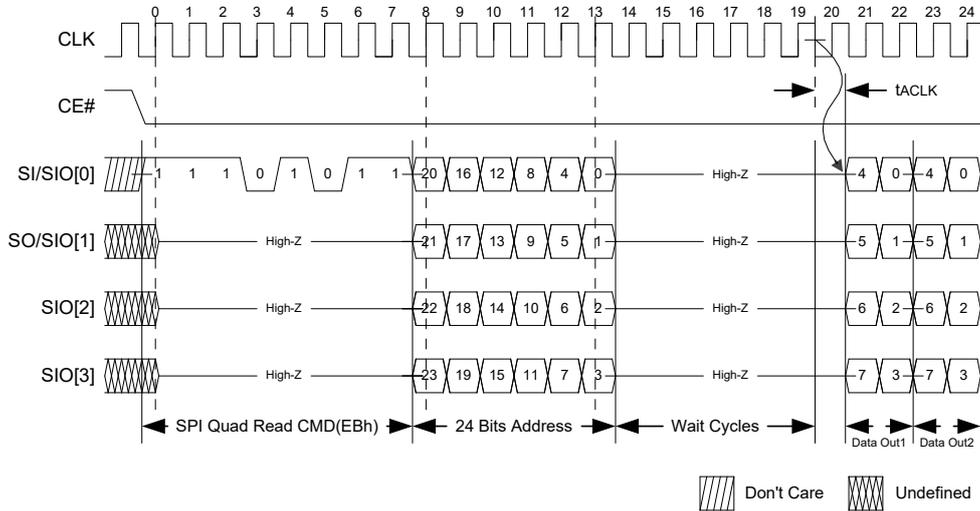
1.1 SPI Read(03h)



1.2 SPI Fast Read(0Bh)



1.3 SPI Quad Read(EBh)

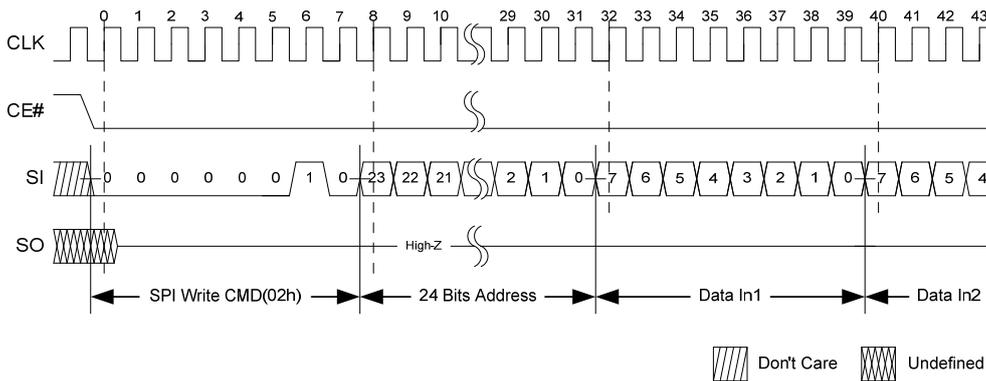


2. SPI Mode : Write Operations

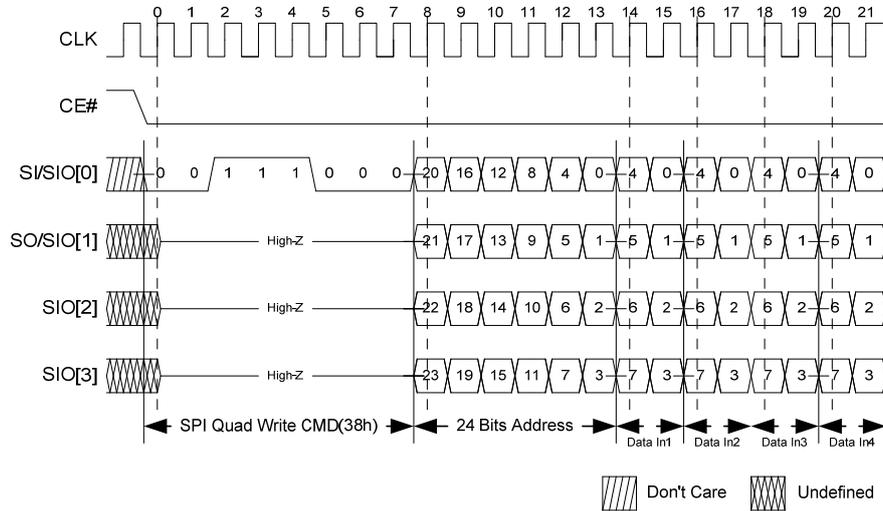
SPI Writes can be done in two ways:

- 2.1 02h : Serial CMD, Serial IO, slow frequency
- 2.1 38h : Serial CMD, Quad IO, fast frequency

2.1 SPI Write(02h)

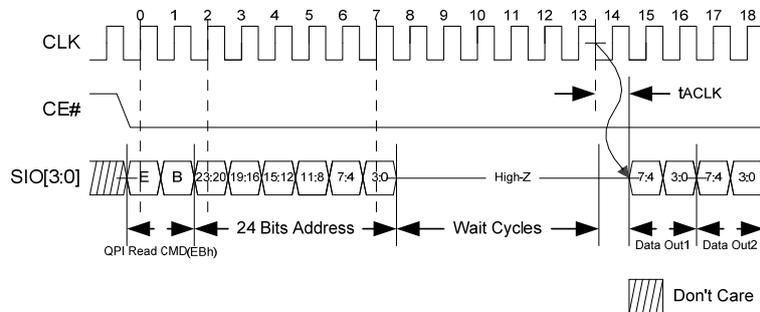


2.2 SPI Quad Write(38h)

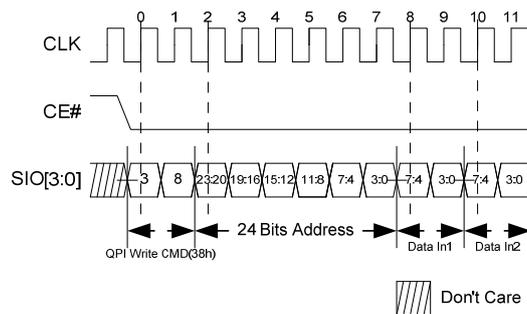


QPI MODE OPERATIONS

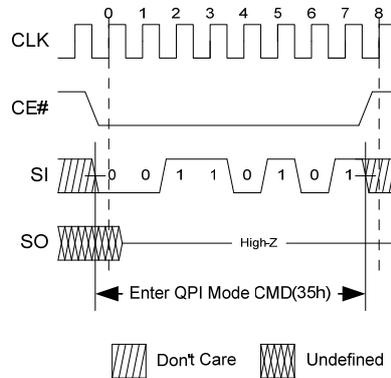
3. QPI Mode : Read Operations (EBh)



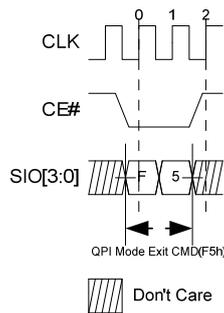
4. QPI Mode : Write Operations(38h or 02h)



5. QPI Mode : Enable Operation(35h)



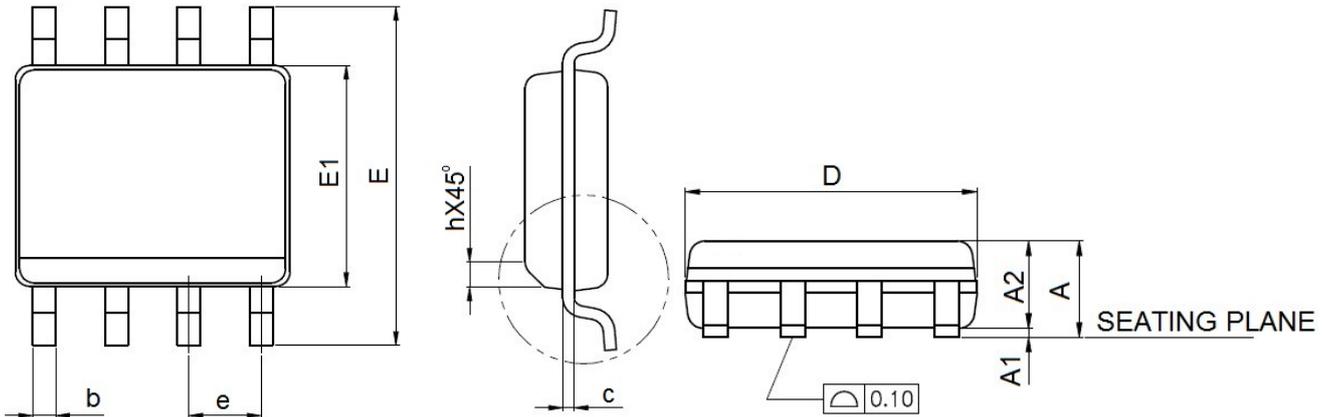
6. QPI Mode : Quit Operation(F5h)





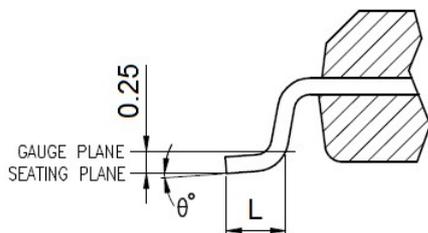
PACKAGE OUTLINE DIMENSION

8-pin 150mil SOP Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	STANDARD	
	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8



NOTES:

1. JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
MS-012 BA REV.F (THERMAL)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.



ORDERING INFORMATION

Package Type	Maximum Clock Rate(MHz)	Temperature Range(°C)	Packing Type	Lyontek Item No.
8-Pin 150mil SOP	100	-25°C~85°C	Tube	LY68S3200SL
			Tape Reel	LY68S3200SLT



Lyontek Inc.

LY68S3200

Rev. 1.2

32M Bits Serial Pseudo-SRAM with SPI and QPI

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