

## $\eta$ -Balance™ Current Mode PWM Controller

**FEATURES**

- ◆ **Less than 75mW Standby Power**
- ◆ **Programmable OLP Debounce Time**
- ◆ **Proprietary  $\eta$ -Balance™ Control to Boost Light Load Efficiency**
- ◆ **Proprietary “Zero OCP/OPP Recovery Gap” Control**
- ◆ **Proprietary “Audio Noise Free OCP Compensation”**
- ◆ **Fixed 65KHz Switching Frequency**
- ◆ **Built-in Frequency Shuffling**
- ◆ **Built-in Soft Start Function**
- ◆ **Frequency Reduction and Burst Mode Control for Energy Saving**
- ◆ **Built-in Synchronous Slope Compensation**
- ◆ **Cycle-by-Cycle Current Limiting**
- ◆ **Built-in Leading Edge Blanking (LEB)**
- ◆ **Current Mode Control**
- ◆ **Pin Floating Protection**
- ◆ **Very Low Startup Current**
- ◆ **Audio Noise Free Operation**
- ◆ **VDD UVLO, OVP & Clamp**

**APPLICATIONS**

Offline AC/DC Flyback Converter for

- ◆ AC/DC Adaptors
- ◆ Open-frame SMPS

**GENERAL DESCRIPTION**

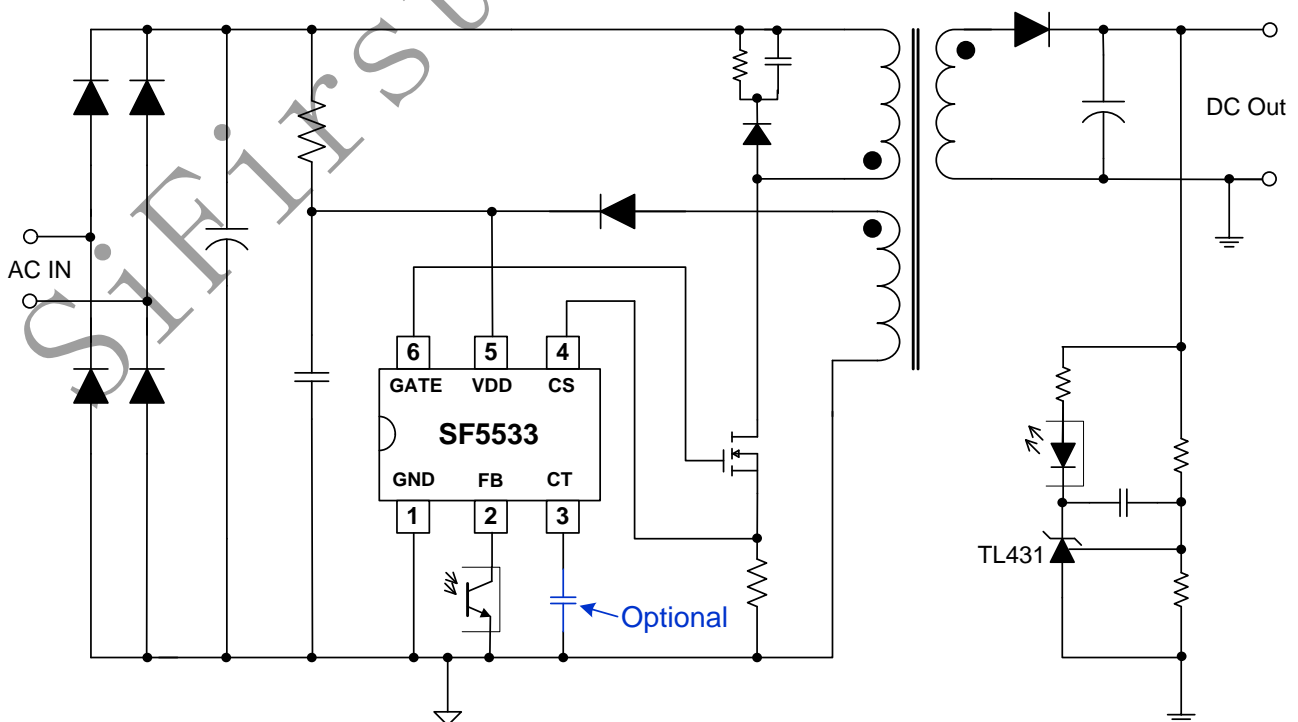
SF5533 is a high performance, high efficiency, highly integrated current mode PWM controller for offline flyback converter applications. The OLP debounce time can be programmed in SF5533.

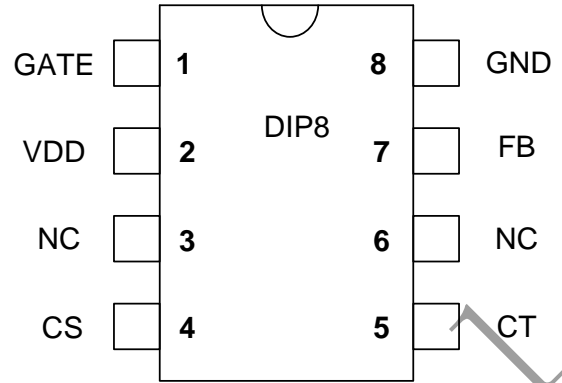
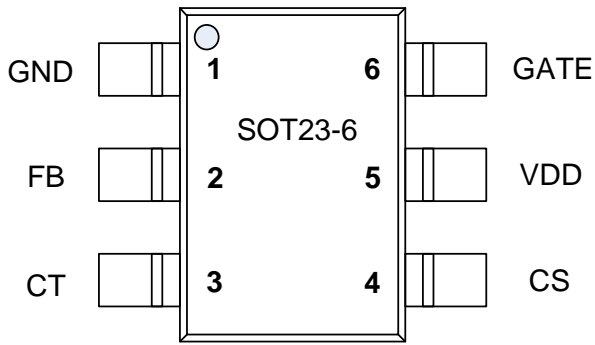
In SF5533, PWM switching frequency with shuffling is fixed to 65KHz and is trimmed to tight range. When the output power demands decrease, the IC decreases switching frequency based on the proprietary  $\eta$ -Balance™ control to boost power conversion efficiency at the light load. When output power falls below a given value, the IC enters into burst mode and can achieve less than 75mW no load power.

The IC can achieve “Zero OCP/OPP Recovery Gap” using SiFirst’s proprietary control algorithm. SF5533 also has built in proprietary “Audio Noise Free OCP Compensation”, which can achieve constant power limiting and can achieve audio noise operation at heavy loading when line input is around 90VAC.

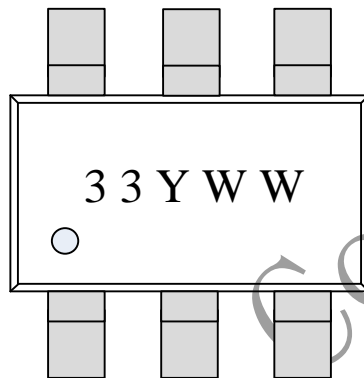
SF5533 integrates functions and protections of Under Voltage Lockout (UVLO), VDD Over Voltage Protection (OVP), Cycle-by-cycle Current Limiting (OCP), Pins Floating Protection, Over Load Protection (OLP), Gate Clamping, VDD Clamping, Leading Edge Blanking (LEB), Soft Start, etc.

SF5533 is available in SOT23-6 and DIP-8 packages.

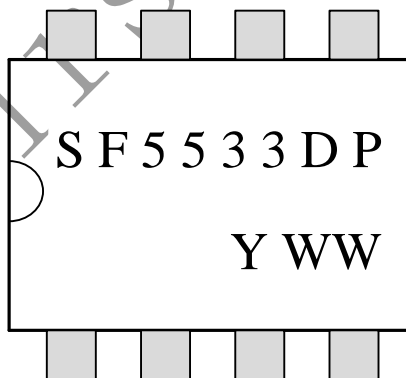
**TYPICAL APPLICATION**


**Pin Configuration**

**Ordering Information**

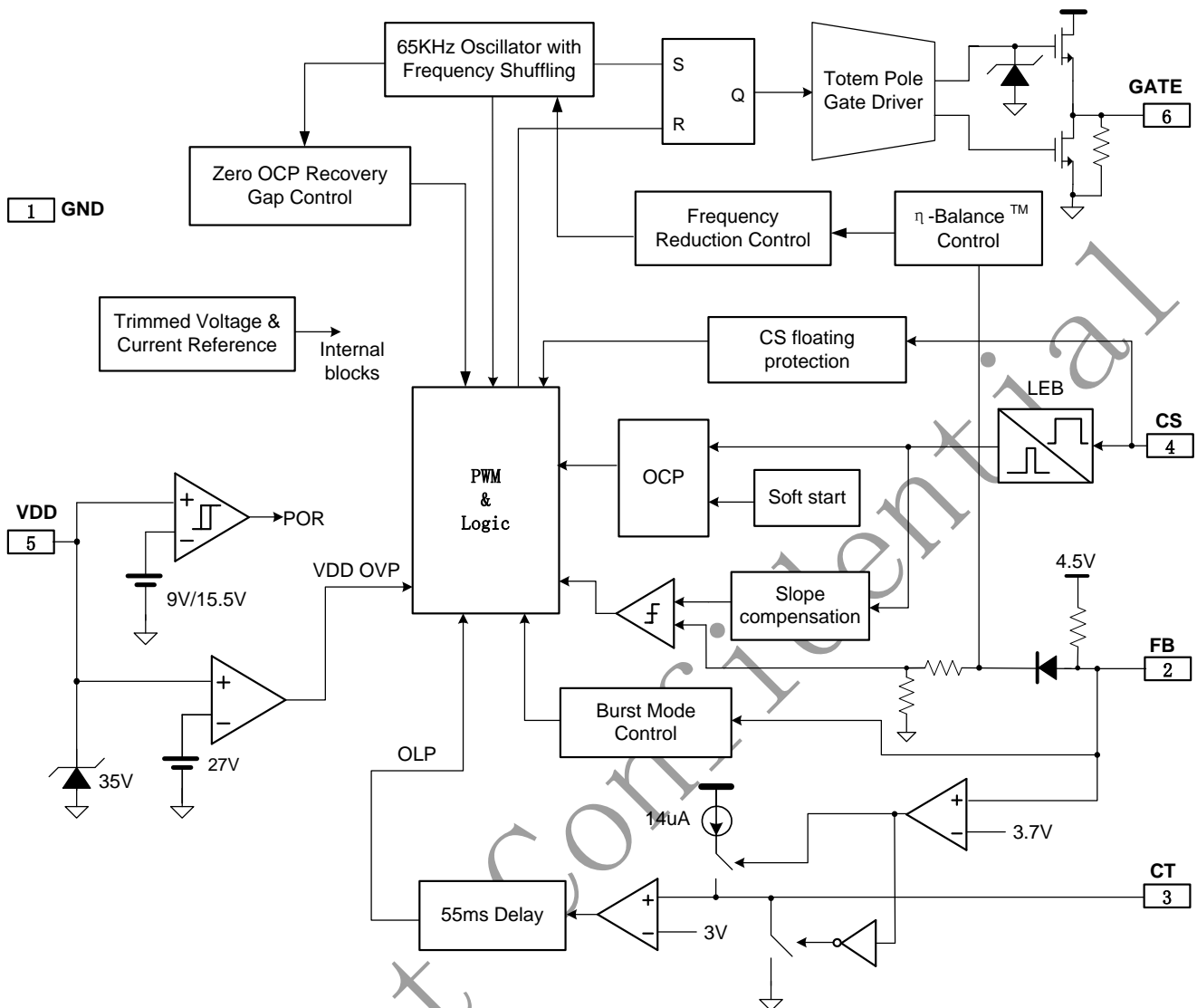
Part Number	Top Mark	Package		Tape & Reel
SF5533LGT	.33YWW	SOT26	Green	Yes
SF5533DP	SF5533DP	DIP8	RoHS	

**Marking Information**


33: Part number SF5533  
YWW: Year&Week Code



YWW: Year&Week code

**Block Diagram**

**Pin Description**

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4.
3	CT	I	Pin for program OLP debounce time. If this pin is floating, the OLP time is 55ms. If an external capacitor is connected between CT and GND, the OLP debounce time can be programmable.
4	CS	I	Current sense input pin.
5	VDD	P	IC power supply pin.
6	GATE	O	Totem-pole gate driver output to drive the external MOSFET.

**Absolute Maximum Ratings (Note 1)**

Parameter	Value	Unit
VDD DC Supply Voltage	35	V
VDD DC Clamp Current	10	mA
GATE pin	20	V

FB, RT, CS voltage range	-0.3 to 7	V
Package Thermal Resistance (SOT-26)	250	°C/W
Package Thermal Resistance (DIP-8)	90	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

**Recommended Operation Conditions** (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	10 to 25	V
Operating Frequency	50 to 130	KHz
Operating Ambient Temperature	-40 to 85	°C

**ELECTRICAL CHARACTERISTICS**

 (T<sub>A</sub> = 25°C, RT=100K ohm, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Supply Voltage Section (VDD Pin)</b>						
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14.5	15.5	16.5	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8	9	9.8	V
I_Startup	VDD Start up Current	VDD =UVLO(ON)-1V, Measure current into VDD		3	15	uA
I_VDD_Op	Operation Current	V <sub>FB</sub> =3V		2.0	3.5	mA
VDD_OVP	VDD Over Voltage Protection trigger		25	27	29	V
V <sub>DD</sub> _Clamp	VDD Zener Clamp Voltage	I(V <sub>DD</sub> ) = 10mA		35.5		V
T_Softstart	Soft Start Time			4		mSec
<b>Feedback Input Section(FB Pin)</b>						
V <sub>FB</sub> _Open	FB Open Voltage		4.1	4.5	5	V
I <sub>FB</sub> _Short	FB short circuit current	Short FB pin to GND, measure current	0.22	0.33	0.45	mA
A <sub>VCS</sub>	PWM Input Gain	$\Delta V_{FB} / \Delta V_{CS}$		1.6		V/V
V <sub>FB</sub> _min_duty	FB under voltage gate clock is off.			1.0		V
V <sub>TH</sub> _PL	Power Limiting FB Threshold Voltage			3.7		V
T <sub>D</sub> _PL_min	Minimum Power limiting Debounce Time	CT Pin is floating		55		mSec
Z <sub>FB</sub> _IN	Input Impedance			14		Kohm
<b>Current Sense Input Section (CS Pin)</b>						
V <sub>th</sub> _OC_min	Internal current limiting threshold	Zero duty cycle	0.70	0.75	0.80	V
V <sub>th</sub> _OC_max	Internal current limiting threshold			1.0		V
T <sub>blanking</sub>	SENSE Input Leading Edge Blanking Time			250		nSec
T <sub>D</sub> _OC	Over Current Detection and Control Delay	GATE=1nF		65		nSec
<b>Oscillator Section</b>						
F <sub>osc</sub>	Normal Oscillation		60	65	70	KHZ

	Frequency					
$\Delta F(\text{shuffle})/F_{osc}$	Frequency shuffling range	Note 8	-4		4	%
$\Delta f_{Temp}$	Frequency Temperature Stability	-20°C to 100 °C (Note 7)		5		%
$\Delta f_{VDD}$	Frequency Voltage Stability	VDD = 12-25V,		5		%
Duty_max	Maximum Duty cycle		75	80	85	%
F_BM	Burst Mode Base Frequency			22		KHZ
<b>OLP Debounce Program Section (CT Pin)</b>						
I_CT	Output Current of CT Pin		10	14	18	uA
V <sub>TH_CT</sub>	Comparator threshold for OLP debounce time			3		V
<b>Gate Drive Output (GATE Pin)</b>						
VOL	Output Low Level	I <sub>o</sub> = 20 mA (sink)			1	V
VOH	Output High Level	I <sub>o</sub> = 20 mA (source)	7.5			V
VG_Clamp	Output Clamp Voltage Level	VDD=24V		16		V
T_r	Output Rising Time	GATE = 1nF		150		nSec
T_f	Output Falling Time	GATE = 1nF		60		nSec

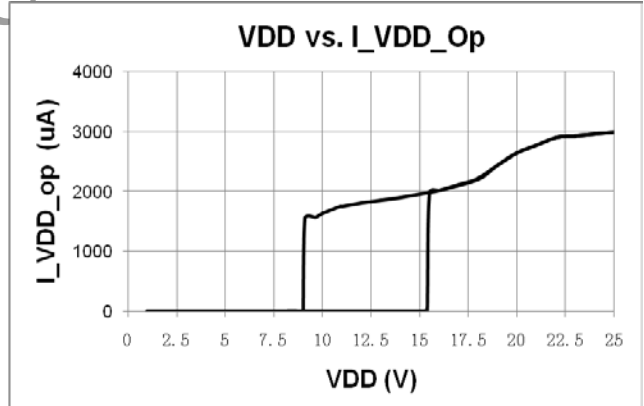
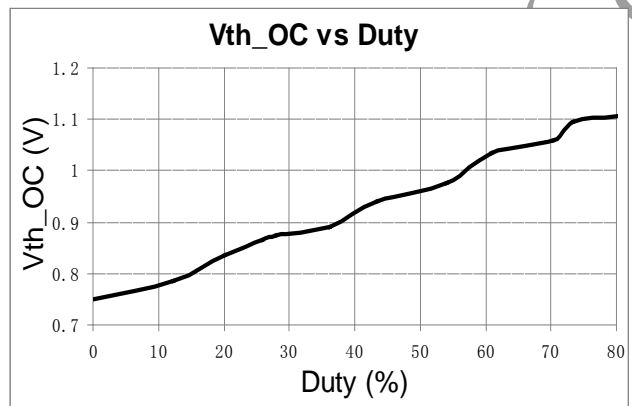
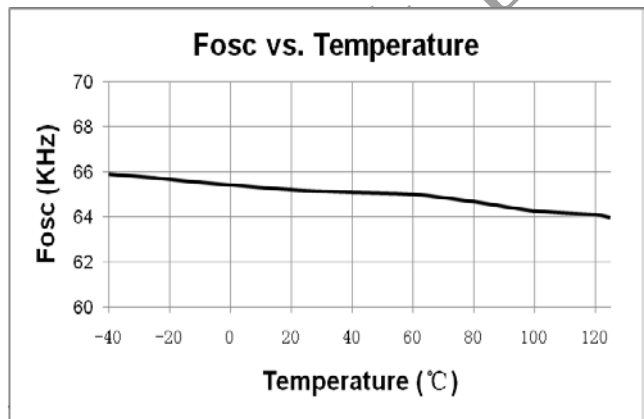
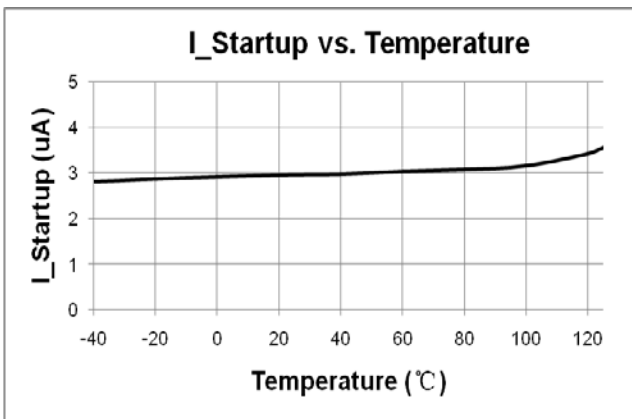
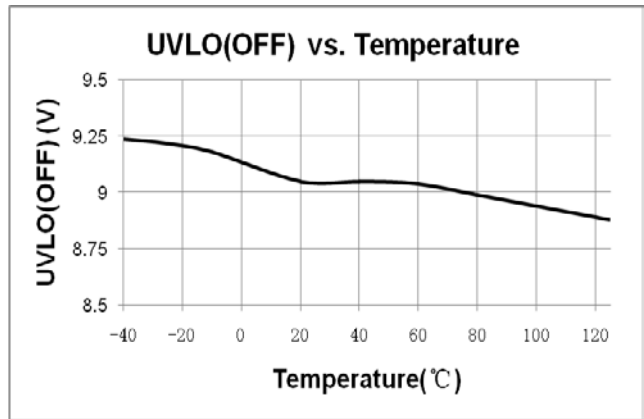
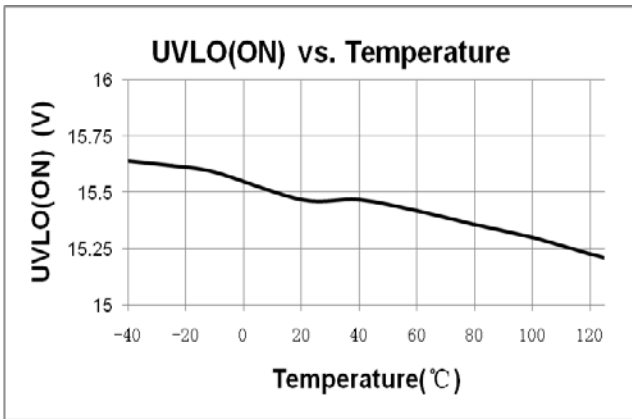
**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** The device is not guaranteed to function outside its operating conditions.

**Note 3.** The OLP debounce time is proportional to the period of switching cycle.

**Note 4.** Guaranteed by design.

CHARACTERIZATION PLOTS



## OPERATION DESCRIPTION

SF5533 is a high performance, highly efficiency current mode PWM controller for offline flyback converter applications. The built-in proprietary “Efficiency Equalization” with high level protection features improves the SMPS reliability and performance without increasing the system cost.

### ◆ UVLO and Startup Operation

Fig.1 shows a typical startup circuit. Before the IC begins switching operation, it consumes only startup current (typically 3uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 15.5V(typical), SF5533 begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The selection of Rst and Cdd should be a trade off between the power loss and startup time.

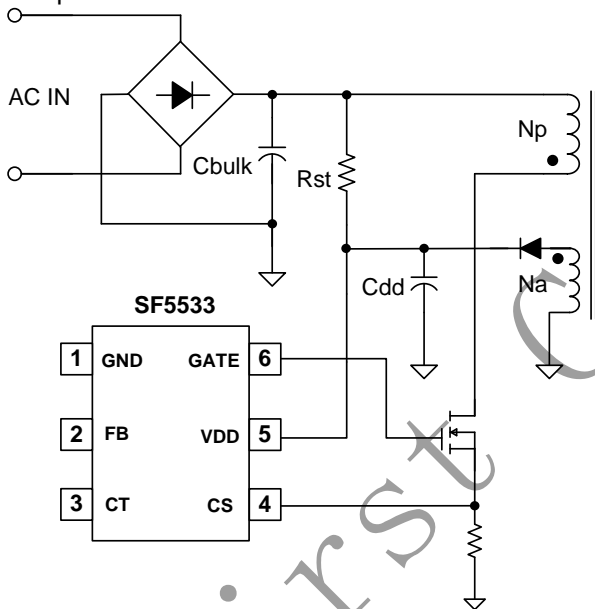


Fig.1

### ◆ Low Operating Current

The operating current in SF5533 is as small as 2mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

### ◆ Soft Start

SF5533 features an internal 4ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

### ◆ “Zero OCP/OPP Recovery Gap” Control

The definition of OCP or OPP recovery gap of a power adaptor is illustrated in Fig.2. At T0, assuming an adaptor is at full loading mode. If the loading keeps increasing, then the system will output maximum power P\_opp, which will trigger OPP protection at the same time. After the OPP protection is triggered, usually the system will enter into the auto-recovery mode, in burst manner. If the system power demand decreases below P\_recovery, then system will enter into normal mode again, as shown in Fig.2. The difference between P\_opp and P\_recovery is defined as “**OPP Recovery Gap**”, which can cause system startup failure especially in 90VAC full load startup.

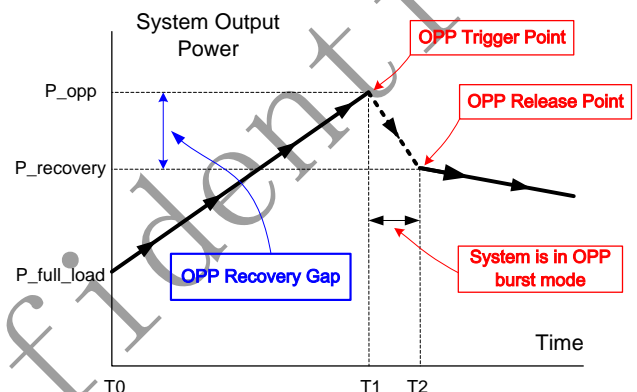


Fig.2

SF5533 can achieve “**Zero OCP/OPP Recovery Gap**” in the whole universal AC input range using SiFirst’s proprietary control algorithm.

### ◆ Oscillator with Frequency Shuffling

PWM switching frequency in SF5533 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, SF5533 operates the system with ±4% frequency shuffling around setting frequency.

### ◆ Synchronous Slope Compensation

In SF5533, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

### ◆ Programmable OLP Debounce Time

Connecting a capacitor C<sub>CT</sub> from CT pin to GND according to the equation below to program the OLP debounce time. In OLP debounce time, an internal current (14uA, typical) charges C<sub>CT</sub>, when CT pin voltage reaches 3V, an internal 55ms debounce is triggered. When internal 55ms debounce time is over, the OLP protection is triggered and the system will enter into auto recovery protection mode.

$$T_{OLP\_debounce} = \frac{3V * C_{CT}}{14\mu A} + 55ms$$

If CT pin is floating, the OLP debounce time is 55ms. Otherwise, the OLP debounce time can be programmed by CT capacitor.

◆ **Proprietary  $\eta$ -Balance™ Control**

The efficiency requirement of power conversion is becoming tighter than before. These new energy standards focus on the average efficiency of the whole loading range. Therefore, the light load efficiency is becoming more and more important.

In SF5533, a proprietary  $\eta$ -Balance™ control is integrated to boost the light load efficiency. As shown in Fig.3, when the loading becomes light, the IC will reduce the PWM switching frequency according to an optimized frequency reduction curve. The specific frequency reduction curve and the power at a frequency are determined by the output of  $\eta$ -Balance™ control. For example, P1 is at full load, P2 is at 75% full load, P3 and P4 are 50% and 25% full load respectively. The  $\eta$ -Balance™ control can provide higher average efficiency than conventional frequency reduction technique, as illustrated in Fig.3

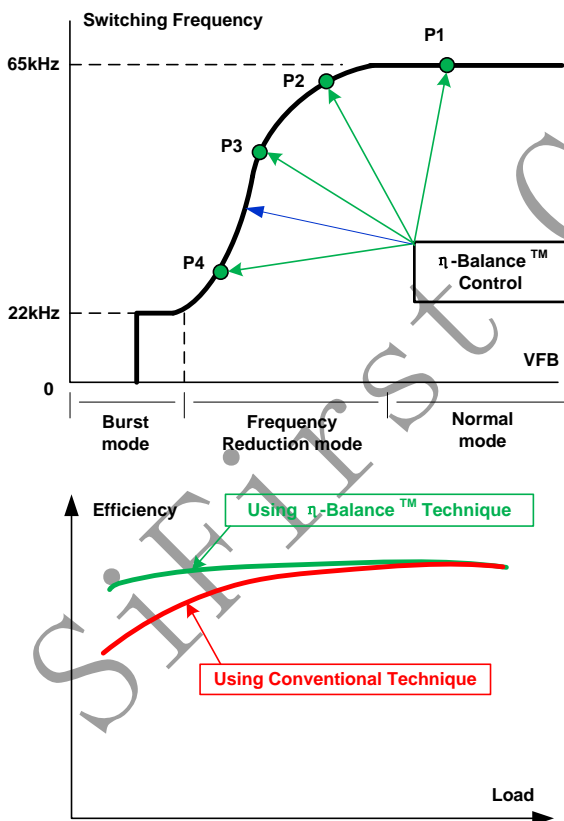


Fig.3

◆ **Leading Edge Blanking (LEB)**

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To

avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

◆ **Burst Mode Control**

When the loading is very small, the system enters into burst mode. When VFB drops below  $V_{skip}$ , SF5533 will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above  $V_{skip}$ , switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

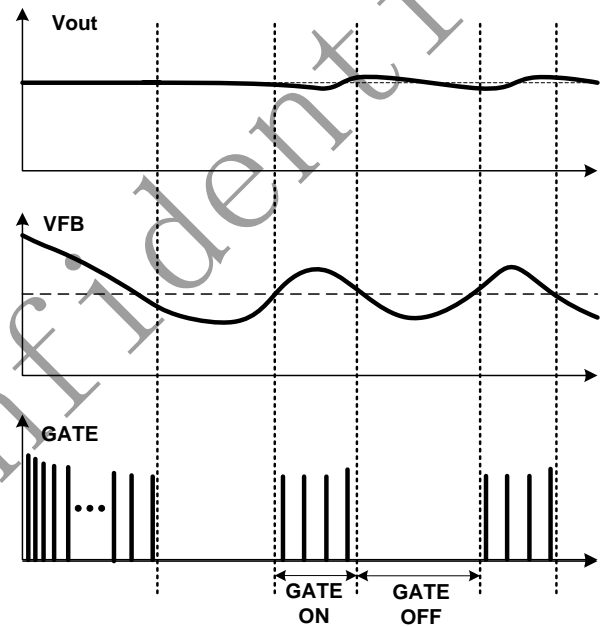


Fig.4

◆ **Audio Noise Free OCP Compensation**

Conventional OCP compensation may have audio noise issue when AC line is around 90VAC and heavy loading. As shown in Fig.5, when increasing from full load to hiccup load at 90VAC, VFB may oscillate in conventional OCP compensation system. The oscillation can generate large audio noise. In SF5533, a proprietary “Audio Noise Free OCP Compensation” is integrated, which can achieve constant power limiting with no audio noise generated.



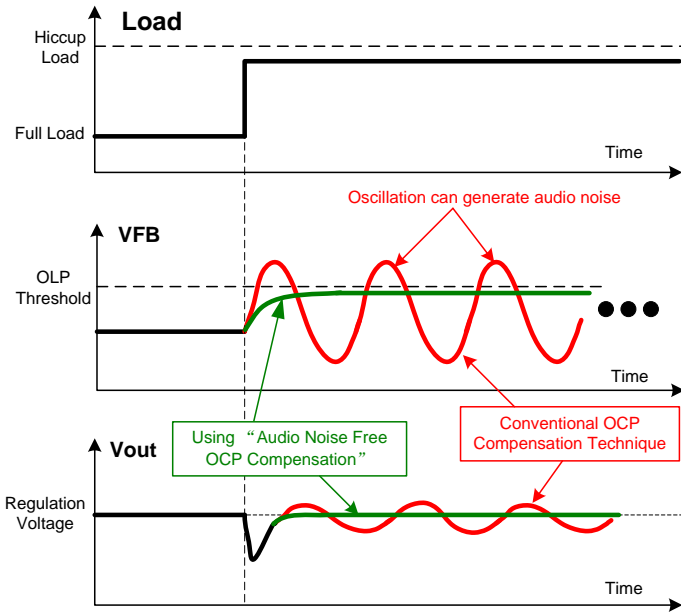


Fig.5

◆ **Auto Recovery Mode Protection**

As shown in Fig.6, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to UVLO(OFF) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

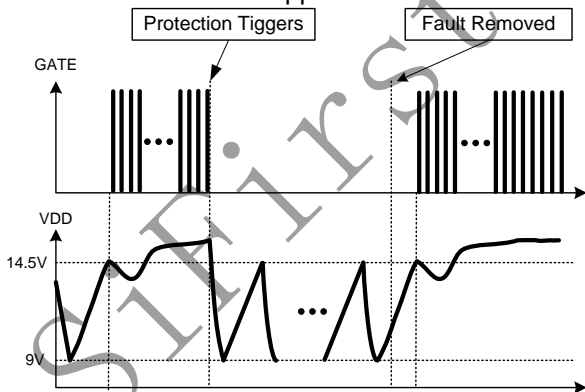


Fig.6

◆ **Over Load Protection (OLP) / Over Current Protection (OCP) / Over Power**

**Protection (OPP) / Open Loop Protection (OLP)**

When OLP/OCP/OPP/Open Loop occurs, a fault is detected. If this fault is present for more than  $T_{OLP\_debounce}$ , the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above, as shown in Fig.7. The  $T_{OLP\_debounce}$  debounce time is to prevent the false trigger from the power-on and turn-off transient.

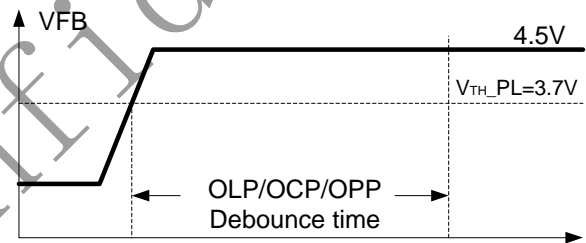
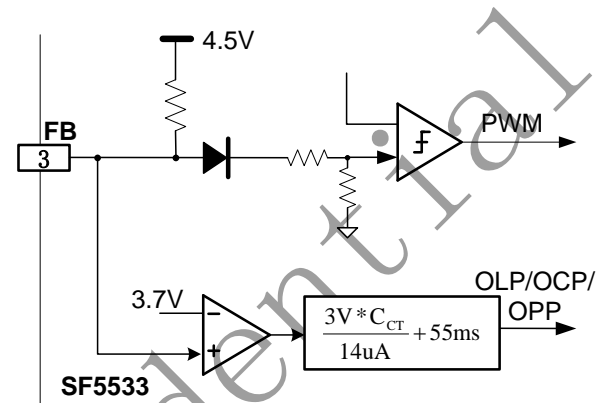


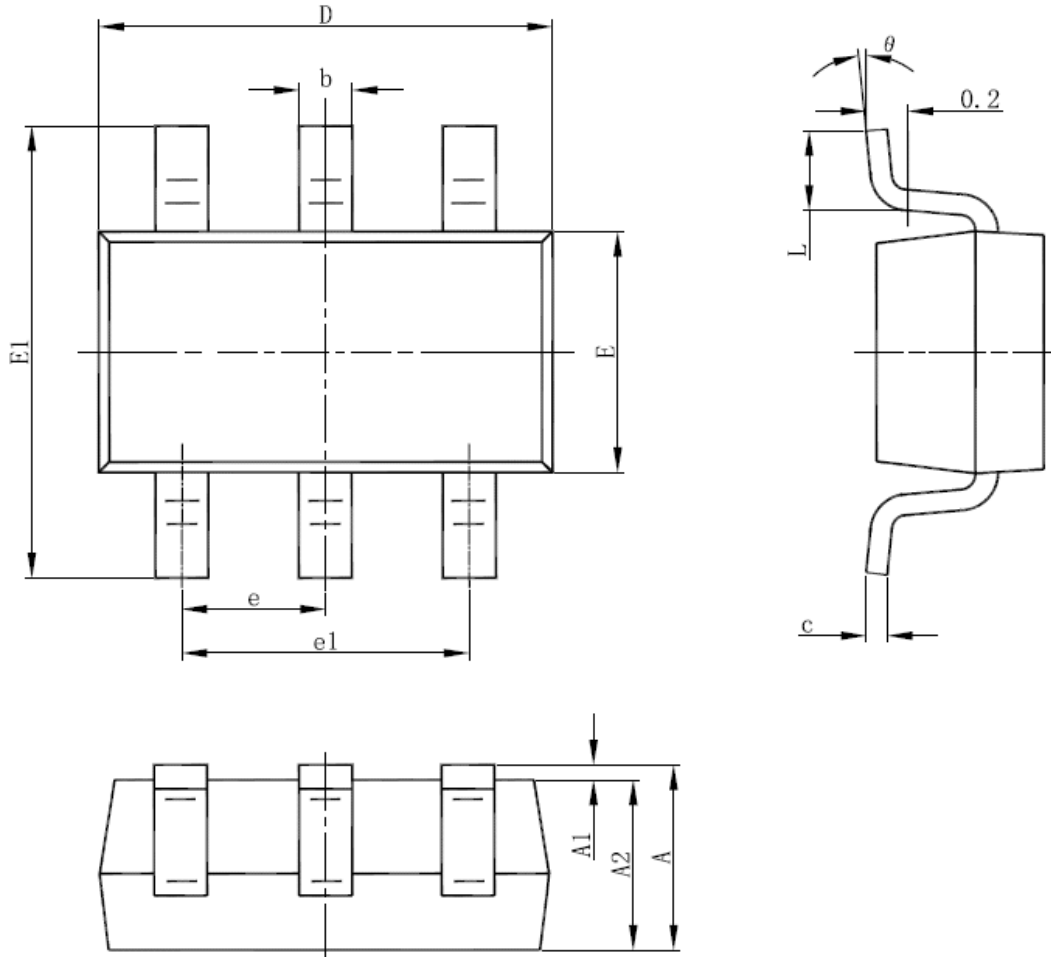
Fig.7

◆ **Soft Gate Drive**

SF5533 has a fast totem-pole gate driver with 300mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

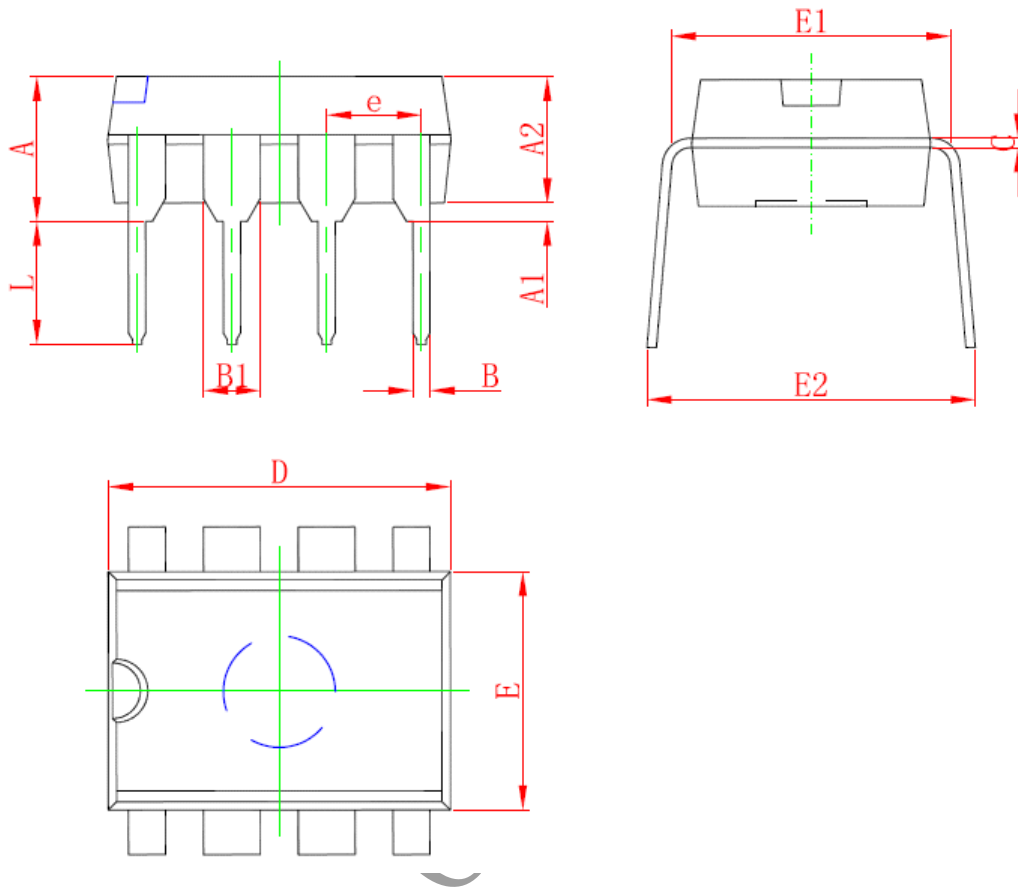
**PACKAGE MECHANICAL DATA**

**SOT-23-6L PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°

**DIP8 PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.06 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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