# 2nd Generation Quasi-Resonant (QR-II™ ) PWM Controller with Brownout Protection

## FEATURES

◆ **Easily Meet EPS Level 6**
◆ **AC Brownout Protection (BOP)**
◆ **Proprietary QR-II™ Technology:**
  ●Digital Anti-jitter for Audio Noise Free Operation
  ● Digital Frequency Foldback
  ● Digital Frequency Jittering for Better EMI
◆ **Less than 100mW Standby Power**
◆ **Multi-Mode Operation for High Efficiency**
◆ **12.7us Maximum On Time**
◆ **80KHz Maximum Frequency Limit**
◆ **52KHz Frequency Low Clamping in QR Mode**
◆ **65% Maximum Duty Cycle**
◆ **Adaptive Slope Compensation for CCM Mode**
◆ **Built-in Soft Start Function**
◆ **Pin Floating Protection**
◆ **Built-in Synchronous Slope Compensation**
◆ **Cycle-by-Cycle Current Limiting**
◆ **Leading Edge Blanking (LEB)**
◆ **Constant Power Limiting**
◆ **VDD UVLO, OVP & Clamp**

## APPLICATIONS

**Offline AC/DC Flyback Converter for**
◆ **AC/DC Adaptors**
◆ **SMPS Power Supply**

## GENERAL DESCRIPTION

SF5773S is a high performance, 2nd Generation Quasi-Resonant (QR-II™) PWM controller for offline flyback power converter applications. The built-in proprietary **QR-II™** technology with high level protection features improves the SMPS reliability and performance.

In SF5773S, the "**Digital Anti-Jitter**" function can automatically select and lock a valley at a given loading, which can achieve audio noise free operation. On the other hand, the "**Digital Frequency Jittering**" function makes the system have superior EMI performance than conventional QR system.

SF5773S is a multi mode controller. When full loadings, the IC works in CCM mode or QR mode based on the AC line input. When the loading goes low, the IC enters into "**Digital Frequency Foldback**" mode to boost power conversion efficiency. When the output power is very small, the IC enters into burst mode and can achieve less than 100mW no load power.

SF5773S integrates functions and protections of Under Voltage Lockout (UVLO), VCC Over Voltage Protection (OVP), Output Over Voltage Protection (Output OVP), Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, Over Load Protection (OLP), AC Brownout Protection, Soft Start, VCC Clamping, Gate Clamping, etc. In SF5773S, the protection functions are auto-recovery mode protection.
 SF5773S is available in SOT23-6 package.

## TYPICAL APPLICATION

# SF5773S

## Pin Configuration

```
GND  1      6  GATE
          SOT23-6
FB   2      5  VDD

DEM  3      4  CS
```
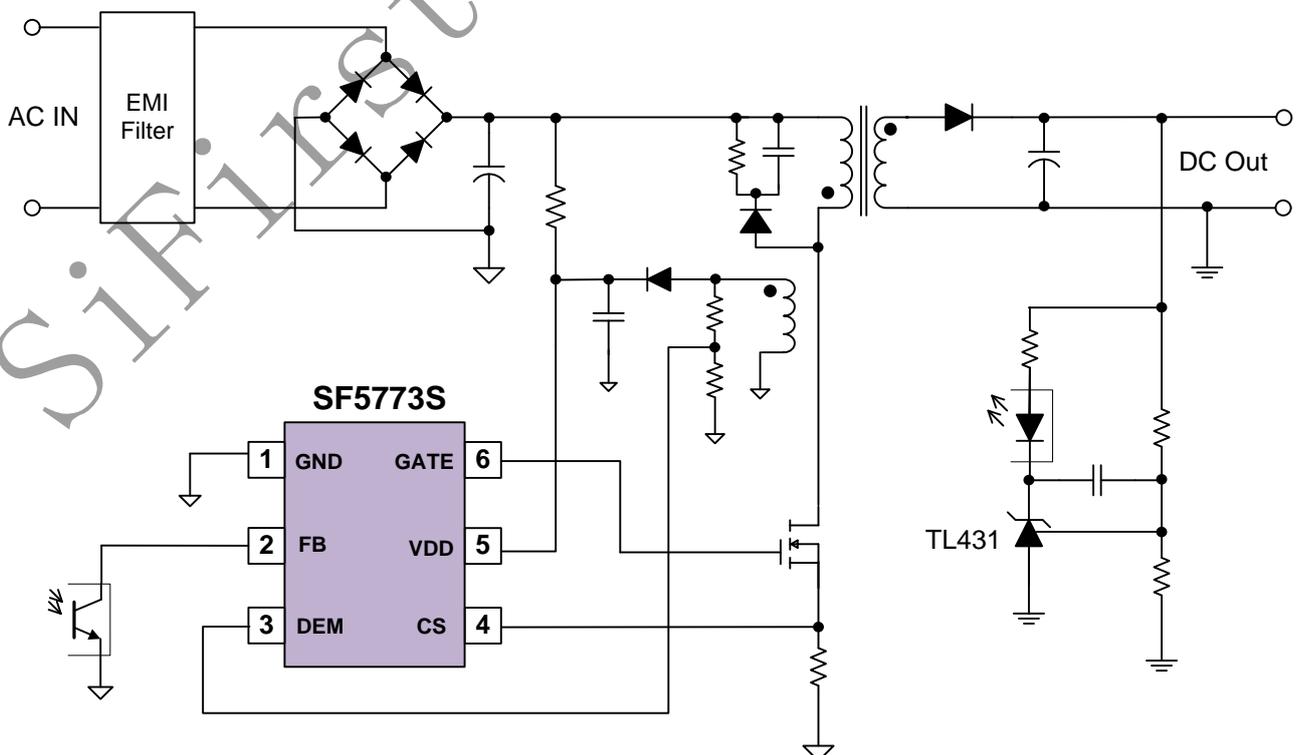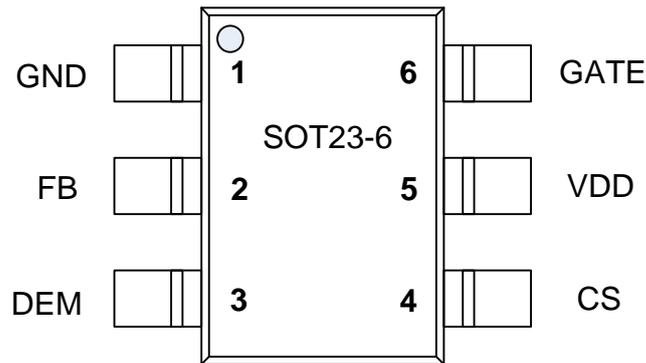
## Ordering Information

| Part Number | Top Mark | Package | | Tape & Reel |
|---|---|---|---|---|
| SF5773SLGT | .73SYW | SOT26 | Green | Yes |

## Marking Information
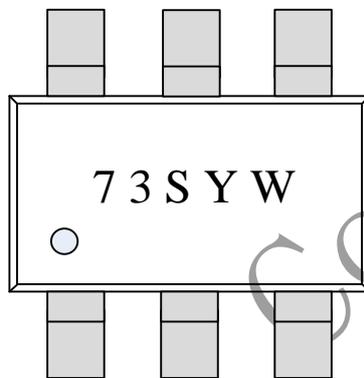
73SYW

Dot: Pin1 Mark
73S:Part number SF5773S
YW: Year&Week Code

## Pin Description

| Pin Num | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | GND | P | IC ground pin. |
| 2 | FB | I | Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is generated by this pin voltage and the current sense signal at Pin 4. |
| 3 | DEM | I | Transformer core demagnetization detection pin. This pin is also used for output over voltage protection (Output OVP) and AC Brownout Protection (BOP). |
| 4 | CS | I | Current sense input pin. |
| 5 | VDD | P | IC power supply pin. |
| 6 | GATE | O | Totem-pole gate driver output to drive the external MOSFET. |

## Block Diagram
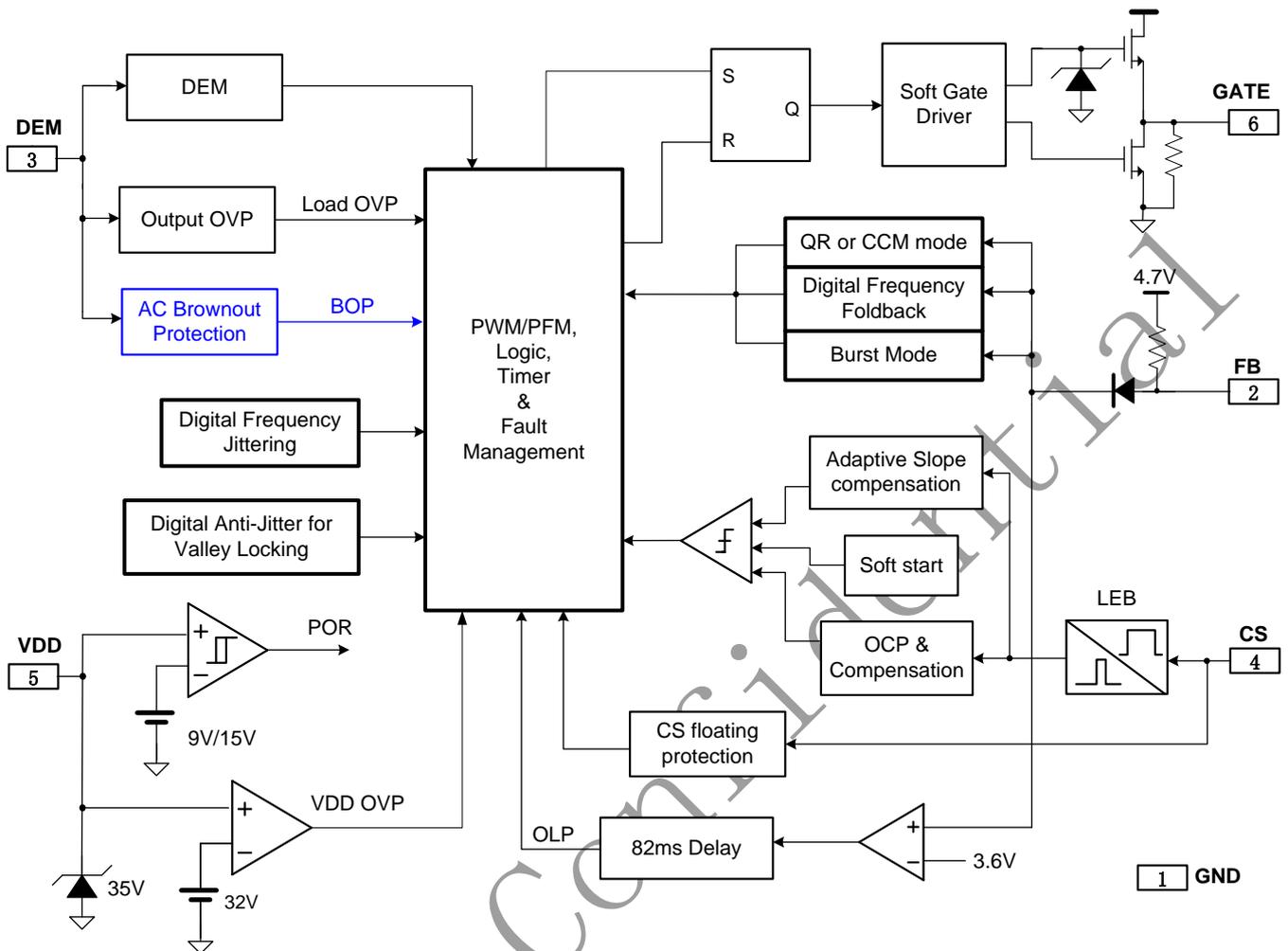


## Absolute Maximum Ratings (Note 1)

| Parameter | Value | Unit |
|---|---|---|
| VDD DC Supply Voltage | 35 | V |
| VCC DC Clamp Current | 10 | mA |
| DEM Voltage Range | -0.7 to 6 | V |
| FB, CS Voltage Range | -0.3 to 7 | V |
| Package Thermal Resistance (SOT-26) | 250 | $^{o}$C/W |
| Maximum Junction Temperature | 150 | $^{o}$C |
| Operating Temperature Range | -40 to 85 | $^{o}$C |
| Storage Temperature Range | -65 to 150 | $^{o}$C |
| Lead Temperature (Soldering, 10sec.) | 260 | $^{o}$C |
| ESD Capability, HBM (Human Body Model) | 3 | kV |
| ESD Capability, MM (Machine Model) | 250 | V |

## Recommended Operation Conditions (Note 2)

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage, VDD | 11 to 29 | V |
| Operating Ambient Temperature | -40 to 85 | $^{o}$C |

# ELECTRICAL CHARACTERISTICS

($T_A = 25^O$C, VDD=18V, if not otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage Section (VDD Pin)** | | | | | | |
| I_Startup | VDD Start up Current | | | 5 | 20 | uA |
| I_VDD_Op | Operation Current | $V_{FB}$=3.2V, GATE=1nF | | 1.8 | 3.5 | mA |
| UVLO(ON) | VDD Under Voltage Lockout Exit (Startup) | | 14 | 15 | 16 | V |
| UVLO(OFF) | VDD Under Voltage Lockout Enter | | 8 | 9 | 10 | V |
| VDD_OVP | VDD Over Voltage Protection trigger | | 30 | 32 | 34 | V |
| $V_{DD}$_Clamp | VDD Zener Clamp Voltage | $I(V_{DD})$ = 10mA | 33 | 35 | | V |
| T_Softstart | Soft Start Time | | | 4 | | mSec |
| **Feedback Input Section(FB Pin)** | | | | | | |
| $V_{FB}$_Open | FB Open Voltage | | 4.2 | 4.7 | 5.5 | V |
| $I_{FB}$_Short | FB short circuit current | Short FB pin to GND, measure current | | 0.4 | | mA |
| $A_{VCS}$ | PWM Input Gain | $\Delta V_{FB} / \Delta V_{cs}$ | | 3 | | V/V |
| VFB_foldback | FB under voltage foldback mode is entered | | | 1.6 | | V |
| VFB_min_duty | FB under voltage gate clock is off. | | | 1.1 | | V |
| VFB_PL | Power Limiting FB Threshold Voltage | | | 3.6 | | V |
| $T_D$_PL | Power limiting Debounce Time | Note 3 | | 82 | | mSec |
| $Z_{FB}$_IN | Input Impedance | | | 10 | | Kohm |
| **Current Sense Input Section (CS Pin)** | | | | | | |
| Vth_OC_min | Internal current limiting threshold | Zero duty cycle | 0.44 | 0.45 | 0.46 | V |
| Vth_OC_max | Internal current limiting threshold | | | 0.77 | | V |
| T_blanking | SENSE Input Leading Edge Blanking Time | | | 250 | | nSec |
| $T_D$_OC | Over Current Detection and Control Delay | | | 60 | | nSec |
| **Demagnetization Detection Section (DEM Pin)** | | | | | | |
| $V_{TH}$_DEM | DEM Comparator Threshold Voltage (Negative going edge) | | | 125 | | mV |
| $V_{DEM}$_clamp_H | High clamp voltage | | | 5.8 | | V |
| $V_{DEM}$_clamp_L | Low clamp voltage | | | -0.7 | | V |
| $V_{TH}$_OVP | Output over voltage protection threshold | | | 3.4 | | V |
| $N_{TRUE}$_OVP | Number of subsequent cycles to be true OVP | | | 3 | | Cycle |
| $T_{supp}$ | Suppression of the transformer ringing at start of secondary stroke | Note 4 | | 2.5 | | uSec |
| $T_{DEM\_OUT}$ | Timeout after last Demag Transition | Note 4 | | 5 | | uSec |
| $I_{TH}$_BOP_ON | Brownout Turn-on trip level | | 66.5 | 71.5 | 76.5 | uA |

| ITH_BOP_OFF | Brownout Turn-off trip level | | | 72 | 77 | 82 | uA |
|---|---|---|---|---|---|---|---|
| T_BOP_PL | Brownout Debounce Time | Note 3 | | 25 | 35 | | mSec |
| **Timer Section** | | | | | | | |
| T_counter | Sampling Time for Digital Anti-jitter Function | | | | 40 | | mSec |
| N_counter_max | Maximum Number for Valley Locking | | | | 8 | | |
| F_BM | Burst Mode Base Frequency | | | | 22 | | KHz |
| Duty_max | Maximum Duty cycle | Note 4 | | | 65 | | % |
| Fmax_QR_H | Frequency High Clamp in QR Mode | | | 72 | 80 | 88 | KHz |
| Fmin_QR_L | Frequency Low Clamp in QR Mode | | | 47 | 52 | 57 | KHz |
| ΔF(jitter)/Fsw | Frequency Jittering range | Note 4 | | -4 | | 4 | % |
| Ton_max | Maximum ON Time | | | 11.5 | 12.7 | 14 | us |
| Toff_max | Maximum OFF Time | | | 52 | 57 | 64 | us |
| Toff_min | Minimum OFF Time | Note 4 | | | 2.5 | | uSec |
| **Gate Drive Output (GATE Pin)** | | | | | | | |
| VOL | Output Low Level | Io = 20 mA (sink) | | | | 1 | V |
| VOH | Output High Level | Io = 20 mA (source) | 7.5 | | | | V |
| VG_Clamp | Output Clamp Voltage Level | VDD=24V | | | 16 | | V |
| T_r | Output Rising Time | GATE= 1nF | | | 150 | | nSec |
| T_f | Output Falling Time | GATE= 1nF | | | 60 | | nSec |

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** The device is not guaranteed to function outside its operating conditions.

**Note 3.** The OLP debounce time is proportional to the period of switching cycle.

**Note 4.** Guaranteed by design.

## CHARACTERIZATION PLOTS



UVLO(ON) vs Temperature



UVLO(OFF) vs Temperature



I_VDD_op vs Temperature



VFB_Open vs Temperature



F_QR_clamp_L vs Temperature



Vth_OC_min vs Temperature
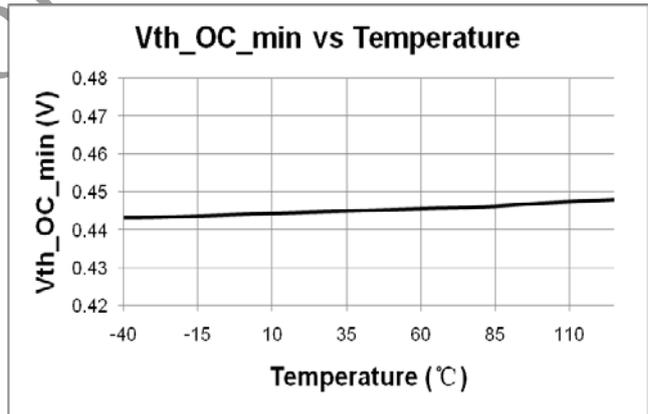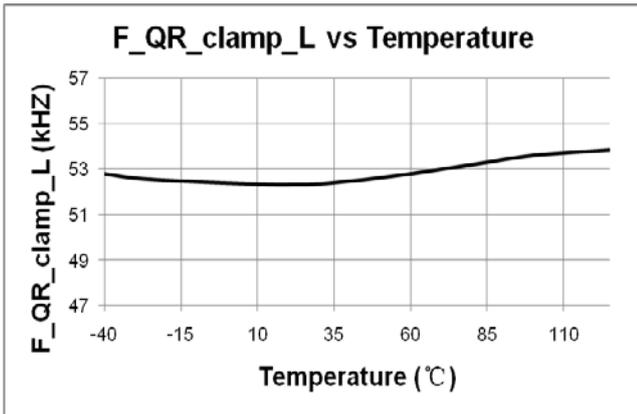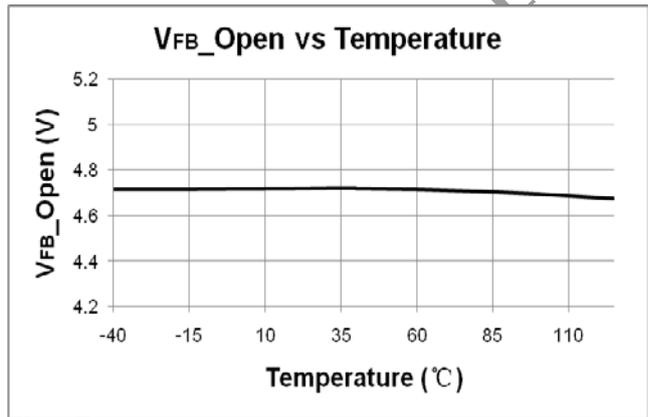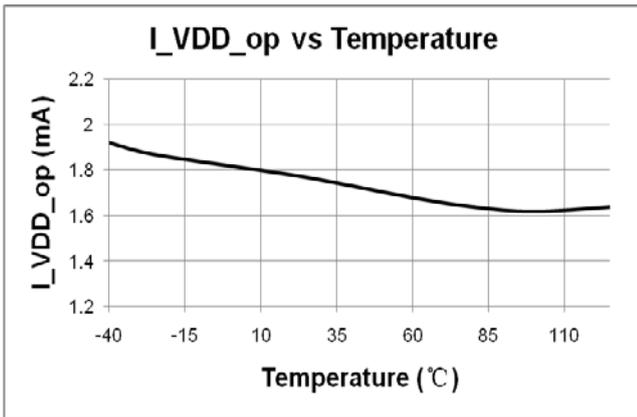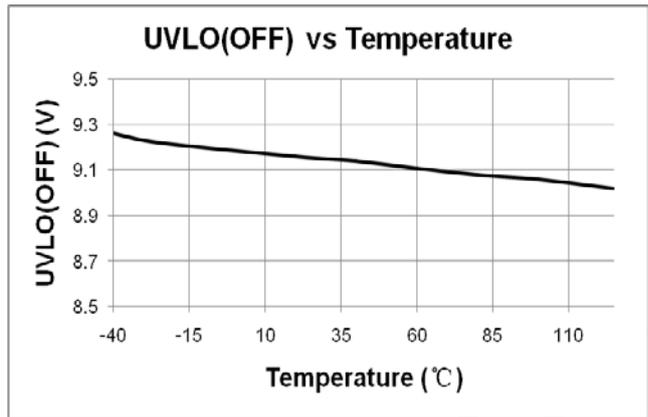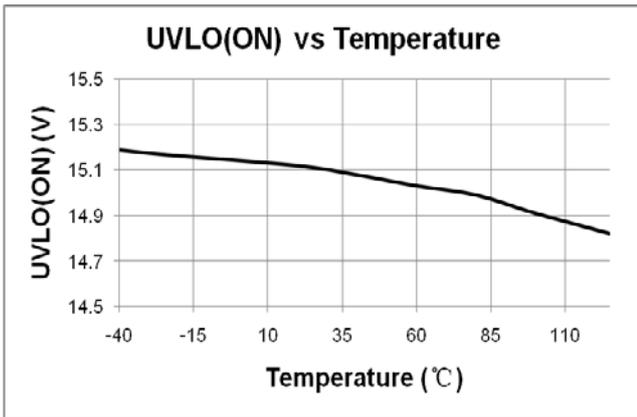
# OPERATION DESCRIPTION

SF5773S is a high performance, 2nd Generation Quasi-Resonant (QR) PWM controller for offline flyback power converter applications. The built-in proprietary **QR-II[TM]** technology with high level protection features improves the SMPS reliability and performance without increasing the system cost.

## ◆ UVLO and Startup Operation

Fig.1 shows a typical startup circuit. Before the IC begins switching operation, it consumes only startup current (typically 5uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 15V(typical), SF5773S begins switching and the IC current consumed increased to 1.8mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The selection of Rst and Cdd should be a trade off between the power loss and startup time.
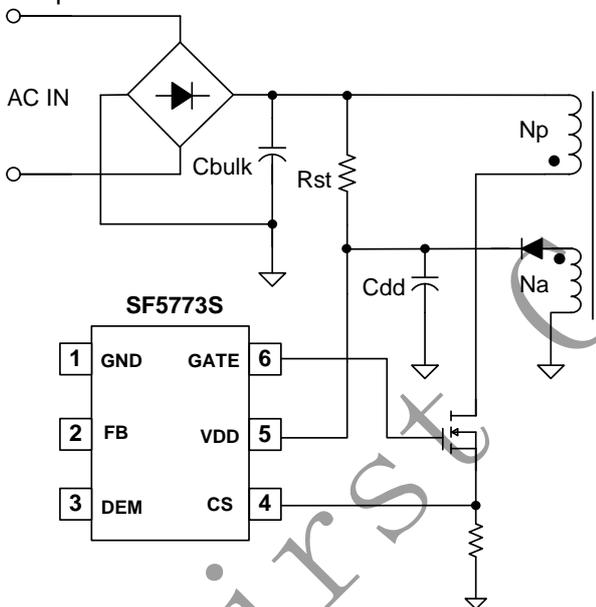


Fig.1

## ◆ QR-II[TM] Technology Introduction
## ● Digital Anti-Jitter for Valley Locking

Traditional QR system suffers from audio noise issues. As shown in Fig.2, traditional QR system triggers new PWM cycle using pure demagnetization information by sensing DEM pin voltage. However, the PWM triggering signal may toggle between different valleys at a given loading, which may cause audio noise issue.

In SF5773S, a "**Digital Anti-Jitter**" function is integrated to lock and select a valley at a given loading, which can achieve audio noise free operation.
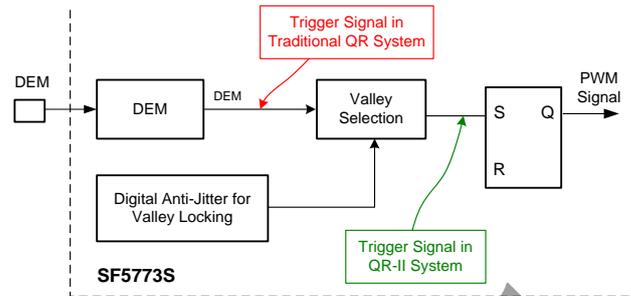


Fig.2

## ● "Digital Frequency Foldback" and Multi-Mode Operation

SF5773S is a multi-mode QR controller. The proprietary "**Digital Frequency Foldback**" can achieve high efficiency when the loading is light.

■ At normal or full loading conditions, the operating mode is CCM when the input is in low line range since the low clamping frequency (52KHz typical) is touched. Thus, small size transformer can be used with high power conversion efficiency. When the input is in high line input range, the IC work in QR mode with high frequency clamping (typical 80KHz), as shown in Fig.3. When FB voltage is larger than VFB_PL, the system enters into OLP mode with auto recovery protection (as illustrated in Fig.8 and Fig.9).
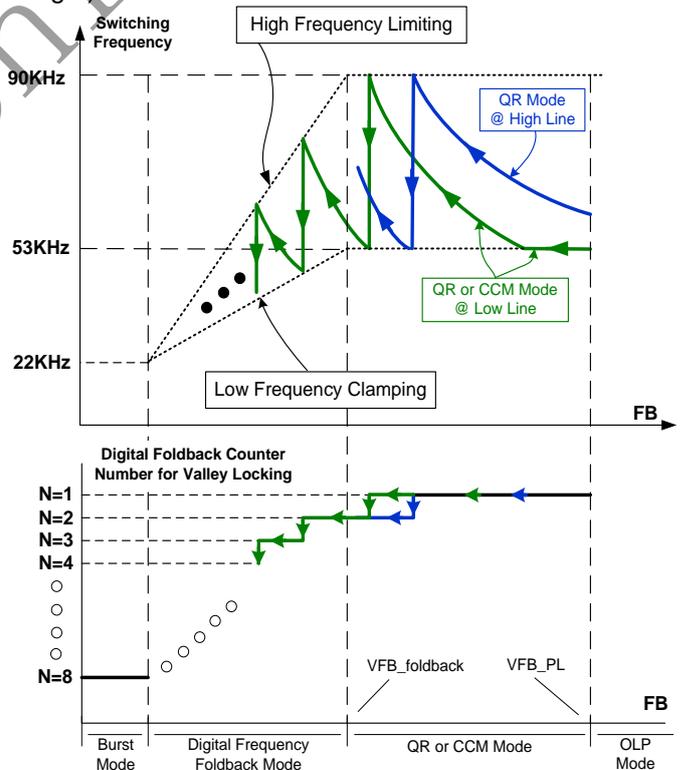


Fig.3

■ At light loading conditions (FB voltage is below VFB_foldback), the IC works in "**Digital Frequency Foldback**" mode. The system frequency is limited between "High Frequency Limiting" and "Low Frequency Clamping", as shown with the dashed line in Fig.3. In "**Digital Frequency Foldback**"

mode, the IC automatically selects and locks the switching valley according to the load changes. In SF5773S, a digital counter is integrated to register a counting number, the system will select the valleys based on the registered counter number. In SF5773S, the maximum counting number is 8.
■ When zero or very light load conditions, the IC enters into burst mode. In the burst mode (as illustrated in Fig.5), the valley locking counting number is fixed at 8. In this way, a small standby power can be achieved.

● **Digital Frequency Jittering**
Traditional QR system suffers from EMI issues since the PWM switching frequency is actually fixed with a given loading. To improve system EMI performance, SF5773S integrates a "**Digital Frequency Jittering**" block to operate the system with ±4% frequency jittering around the PWM switching frequency. The digital frequency jittering is active on all working modes.

◆ **Low Operating Current**
The operating current in SF5773S is as small as 1.8mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ **Soft Start**
SF5773S features an internal 4ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

◆ **Demagnetization Detection**
The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. When the stored energy is fully released to the output, the voltage on DEM goes down. If DEM pin voltage drops below 0.125V, an internal DEM comparator is triggered and a new switching cycle is initiated following the DEM triggering. The power MOSFET is always turned on with zero inductor current such that the turn-on loss and noise can be minimized.

◆ **Ringing Suppression Timer**
After power MOSFET is turned off, there will be some oscillation on Vds, which will also appear on the voltage on DEM pin. To avoid that the power MOSFET is turned on mistriggered by such oscillations, a ringing suppression timer Tsupp is implemented in SF5773S. In normal operation, Tsupp starts when CS reaches the feedback voltage FB, the external power MOSFET is set to OFF state. During Tsupp, the external power MOSFET remains in OFF state and cannot be

turned on gain. In SF5773S, the ringing suppression timer Tsupp is set to 2.5us internally.

◆ **Leading Edge Blanking (LEB)**
Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

◆ **OCP Compensation**
The variation of maximum output power in QR system can be rather large if no compensation is provided. In SF5773S, a proprietary OCP compensation block is integrated and no external components are needed. The OCP threshold in SF5773S is a function of the switching ON time. For the ON time less than 12.7us, the OCP threshold changes linearly from 0.45V to 0.77V. For the ON time larger than 12.7us, the OCP threshold is clamped to 0.77V, as shown in Figure 4. The maximum PWM duty cycle is about 65% in SF5773S.
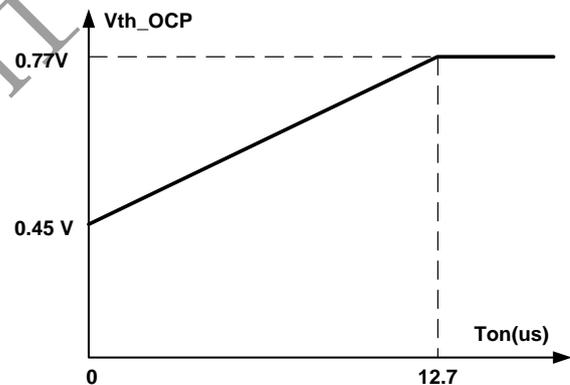


Fig.4

◆ **Adaptive Slope Compensation**
InSF5773S, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.
In SF5773S, when the fix frequency CCM mode is touched (as show in Fig.2), the slope compensation will be automatically added to the system to improve current loop stability. When the system leaves fix frequency CCM mode, the slope compensation will automatically disappear.

◆ **Maximum Frequency Clamp**
According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, when the output power

decreases, the switching frequency can become rather high without limiting. To meet EMI limit and to achieve high efficiency at light loading conditions, the maximum switching frequency in SF5773S is internally limited to 80KHz in QR mode.

### ◆ Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below VFB_min_duty, SF5773S will stop switching and output voltage starts to drop, which causes the VFB to rise, as shown in Fig.5. Once VFB rises above VFB_min_duty, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.
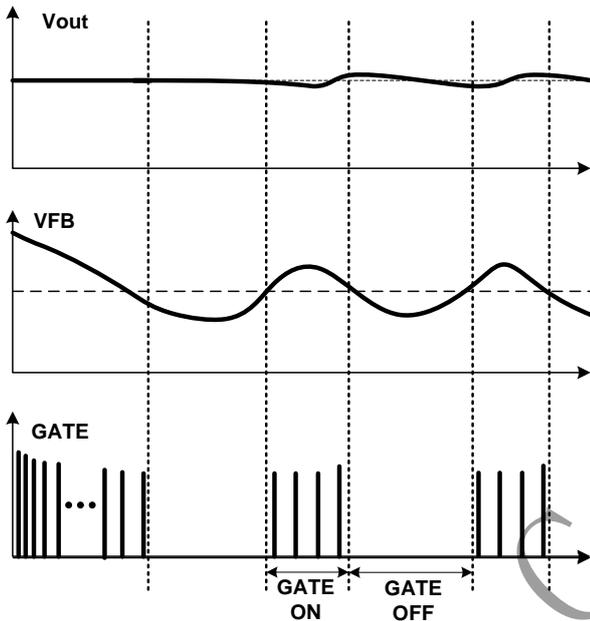


Fig.5

### ◆ Output Over Voltage Protection (Output OVP)

In SF5773S, the output OVP is integrated by plateau sampling the auxiliary winding in flyback phase. An internal 2.5us sampling delay guarantees a clean plateau, provided that the leakage inductance ringing has been fully damped. The threshold voltage for output OVP is 3.4V, as shown in Fig.6

If the sampled plateau voltage exceeds the OVP threshold (3.4V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 3 cycles, the controller assumes a true output OVP and it stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP threshold less than 3 successive cycles, the internal counter will be cleared and no fault is asserted. Output OVP is auto-recovery mode protection (mentioned below).
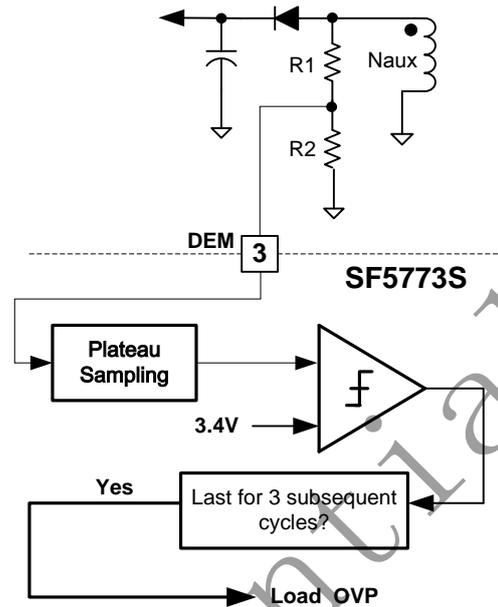


Figure 6

### ◆ Over Load Protection (OLP) / Over Current Protection (OCP) / Over Power Protection (OPP) / Open Loop Protection (OLP)

When OLP/OCP/OPP/Open Loop occurs, a fault is detected. If this fault is present for more than 82ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection, as shown in Fig.8. The 82ms delay time is to prevent the false trigger from the power-on and turn-off transient.
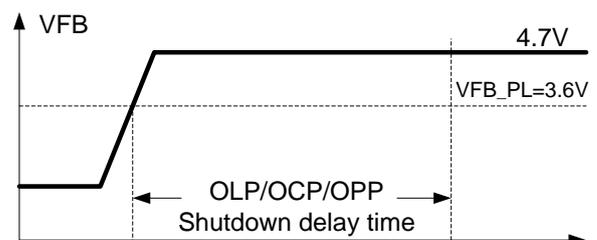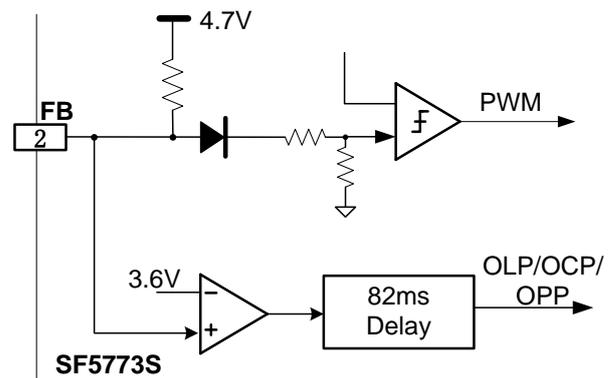


Fig.8

### ◆ Auto Recovery Mode Protection

As shown in Fig.9, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO(off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.9. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.
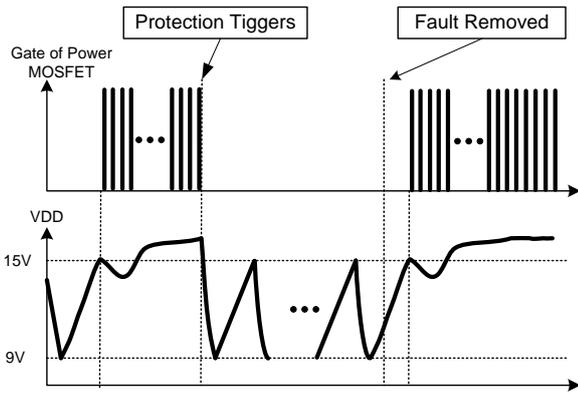
Fig.9

### ◆ AC Brownout Protection (BOP)

To prevent high current stress at too low AC voltage condition, SF5773S implements an AC Brownout Protection (BOP) through DEM pin, as shown in Fig.10. The current sourcing out from DEM pin when GATE pin is enabled is monitored to have the AC input voltage information. Once if the current keeps under $I_{TH\_BOP\_ON}$ (typical 71.5uA) for more than $T_{BOP\_PL}$ (typical 35ms), the AC BOP is issued and the PWM switching is disabled. When the current keeps above the $I_{TH\_BOP\_OFF}$ (typical 77uA), the AC brown in condition is issued and the PWM switching is enabled.
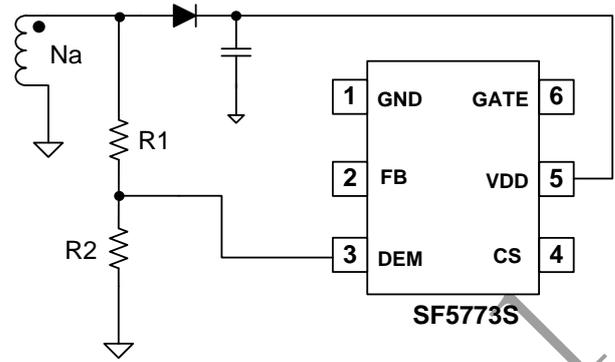
Fig.10

The AC line BOP triggering voltage and exit voltage are given by:

$$V_{Line\_BOP\_trigger} = \frac{71.5uA \times R_1}{\sqrt{2}} \times \frac{N_P}{N_A}$$

$$V_{Line\_BOP\_exit} = \frac{77uA \times R_1}{\sqrt{2}} \times \frac{N_P}{N_A}$$

By adjusting R1, the window between brownout trigger voltage and exit voltage can be programmed.

### ◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SF5773S and it is a protection of auto-recovery mode.

### ◆ Pin Floating Protection

In SF5773S, if pin floating situation occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

### ◆ Soft Gate Drive

The driving stage of SF5773S is a soft totem-pole gate driver to minimize EMI. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability.

## PACKAGE MECHANICAL DATA

### SOT-23-6L PACKAGE OUTLINE DIMENSIONS
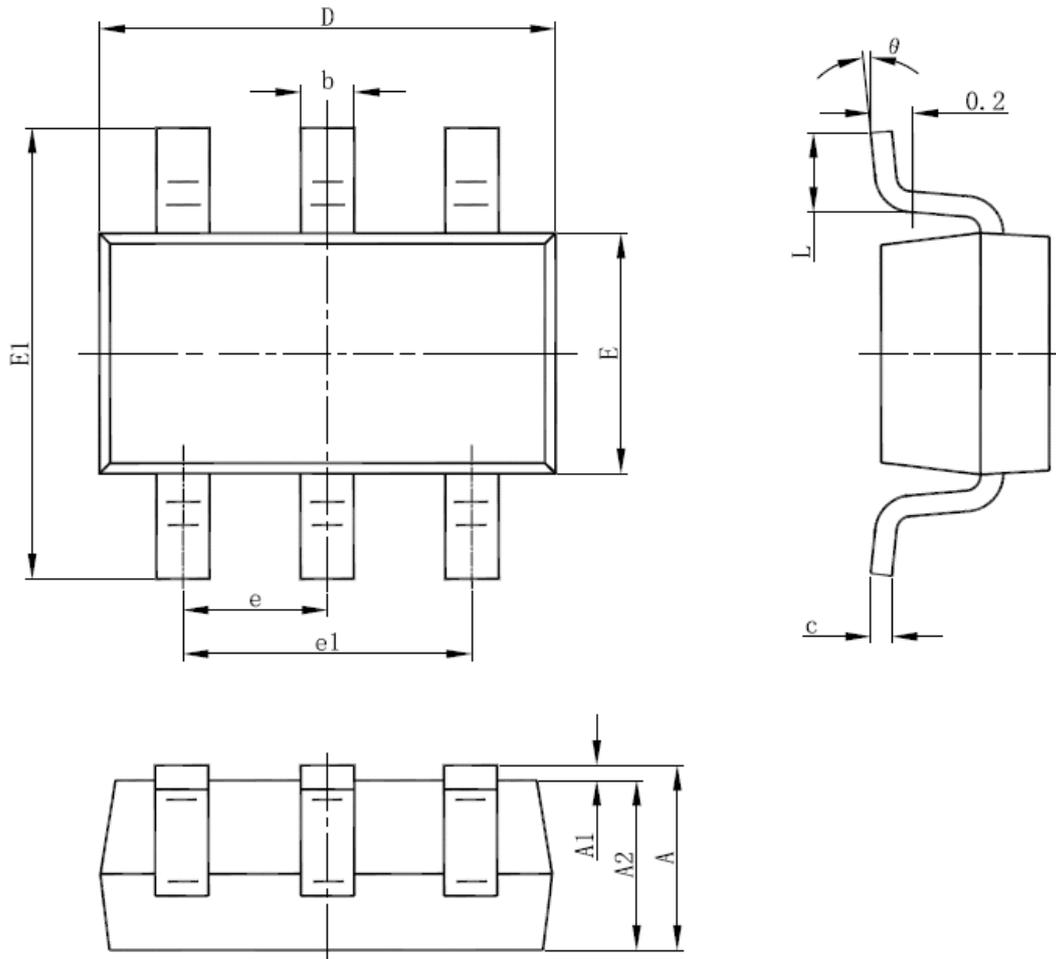


| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 1.000 | 1.300 | 0.039 | 0.051 |
| A1 | 0.000 | 0.150 | 0.000 | 0.006 |
| A2 | 1.000 | 1.200 | 0.039 | 0.047 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.100 | 0.200 | 0.004 | 0.008 |
| D | 2.800 | 3.020 | 0.110 | 0.119 |
| E | 1.500 | 1.700 | 0.059 | 0.067 |
| E1 | 2.600 | 3.000 | 0.102 | 0.118 |
| e | 0.950 (BSC) | | 0.037 (BSC) | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0º | 8º | 0º | 8º |

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