HV-mW™、2nd Generation Quasi-Resonant (QR-II™) PWM Controller

FEATURES

- **Easily Meet EPS Level 6**
- **Proprietary QR-II™ Technology:**
  - **●Digital Anti-jitter for Audio Noise Free Operation**
  - **● Digital Frequency Foldback**
  - **● Digital Frequency Jittering**
- **Proprietary HV-mW™ to Achieve Less than 50mW Standby Power**
- **Multi-Mode Operation for High Efficiency**
- **12.7us Maximum On Time**
- **80KHz Maximum Frequency Limit**
- **53KHz Frequency Low Clamping in QR Mode**
- **Maximum 65% Duty Cycle**
- **Adaptive Slope Compensation for CCM Mode**
- **Latch Plug-off Protection**
- **Built-in Soft Start Function**
- **Pin Floating Protection**
- **Built-in Synchronous Slope Compensation**
- **Cycle-by-Cycle Current Limiting**
- **Leading Edge Blanking (LEB)**
- **Constant Power Limiting**
- **VDD UVLO, OVP & Clamp**

APPLICATIONS

Offline AC/DC Flyback Converter for

- **AC/DC Adaptors**
- **SMPS Power Supply**

GENERAL DESCRIPTION

SF5877 is a high performance, 2nd Generation Quasi-Resonant (QR-II™) PWM controller for offline flyback power converter applications. The built-in proprietary **HV-mW™** technology and **QR-II™** technology with high level protection features can improve the SMPS reliability and performance.

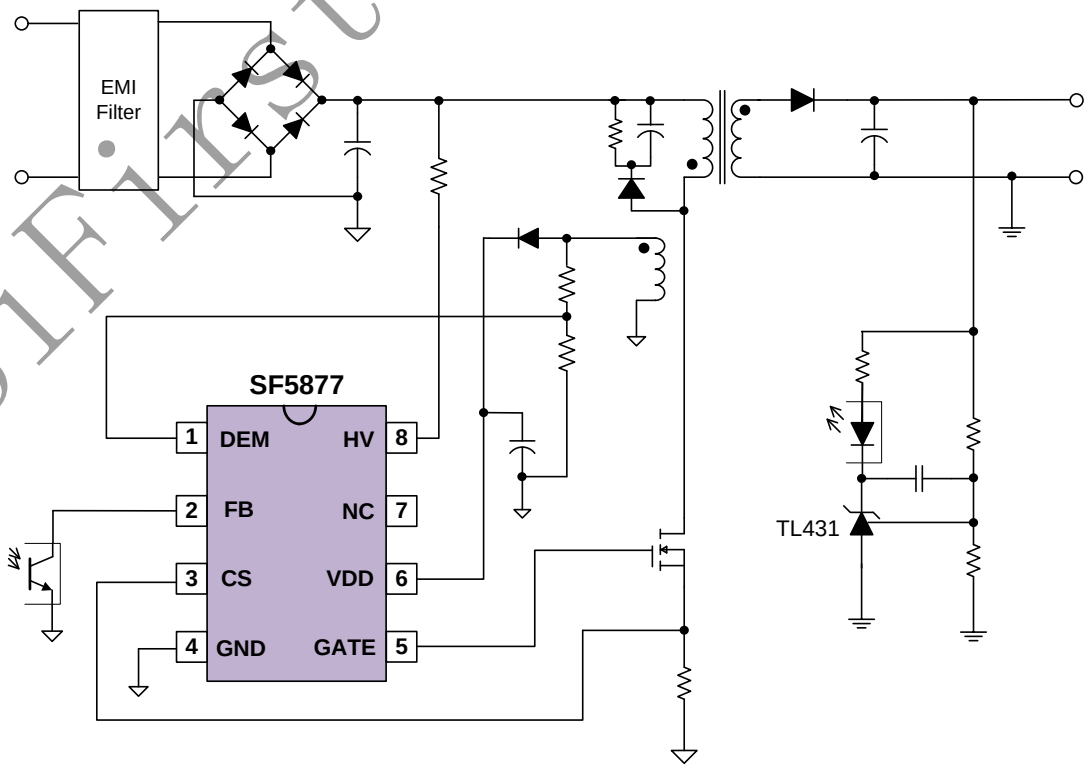
In SF5877, the "**Digital Anti-Jitter**" function can automatically select and lock a valley at a given loading, which can achieve audio noise free operation. On the other hand, the "**Digital Frequency Jittering**" function makes the system have superior EMI performance than conventional QR system.

SF5877 is a multi mode controller. When full loadings, the IC works in CCM mode or QR mode based on the AC line input. When the loading goes low, the IC enters into "**Digital Frequency Foldback**" mode to boost power conversion efficiency. When the output power is very small, the IC enters into burst mode and can achieve less than 50mW no load power.

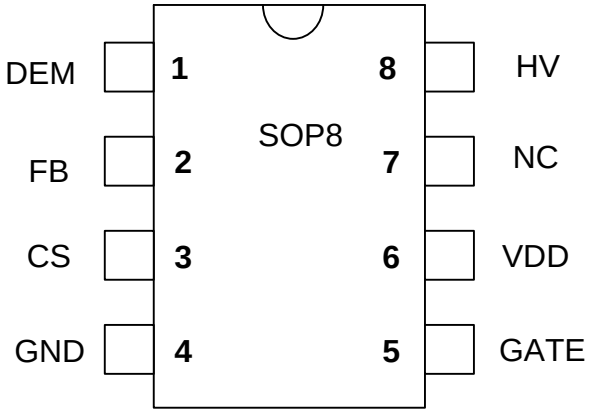
SF5877 integrates functions and protections of Under Voltage Lockout (UVLO), VDD Over Voltage Protection (VDD OVP), Output Over Voltage Protection (Output OVP), Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, Over Load Protection (OLP), Soft Start, VCC Clamping, Gate Clamping, etc. In SF5877, VDD OVP and Output OVP are latch mode protections, the other protections are auto-recovery mode.

SF5877 is available in SOP8 package.

TYPICAL APPLICATION



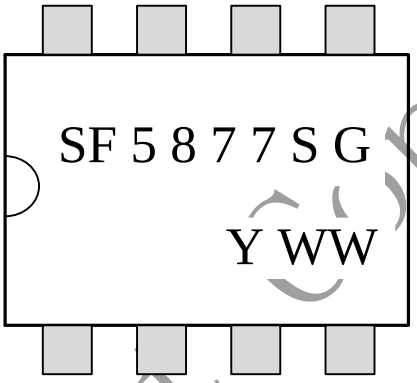
Pin Configuration



Ordering Information

Part Number	Top Mark	Package		Tape & Reel
SF5877SG	SF5580SG	SOP8	Green	
SF5877SGT	SF5580SGT	SOP8	Green	Yes

Marking Information

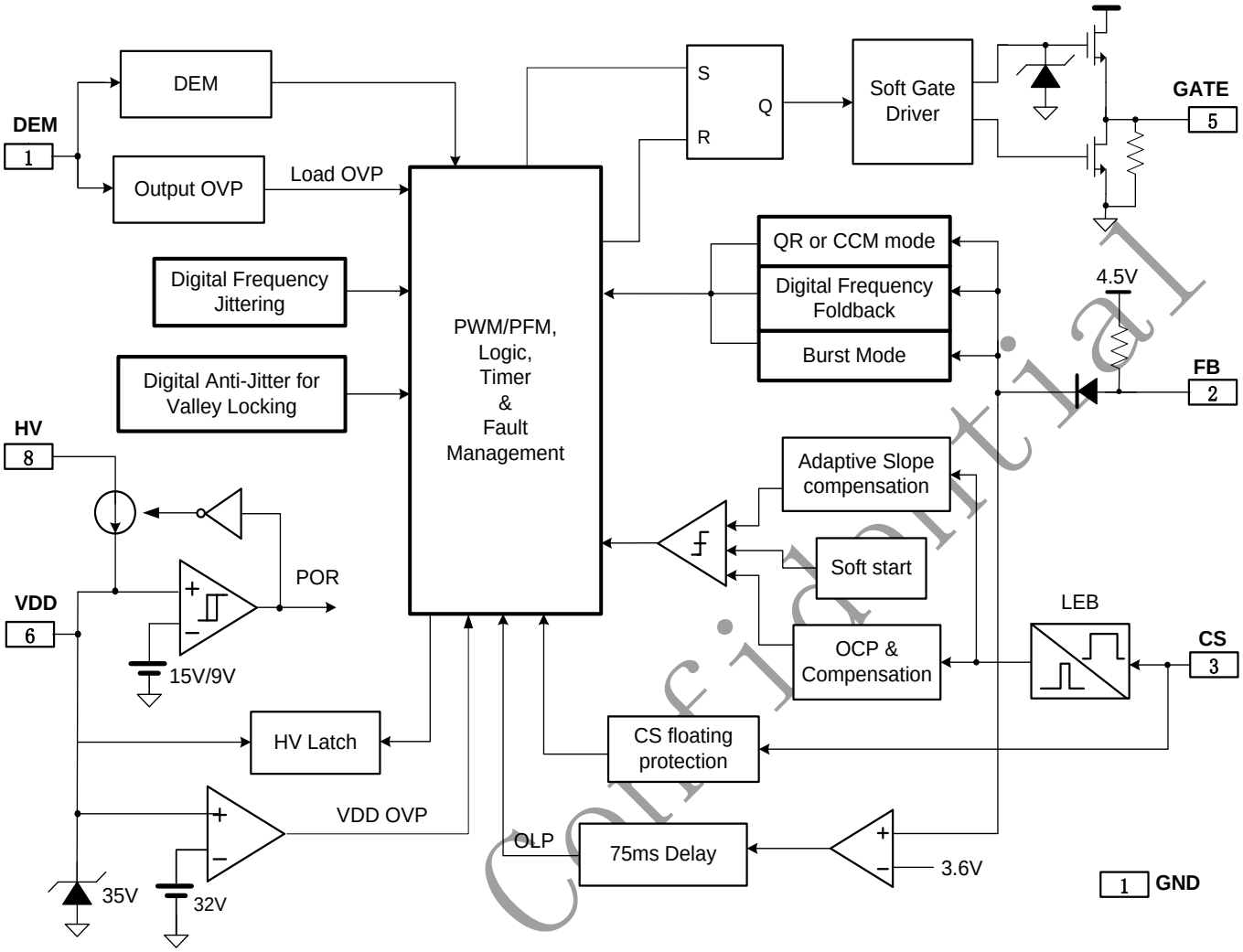


YWW: Year&Week code

Pin Description

Pin Num	Pin Name	I/O	Description
1	DEM	I	Transformer core demagnetization detection pin. This pin is also used for output over voltage protection (OVP).
2	FB	I	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is generated by this pin voltage and the current sense signal at Pin 3.
3	CS	I	Current sense input pin.
4	GND	P	IC ground pin.
5	GATE	O	Totem-pole gate driver output to drive the external MOSFET.
6	VDD	P	IC power supply pin.
7	NC	-	No connection.
8	HV	P	This pin connects to bulk capacitor for high voltage startup.

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
HV Voltage range	-0.3 to 700	V
VDD DC Supply Voltage	35	V
VDD DC Clamp Current	10	mA
DEM Voltage Range	-0.7 to 6	V
FB, CS Voltage Range	-0.3 to 7	V
Package Thermal Resistance (SOP-8)	150	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model) (Except HV Pin)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 29	V
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
High Voltage Supply Voltage Section (HV Pin)						
I_HV1	HV Current Source	VDD=2V, HV=500V	2	4	7	mA
I_HV2	HV Current Source	VDD=13V, HV=500V	1	2	3.5	mA
I_HV_leak	HV leakage current	VDD=18V, HV=500V			10	uA
Supply Voltage Section (VDD Pin)						
I_Startup	VDD Start up Current			5	20	uA
I_VDD_Op	Operation Current	V_{FB}=3.2V, GATE=1nF		2	3.5	mA
I(VDD_latch)	VDD latch mode current			100		uA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14	15	16	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8	9	10	V
VDD_OVP	VDD Over Voltage Protection trigger		30	32	34	V
V_{DD}_Clamp	VDD Zener Clamp Voltage	I(V_{DD}) = 7mA	33	35		V
T_Softstart	Soft Start Time			4		mSec
Feedback Input Section(FB Pin)						
V_{FB}_Open	FB Open Voltage			4.5		V
I_{FB}_Short	FB short circuit current	Short FB pin to GND, measure current		360		uA
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		3.5		V/V
VFB_foldback	FB under voltage foldback mode is entered			1.6		V
VFB_min_duty	FB under voltage gate clock is off.			1.1		V
VFB_PL	Power Limiting FB Threshold Voltage			3.6		V
T_D_PL	Power limiting Debounce Time	Note 3		75		mSec
Z_{FB}_IN	Input Impedance			13		Kohm
Current Sense Input Section (CS Pin)						
Vth_OC_min	Internal current limiting threshold	Zero duty cycle	0.44	0.45	0.46	V
Vth_OC_max	Internal current limiting threshold			0.77		V
T_blanking	SENSE Input Leading Edge Blanking Time			250		nSec
T_D_OC	Over Current Detection and Control Delay			60		nSec
Demagnetization Detection Section (DEM Pin)						
V_{TH}_DEM	DEM Comparator Threshold Voltage (Negative going edge)			100		mV
V_{DEM}_clamp_H	High clamp voltage			6		V
V_{DEM}_clamp_L	Low clamp voltage			-0.7		V
V_{TH}_OVP	Output over voltage protection threshold			3.4		V
N_{TRUE}_OVP	Number of subsequent cycles to be true OVP			3		Cycle
T_{supp}	Suppression of the transformer ringing at	Note 4		2.5		uSec

	start of secondary stroke					
T_{DEM_OUT}	Timeout after last demag transition	Note 4		5		uSec
Timer Section						
T_counter	Sampling Time for Digital Anti-jitter Function			40		mSec
N_counter_max	Maximum Number for Valley Locking			8		
F_BM	Burst Mode Base Frequency			22		KHz
Duty_max	Maximum Duty cycle			65		%
Fmax_QR_H	Frequency high clamp in QR mode		72	80	88	KHz
Fmin_QR_L	Frequency low clamp in QR mode		47	52	57	KHz
ΔF(shuffle)/Fosc	Frequency shuffling range	Note 4	-4		4	%
Ton_max	Maximum on time		11.5	12.7	14	us
Toff_max	Maximum off time		52	57	64	us
Toff_min	Minimum OFF time	Note 3		2.5		uSec
Latch Protection						
VDD_latch_H	VDD latch mode high voltage			12		V
$V_{Latch\_release}$	VDD Latch Release Voltage			8.7		V
Ivdd(latch)	VDD Current when latch off	VDD= $V_{Latch\_release}$+1V		100		uA
Gate Drive Output (GATE Pin)						
VOL	Output Low Level	Io = 20 mA (sink)			0.3	V
VOH	Output High Level	Io = 20 mA (source)	11			V
VG_Clamp	Output Clamp Voltage Level	VDD=24V		16		V
T_r	Output Rising Time	GATE= 1nF		80		nSec
T_f	Output Falling Time	GATE= 1nF		40		nSec

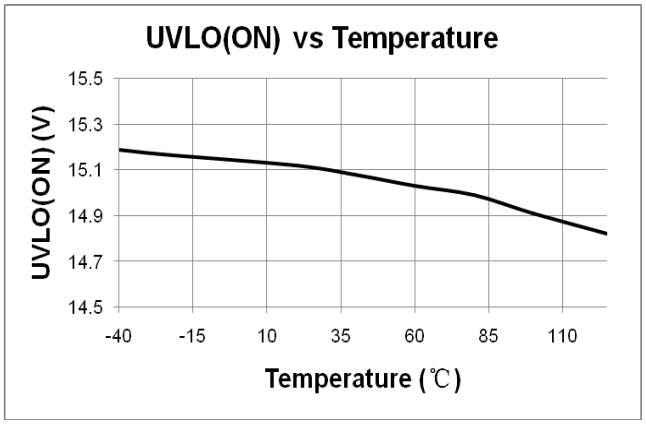
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

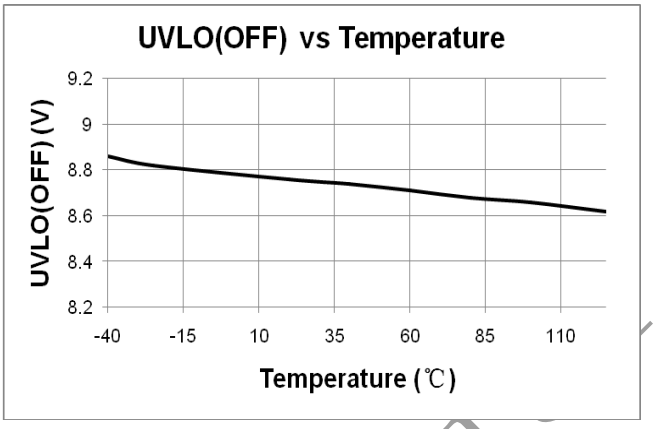
Note 2. The device is not guaranteed to function outside its operating conditions.

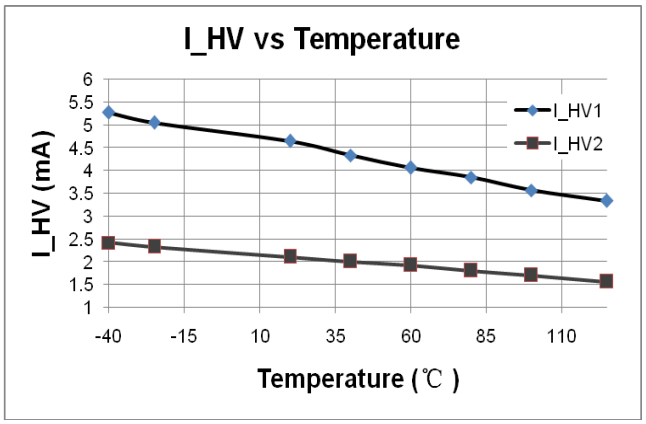
Note 3. The OLP debounce time is proportional to the period of switching cycle.

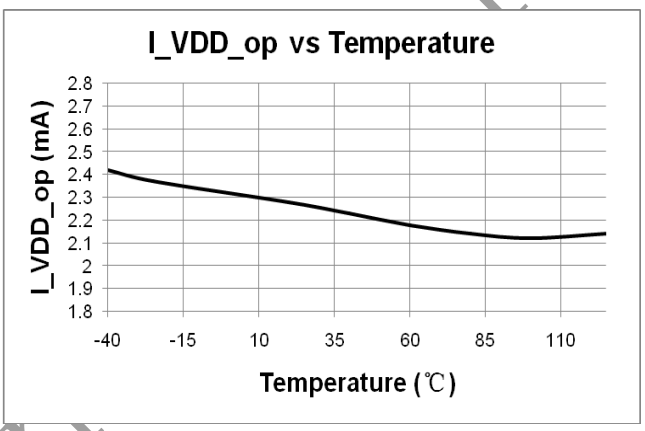
Note 4. Guaranteed by design.

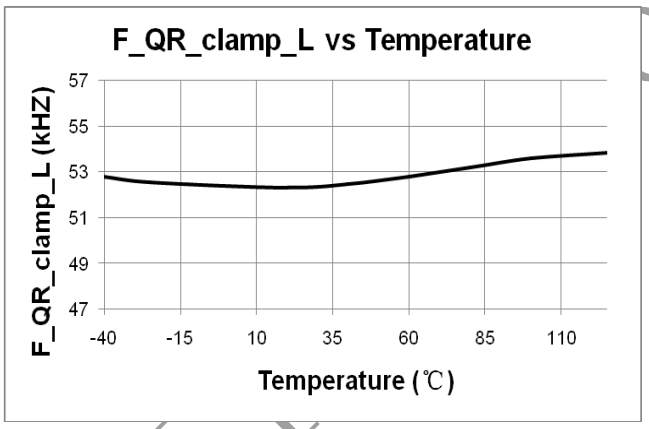
CHARACTERIZATION PLOTS

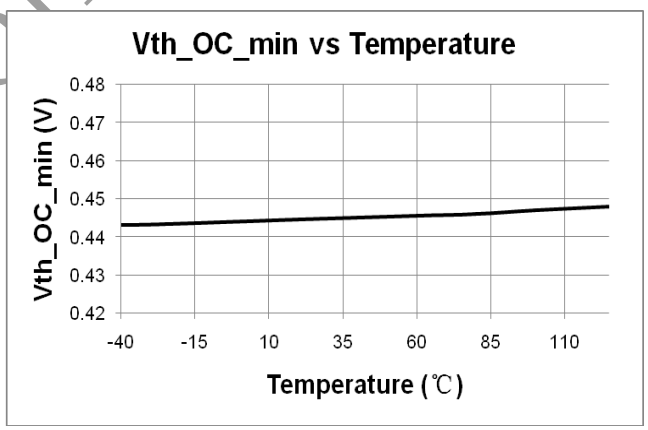


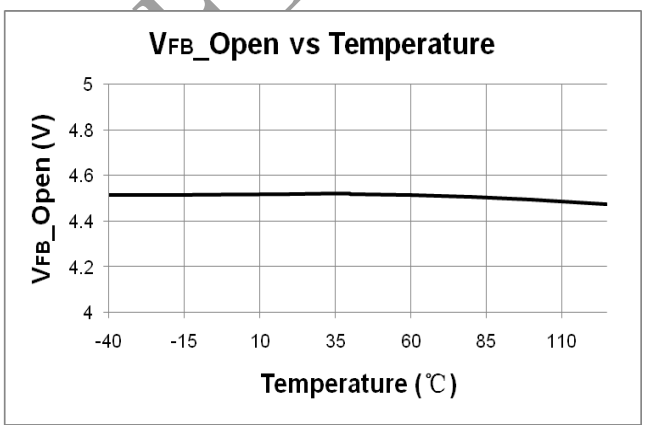












OPERATION DESCRIPTION

SF5877 is a high performance, highly integrated Quasi-Resonant (QR) PWM controller for medium to large offline flyback power converter applications. The built-in proprietary **QR-II™** technology with high level protection features improves the SMPS reliability and performance without increasing the system cost.

◆ Proprietary HV-mW™ Technology to Achieve Less than 50mW Standby Power

SF5877 Integrates proprietary HV-mW™ technology to achieve less than 50mW standby power. The core of HV-mW™ technology is related a built-in 700V startup circuit and standby control. Fig.1 shows the high voltage (HV) startup circuit for SF5877 applications. The HV pin is connected to the line input or bulk capacitor through a resistor. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cdd through Rst. When VDD reaches UVLO turn-on voltage of 15V(typical), SF5877 begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V).

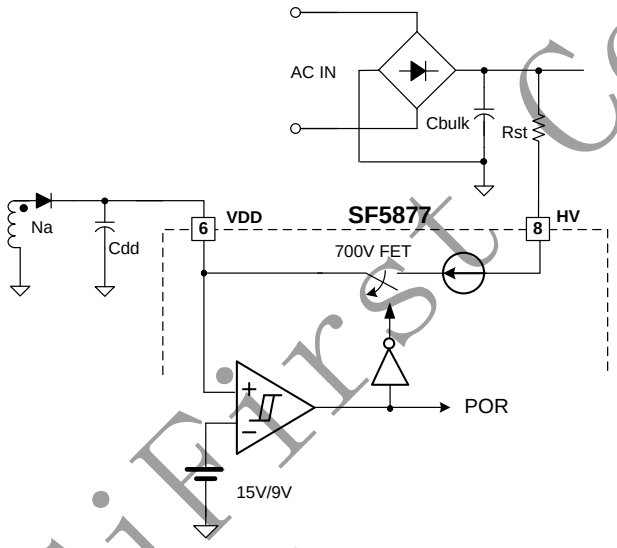


Fig.1

In general application, Rst is recommended to be larger than 30KΩ to limit the startup current.

◆ QR-II™ Technology Introduction

● Digital Anti-Jitter for Valley Locking

Traditional QR system suffers from audio noise issues. As shown in Fig.2, traditional QR system triggers new PWM cycle using demagnetization information by sensing DEM pin voltage. However, the PWM trigger signal may toggle between different valleys at a given loading, which may cause audio noise issue.

In SF5877, a "**Digital Anti-Jitter**" function is integrated to lock and select a valley at a given loading, which can achieve audio noise free operation.

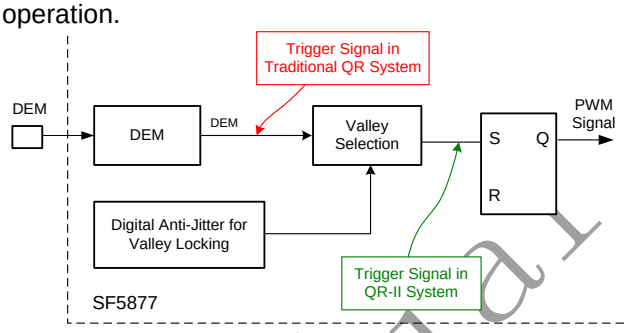


Fig.2

● "Digital Frequency Foldback" and Multi-Mode Operation

SF5877 is a multi-mode QR controller. The proprietary "**Digital Frequency Foldback**" can achieve high efficiency when the loading is light.

■ At normal or full loading conditions, the operating mode is CCM when the input is in low line range since the low clamping frequency (52KHz typical) is touched. Thus, small size transformer can be used with high power conversion efficiency. When the input is in high line input range, the IC work in QR mode with high frequency clamping (typical 80KHz), as shown in Fig.3. When FB voltage is larger than VFB_PL, the system enters into OLP mode with auto recovery protection (as illustrated in Fig.8 and Fig.9).

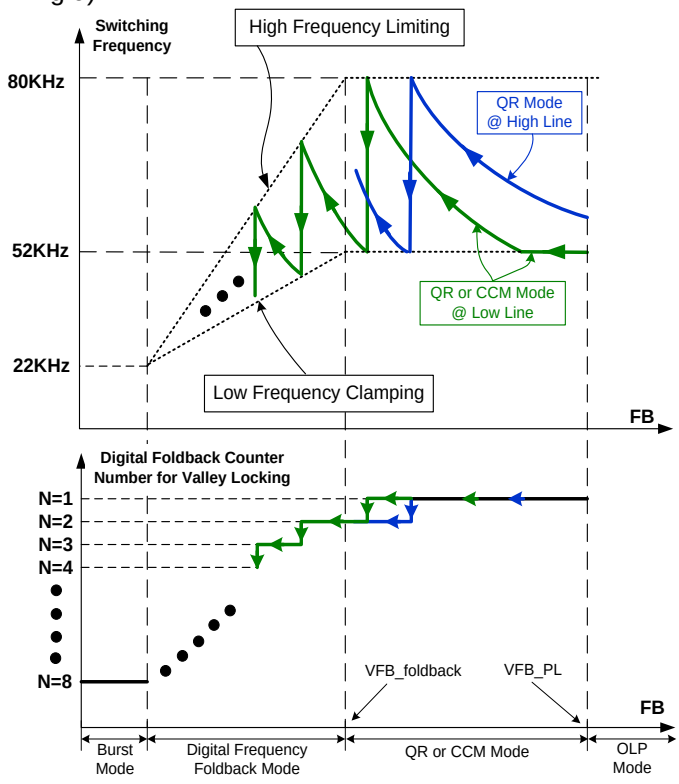


Fig.3

■ At light loading conditions (FB voltage is below

VFB_foldback), the IC works in "**Digital Frequency Foldback**" mode. The system frequency is limited between "High Frequency Limiting" and "Low Frequency Clamping", as shown with the dashed line in Fig.3. In "**Digital Frequency Foldback**" mode, the IC locks the switching valley and selects the valley according to the load changes. There is a counter in SF5877, the IC selects the valleys according to the registered counter number. In SF5877, the maximum counting number is 8.

■ When zero or very light load conditions, the IC enters into burst mode. In the burst mode (as illustrated in Fig.5), the valley locking counting number is fixed at 8. In this way, a small standby power can be achieved.

● Digital Frequency Jittering

Traditional QR system suffers from EMI issues since the PWM switching frequency is actually fixed with a given loading. To improve system EMI performance, SF5877 integrates a "**Digital Frequency Jittering**" block to operate the system with ±4% frequency jittering around the PWM switching frequency.

◆ Low Operating Current

The operating current in SF5877 is as small as 2mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ Soft Start

SF5877 features an internal 4ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

◆ Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. When the stored energy is fully released to the output, the voltage on DEM goes down. If DEM pin voltage drops below 0.1V, an internal DEM comparator is triggered and a new switching cycle is initiated following the DEM triggering. The power MOSFET is always turned on with zero inductor current such that the turn-on loss and noise can be minimized.

◆ Ringing Suppression Timer

After power MOSFET is turned off, there will be some oscillation on Vds, which will also appear on the voltage on DEM pin. To avoid that the power MOSFET is turned on mistriggered by such oscillations, a ringing suppression timer Tsupp is implemented in SF5877. In normal operation, Tsupp starts when CS reaches the feedback voltage FB, the external power MOSFET is set to off state. During Tsupp, the external power MOSFET remains in off state and cannot be turned on gain. In SF5877, the ringing suppression timer Tsupp is set to 2.5us internally.

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

◆ Adaptive Slope Compensation

InSF5877, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

In SF5877, when the fix frequency CCM mode is touched (as show in Fig.2), the slope compensation will be automatically added to the system to improve current loop stability. When the system leaves fix frequency CCM mode, the slope compensation will automatically disappear.

◆ Maximum Frequency Clamp

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, when the output power decreases, the switching frequency can become rather high without limiting. To meet EMI limit and to achieve high efficiency at light loading conditions, the maximum switching frequency in SF5877 is internally limited to 80KHz.

◆ OCP Compensation

The variation of maximum output power in QR system can be rather large if no compensation is provided. The OCP threshold value is self adjusted lower at higher AC voltage. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage. In SF5877, a proprietary OCP compensation block is integrated and no external components are needed. The OCP threshold in SF5877 is a function of the switching ON time. For the ON time less than 12.7us, the OCP threshold changes linearly from 0.45V to 0.77V. For the ON time larger than 12.7us, the OCP threshold is clamped to 0.77V, as shown in Figure 4.

The maximum PWM duty cycle is about 65% in SF5877.

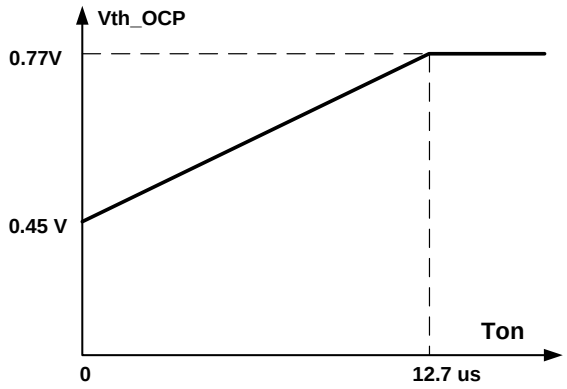


Fig.4

◆ Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below VFB_min_duty, SF5877 will stop switching and output voltage starts to drop, which causes the VFB to rise, as shown in Fig.5. Once VFB rises above VFB_min_duty, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

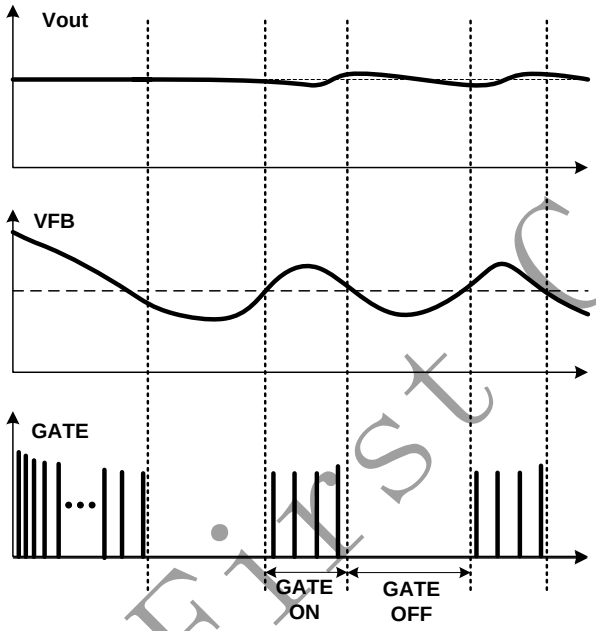


Fig.5

◆ Output Over Voltage Protection (OVP)

In SF5877, the load OVP is integrated by plateau sampling the auxiliary winding in flyback phase. An internal 2.5us sampling delay guarantees a clean plateau, provided that the leakage inductance ringing has been fully damped. The threshold voltage for output OVP is 3.4V, as shown in Fig.6

If the sampled plateau voltage exceeds the OVP threshold (3.4V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 3 cycles, the controller assumes a true OVP and it stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP threshold less than 3 successive cycles, the internal counter will be cleared and no fault is asserted. Output OVP is **latch mode** protection (mentioned below).

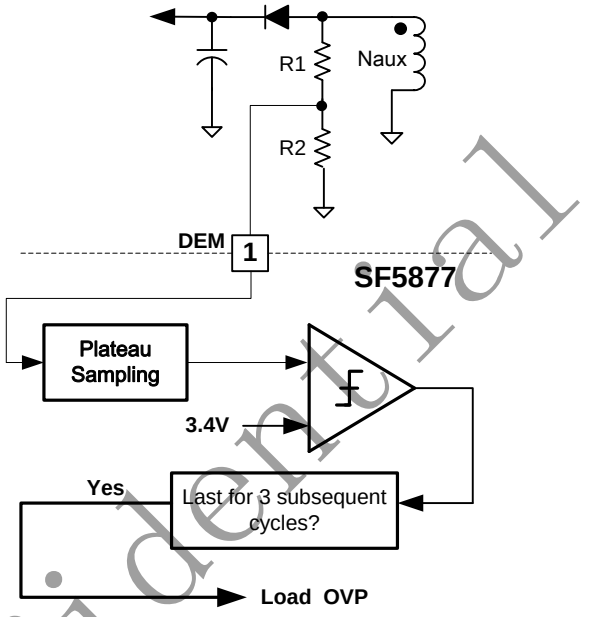


Figure 6

◆ Latch Mode Protection

As shown in Fig.7, once a latch mode protection (such as OTP, VDD OVP, etc) is detected, switching will stop. VDD voltage will ramp up and down between VDD_latch_H (typical 12V) and UVLO(OFF) (typical 9V). The VDD ramping up current is get from HV pin. In latch mode, IC consumption current is about 100uA. The latch will not release unless AC input is unplugged from the mains.

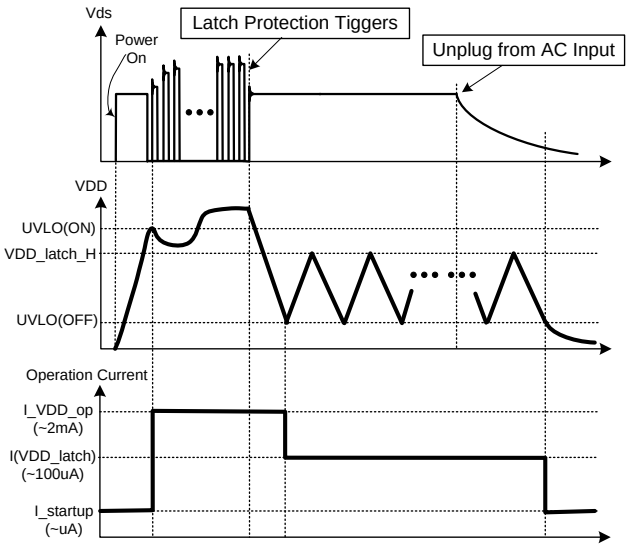


Fig.8

◆ Over Load Protection (OLP) / Over Current Protection (OCP) / Over Power Protection (OPP) / Open Loop Protection (OLP)

When OLP/OCP/OPP/Open Loop occurs, a fault is detected. If this fault is present for more than 75ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection, as shown in Fig.8. The 75ms delay time is to prevent the false trigger from the power-on and turn-off transient.

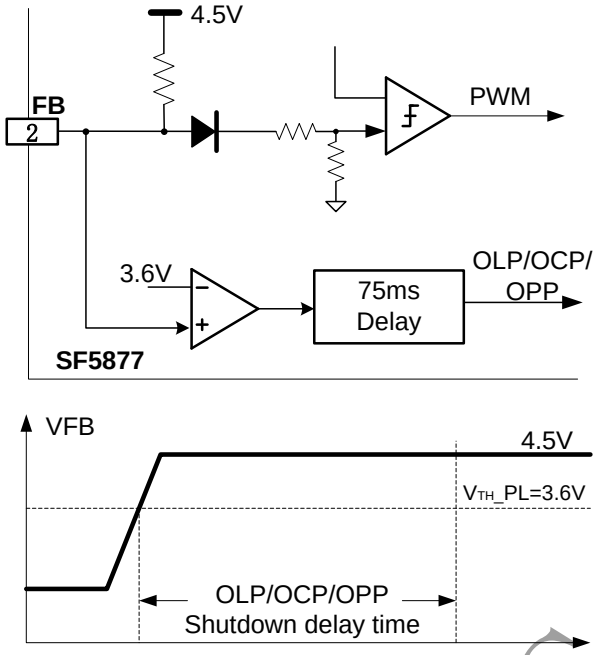


Fig.8

◆ Auto Recovery Mode Protection

As shown in Fig.9, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO(off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.9. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

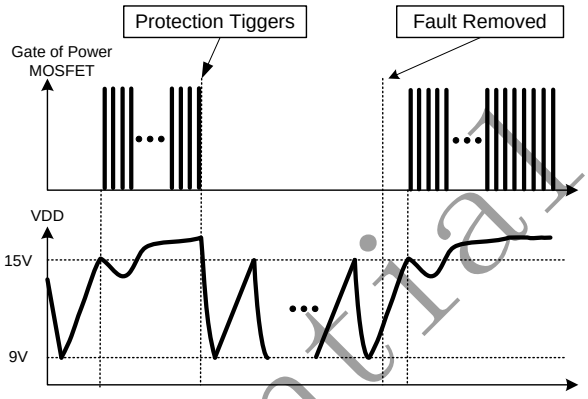


Fig.9

◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SF5877 and it is a protection of **latch mode**.

◆ Pin Floating Protection

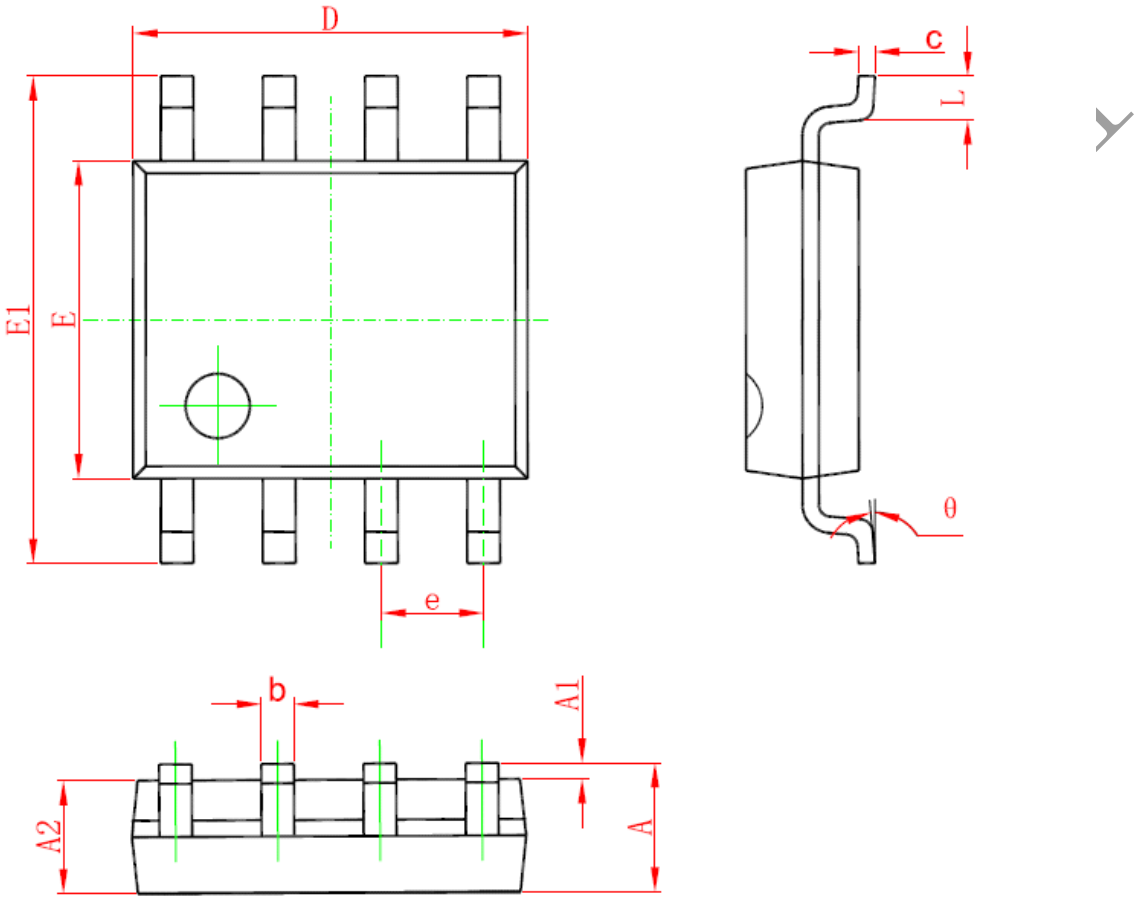
In SF5877, if pin floating situation occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

◆ Soft Gate Drive

The driving stage of SF5877 is a soft totem-pole gate driver to minimize EMI. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability.

PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

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