General Purpose, 1.8V, RRI, Open-Drain Output Comparators

Features

- **Down to 1.8V Supply Voltage: 1.8V to 5.5V**
- **Low Supply Current: 40 µA per Channel Typ**
- **High-to-Low Propagation Delay: 120 ns Typ**
- **Internal Hysteresis Ensures Clean Switching**
- **Offset Voltage: ± 3.5 mV Maximum**
- **Input Bias Current: 6 pA Typical**
- **Input Common-Mode Range Extends 200 mV**
- **No Phase Reversal for Overdriven Inputs**
- **Open-Drain Output for Maximum Flexibility**
- **Green, Space-Saving SC70 Package Available**

Applications

- Peak and Zero-crossing Detectors
- Threshold Detectors/Discriminators
- Sensing at Ground or Supply Line
- Logic Level Shifting or Translation
- Window Comparators
- IR Receivers
- Clock and Data Signal Restoration
- Telecom, Portable Communications
- Portable and Battery Powered Systems

Description

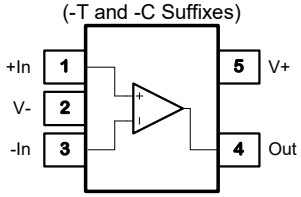
The 3PEAK INCORPORATED LMV331-393 are the most cost-effective solutions for applications where low-voltage operation, low power, space saving, and price are the primary specifications in circuit design for portable consumer products. The LMV331TP is the single-comparator, the LMV393TP is the dual, and both are open-drain output comparators for maximum flexibility.

The chips incorporate 3PEAK's proprietary and patented design techniques to achieve the ultimate combination of high-speed (120ns high-to-low propagation delay) and low power consuming (40µA quiescent current per comparator). These comparators are optimized for low power 1.8V, single-supply applications with greater than rail-to-rail input operation, and also operate with ±0.9V to ±2.75V dual supplies. The input common-mode voltage range extends 200mV below ground and 200mV above supply, allowing both ground and supply sensing. The internal input hysteresis eliminates output switching due to internal input noise voltage, reducing current draw.

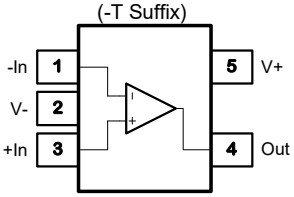
The LMV331TPL1 single comparator is available in tiny SC70 package for space-conservative designs. All chips are specified for the temperature range of –40°C to +85°C.

Pin Configuration (Top View)

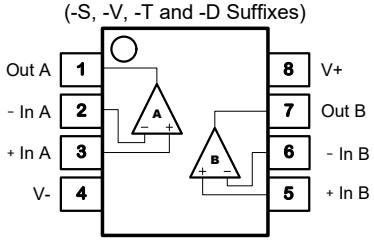
LMV331TP
5-Pin SOT23/SC70
(-T and -C Suffixes)



LMV331TPU
5-Pin SOT23
(-T Suffix)



LMV393TP
8-Pin SOIC/MSOP/TSSOP/DIP
(-S, -V, -T and -D Suffixes)



Related Products

DEVICE	DESCRIPTION
TP1951/TP1951N /TP1952/TP1954	Fast 30ns, Low Power, Internal Hysteresis, ±3mV Maximum V_{OS}, – 0.2V to V_{DD} + 0.2V RRI, Push-Pull (CMOS/TTL) Output Comparators
TP1955/TP1955N /TP1956/TP1958	Fast 30ns, Low Power, Internal Hysteresis, ±3mV Maximum V_{OS}, – 0.2V to V_{DD} + 0.2V RRI, Open-Drain Output Comparators
TP1931 /TP1932/TP1934	950ns, 3µA, 1.8V, ±2.5mV V_{OS-MAX}, Internal Hysteresis, RRI, Push-Pull Output Comparators
TP1935 /TP1936/TP1938	950ns, 3µA, 1.8V, ±2.5mV V_{OS-MAX}, Internal Hysteresis, RRI, Open-Drain Comparators
TP2011 /TP2012/TP2014	Ultra-low 200nA, 13µs, 1.6V, ±2mV V_{OS-MAX}, Internal Hysteresis, RRI, Push-Pull (CMOS/TTL) Output Comparators
TP2015 /TP2016/TP2018	Ultra-low 200nA, 13µs, 1.6V, ±2mV V_{OS-MAX}, Internal Hysteresis, RRI, Open-Drain Output Comparators

Order Information

Model Name	Order Number	Package	MSL Level	Transport Media, Quantity	Marking Information
LMV331TPL1	LMV331TPL1-TR	5-Pin SOT23	Level 1	Tape and Reel, 3000	CA4YW (1)
	LMV331TPL1-CR	5-Pin SC70	Level 1	Tape and Reel, 3000	CB4YW (1)
LMV331TPUL1	LMV331TPUL1-TR	5-Pin SOT23	Level 1	Tape and Reel, 3000	CI4YW (1)
LMV393TPL1	LMV393TPL1-SR	8-Pin SOIC	Level 1	Tape and Reel, 4000	C46S
	LMV393TPL1-VR	8-Pin MSOP	Level 1	Tape and Reel, 3000	C46V
	LMV393TPL1-TR	8-Pin TSSOP	Level 1	Tape and Reel, 3000	C46T
	LMV393TPL1-DR	8-Pin DIP	Level 1	Tape and Reel, 3000	C46D

Note (1): 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^-$.....6.0V
Input Voltage..... V^- – 0.3 to V^+ + 0.3
Input Current: +IN, –IN, Note 2.....±10mA
Output Current: OUT..... ±45mA
Output Short-Circuit Duration Note 3..... Indefinite

Operating Temperature Range.....–40°C to 85°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1	kV

Thermal Information

Package	$R_{\Theta JA}$	$R_{\Theta JC(Top)}$	Unit
8-Pin SOP	112.4	64.1	°C/W
8-Pin MSOP	127.3	50.8	°C/W
8-Pin TSSOP	152.5	51.1	°C/W

Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 27°C. V_{DD} = +1.8V to +5.5V, V_{IN+} = V_{DD}, V_{IN-} = 1.2V, R_{PU}=10kΩ, C_L =15pF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	1.8		5.5	V
V_{OS}	Input Offset Voltage Note 1	VCM = 1.2V		-3.5	±0.6	+3.5	mV
V_{OS} TC	Input Offset Voltage Drift Note 1	VCM = 1.2V			0.5		μV/°C
V_{HYST}	Input Hysteresis Voltage Note 1	VCM = 1.2V		3	6	9	mV
V_{HYST} TC	Input Hysteresis Voltage Drift Note 1	VCM = 1.2V			20		μV/°C
I_B	Input Bias Current	VCM = 1.2V			6		pA
I_{OS}	Input Offset Current				4		pA
R_{IN}	Input Resistance				> 100		GΩ
C_{IN}	Input Capacitance	Differential Common Mode			2 4		pF
CMRR	Common Mode Rejection Ratio	VCM = VSS to VDD			70		dB
V_{CM}	Common-mode Input Voltage Range		●	V– - 0.1		V+ + 0.1	V
PSRR	Power Supply Rejection Ratio				75		dB
V_{OL}	Low-Level Output Voltage	IOUT=1mA				V– + 0.3	V
I_{SC}	Output Short-Circuit Current	Sink or source current			25		mA
I_Q	Quiescent Current per Comparator				40	70	μA
t_R	Rising Time				5		ns
t_F	Falling Time				5		Ns
t_{PD-}	Propagation Delay (High-to-Low)	Input Overdrive=100mV, VIN- =2.5V			120		Ns
t_{PD+}	Propagation Delay (Low-to-High)	RPU=5.1kΩ, Input Overdrive=100mV, VIN- =2.5V			250		ns

Note 1: The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

Note 2: Propagation Delay Skew is defined as: $t_{PD-SKEW}$ = t_{PD+} - t_{PD-}.

Pin Functions

–IN: Inverting Input of the Comparator. Voltage range of this pin can go from V^- – 0.3V to V^+ + 0.3V.

+IN: Non-Inverting Input of Comparator. This pin has the same voltage range as –IN.

NC: No Connection.

V+ (V_{DD}): Positive Power Supply. Typically the voltage is from 1.8V to 5.5V. Split supplies are possible as long as the voltage between V+ and V– is between 1.8V and 5.5V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^- (V_{SS}): Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 1.8V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

OUT: Comparator Output. The voltage range extends to within millivolts of each supply rail.

Operation

The LMV331-393 single-supply comparators feature internal hysteresis, high speed, and low power. Input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is active over different ranges of common mode input voltage. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment.

Applications Information

Inputs

The LMV331-393 comparators use CMOS transistors at the input which prevent phase inversion when the input pins exceed the supply voltages. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion.

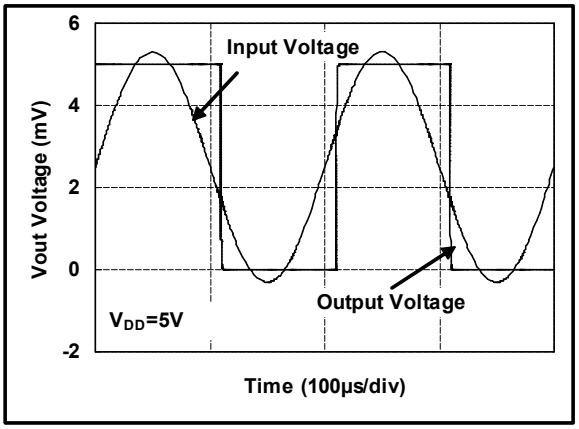


Figure 1. Comparator Response to Input Voltage

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed supply voltages, as shown in Figure 2. Large differential voltages exceeding the supply voltage should be avoided to prevent damage to the input stage.

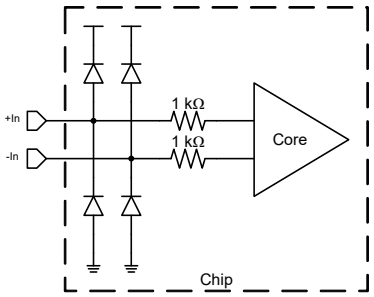


Figure 2. Equivalent Input Structure

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the LMV331-393 implement internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Figure 3. illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

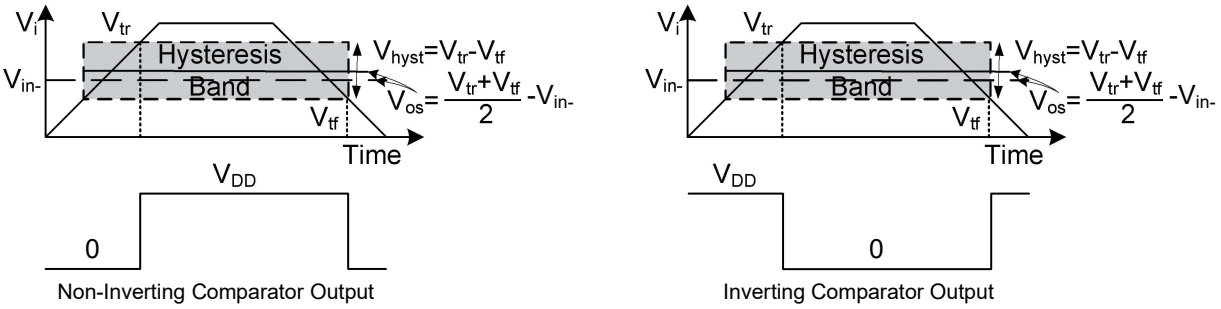


Figure 3. Comparator's hysteresis and offset

External Hysteresis

Greater flexibility in selecting hysteresis is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). Output chatter also increases the dynamic supply current.

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 4 and a voltage reference (V_r) at the inverting input.

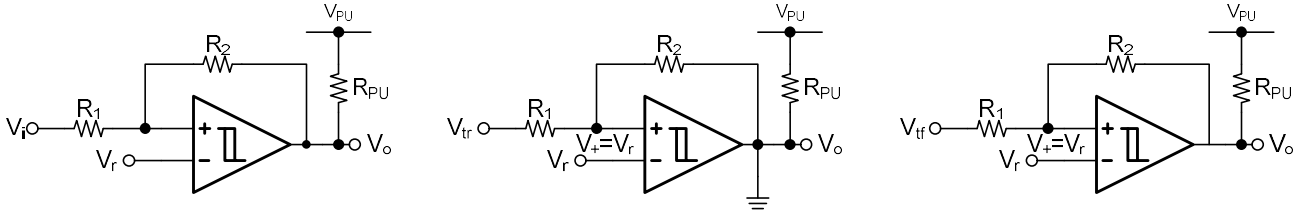


Figure 4. Non-Inverting Configuration with Hysteresis

When V_i is low, the output is also low. For the output to switch from low to high, V_i must rise up to V_{tr}. When V_i is high, the output is also high. In order for the comparator to switch back to a low state, V_i must equal V_{tf} before the non-inverting input V_+ is again equal to V_r.

$$V_r = \frac{R_2}{R_1 + R_2} V_{tr}$$

$$V_r = (V_{DD} - V_{tf}) \frac{R_1}{R_1 + R_2 + R_{PU}} + V_{tf}$$

$$V_{tr} = \frac{R_1 + R_2}{R_2} V_r$$

$$V_{tf} = \frac{R_1 + R_2 + R_{PU}}{R_2 + R_{PU}} V_r - \frac{R_1}{R_2 + R_{PU}} V_{DD}$$

$$V_{hyst} \approx \frac{R_1}{R_2 + R_{PU}} V_{DD} \quad \text{if } R_{PU} << R_2$$

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{DD}), as shown in Figure 5.

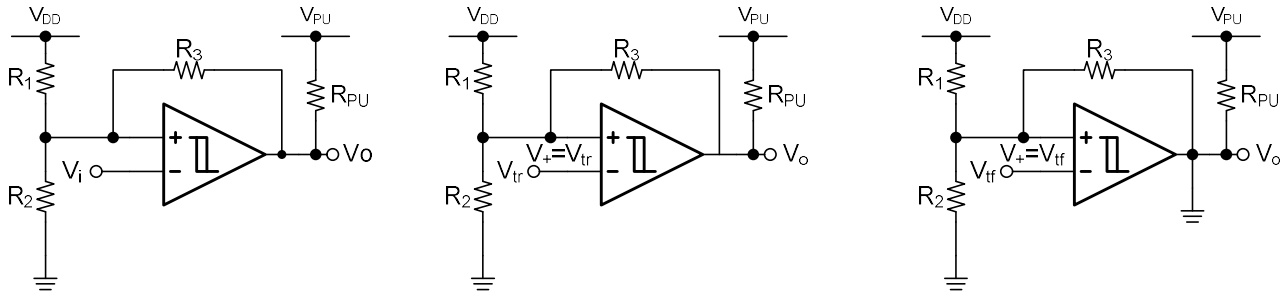


Figure 5. Inverting Configuration with Hysteresis

When V_i is greater than V_+, the output voltage is low. In this case, the three network resistors can be presented as paralleled resistor R_2 || R_3 in series with R_1. When V_i at the inverting input is less than V_+, the output voltage is high. The three network resistors can be represented as R_1 ||R_3 in series with R_2.

$$V_{tr} = \frac{R_2}{R_1 \parallel R_3 + R_2} V_{DD}$$

$$V_{tf} = \frac{R_2 \parallel R_3}{R_2 \parallel R_3 + R_1} V_{DD}$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_3} V_{DD}$$

Low Input Bias Current

The LMV331-393 are CMOS comparator family and feature very low input bias current in pA range. The low input bias current allows the comparators to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the LMV331-393’s input bias current at +27°C (±6pA, typical). It is recommended to use multi-layer PCB layout and route the comparator’s -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 6 for Inverting configuration application.

1. For Non-Inverting Configuration:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the same reference as the comparator.
2. For Inverting Configuration:
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

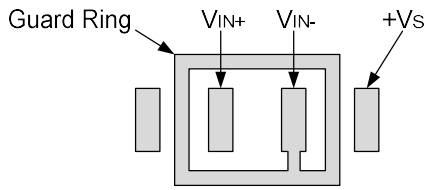


Figure 6. Example Guard Ring Layout for Inverting Comparator

Ground Sensing and Rail to Rail Output

The LMV331-393 implement a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300mV beyond either rail, the comparator can easily perform ‘true ground’ sensing.

The maximum output current is a function of total supply voltage. As the supply voltage of the comparator increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit condition. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The LMV331-393 have reverse-biased ESD protection diodes on all inputs and output. Input and output pins can not be biased more than 300mV beyond either supply rail.

Power Supply Layout and Bypass

The LMV331-393's power supply pin should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Good ground layout improves performance by decreasing the amount of stray capacitance and noise at the comparator's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components as close to the comparator' pins as possible.

Proper Board Layout

The LMV331-393 are a series of fast-switching, high-speed comparator and requires high-speed layout considerations. For best results, the following layout guidelines should be followed:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.

2. Place a decoupling capacitor (0.1μF ceramic, surface-mount capacitor) as close as possible to supply.

3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.

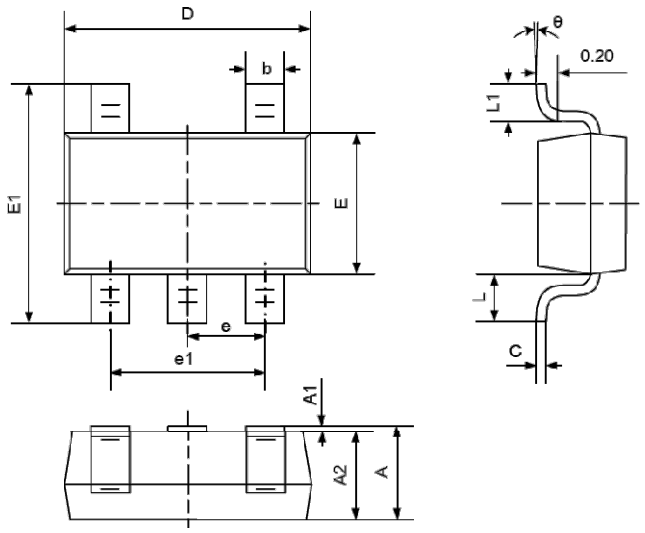
4. Solder the device directly to the PCB rather than using a socket.

5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane should be placed between the output and inputs.

6. The ground pin ground trace should run under the device up to the bypass capacitor, thus shielding the inputs from the outputs.

Package Outline Dimensions

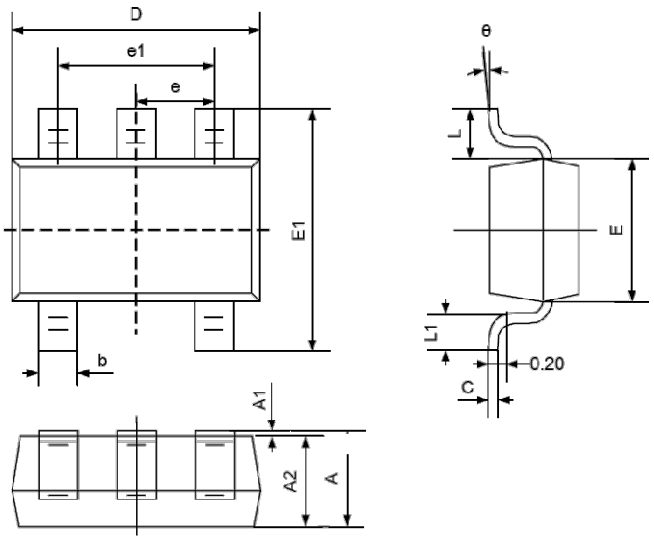
SOT23-5



Symbol	Dimensions In Millimeters	
	Min	**Max**
A	1.050	1.250
A1	0.000	0.100
A2	1.000	1.150
b	0.300	0.500
C	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.600	3.000
e	0.950TYP	
e1	1.800	2.000
L	0.600REF	
L1	0.300	0.600
θ	0°	8°

Package Outline Dimensions

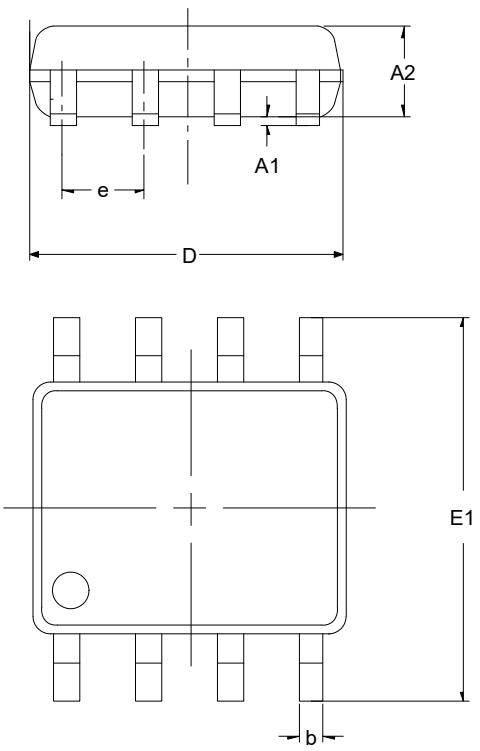
SC-70-5 (SOT353)



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.900	1.100
A1	0.000	0.100
A2	0.900	1.000
b	0.150	0.350
C	0.110	0.175
D	2.000	2.200
E	1.150	1.350
E1	2.150	2.450
e	0.650TYP	
e1	1.200	1.400
L	0.525REF	
L1	0.260	0.460
θ	0°	8°

Package Outline Dimensions

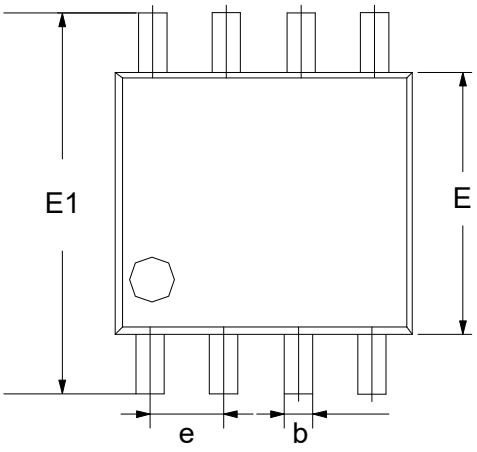
SO-8 (SOIC-8)

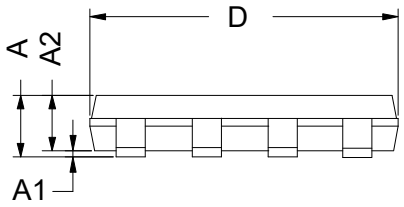


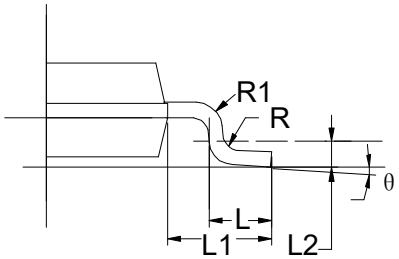
Symbol	Dimensions In Millimeters	
	Min	Max
A1	0.100	0.250
A2	1.300	1.550
b	0.330	0.510
C	0.170	0.250
D	4.780	5.000
E	3.800	4.000
E1	5.800	6.300
e	1.270TYP	
L1	0.400	0.900
θ	0°	8°

Package Outline Dimensions

MSOP-8







Symbol	Dimensions In Millimeters	
	Min	Max
A	0.800	1.200
A1	0.000	0.200
A2	0.750	0.950
b	0.30 TYP	
C	0.15 TYP	
D	2.900	3.100
e	0.65 TYP	
E	2.900	3.100
E1	4.700	5.100
L1	0.400	0.800
θ	0°	6°