Single 16-/14-/12-Bit, Low Power, High Performance DACs

Features

- **Single, 16-/14-/12-Bit Pin Compatible DACs**
  TPC116S1: 16bit
  TPC114S1: 14bit
  TPC112S1: 12bit
- **Low Power Consumption(90μA typ)**
- **Differential Nonlinearity: ±1LSB(max)**
- **Glitch Energy: 0.1nV-s**
- **Power-On Reset to Zero**
- **Supply Range: 2.7V to 5.5V**
- **Buffered Rail-to-Rail Output Operation**
- **Safe Power-On Reset (POR) to Zero DAC Output**
- **Fast 30MHz, 3-Wire, SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Schmitt-Trigger Inputs for Direct Optocoupler Interface**
- **SYNC Interrupt Facility**
- **High Performance Drop-In Compatible With DAC8551,DAC7512**
- **Available in a Tiny MSOP-8 Package**

Applications

- Gain and Offset Adjustment
- 2-Wire Sensors
- Process Control and Servo Loops
- Portable Instrumentation
- Programmable voltage and current sources
- Programmable attenuators
- Automatic Test Equipment

Description

The TPC116S1/TPC114S1/TPC112S1 are pin compatible 12-bit, 14-bit and 16-bit digital-to-analog converter, these series product are single channel, low power, buffered voltage-out DACs and are guaranteed monotonic by design. The devices use a precision external reference applied through the high resistance input for rail-to-rail operation and low system power consumption.

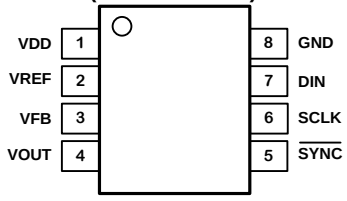
The TPC116S1/TPC114S1/TPC112S1 accepts a wide 2.7V to 5.5V supply voltage range. The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V and remains there until a valid write takes place. The parts contain a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode. The power consumption is 0.45 mW at 5 V, reducing to 1μW in power-down mode.

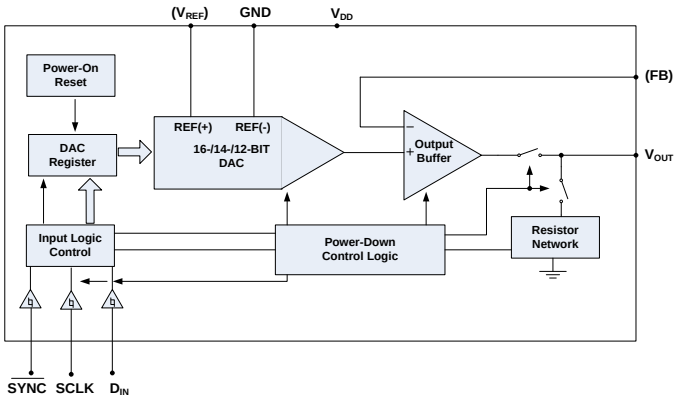
The TPC116S1/TPC114S1/TPC112S1 on-chip precision output amplifier allows rail-to-rail output swing to be achieved. For remote sensing applications, the output amplifier's inverting input is available to the user. The TPC116S1/TPC114S1/TPC112S1 use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The TPC116S1/TPC114S1/TPC112S1 are available in an small size 8-pin MSOP package, all package are specified over the -40°C to +125°C extended industrial temperature range.

Package Information (Top View)

TPC11xS1
8-Pin MSOP
(-V and Suffixes)





Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TPC112S1	TPC112S1-VR	8-Pin MSOP	Tape and Reel, 3,000	112S1
TPC114S1	TPC114S1-VR	8-Pin MSOP	Tape and Reel, 3,000	114S1
TPC116S1	TPC116S1-VR	8-Pin MSOP	Tape and Reel, 3,000	116S1

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ - V^-$ Note 2.....7.0V
Input Voltage..... V^- – 0.3 to V^+ + 0.3
Input Current: +IN, –IN Note 3..... ±20mA
Output Short-Circuit Duration Note 4..... Indefinite
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin MSOP	210	45	°C/W

Electrical Characteristics

(V_{DD} = 5V, V_{REF} = 5V, C_L = 100pF, R_L = 10kΩ, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 5)						
N	Resolution	TPC112S1	12			Bits
		TPC114S1	14			
		TPC116S1	16			
INL	Integral Nonlinearity	TPC112S1 (12-bit) (Note 6)	-4	±0.25	4	LSB
		TPC114S1 (14-bit) (Note 6)	-8	±2	8	
		TPC116S1 (16-bit) (Note 6)	-16	±8	16	
DNL	Differential Nonlinearity	TPC112S1 (12-bit) (Note 6)	-1	±0.05	1	LSB
		TPC114S1 (14-bit) (Note 6)	-1	±0.1	1	
		TPC116S1 (16-bit) (Note 6)	-1	±0.5	1	
OE	Zero Offset Error			6.5	12	mV
	Full-Scale Offset Error		-10	0	10	mV
	Offset-Error Drift			±1		μV/°C
GE	Gain Error		-0.3	±0.13	0.3	%FS
	Gain Temperature Coefficient			±2		ppmFS/°C
REFERENCE INPUT						
V_{REF}	Reference-Input Voltage Range		2		V_{DD}	V
R_{REF}	Reference-Input Impedance			333		kΩ
DAC OUTPUT						
	Output Voltage Range	No load (typical)			V_{REF}	V
		10 kΩ load	0.2		V_{REF}-0.1	
	DC Output Impedance			0.1		Ω
C_L	Capacitive Load (Note 8)	Series resistance = 0Ω			0.1	nF
		Series resistance = 1kΩ			15	μF
R_L	Resistive Load (Note 8)		5			kΩ
	Short-Circuit Current	V_{DD} = 5.5V		35		mA
	Power-Up Time	From power-down mode		25		μs
DIGITAL INPUTS (SCLK, DIN, $\overline{SYNC}$)						
V_{IH}	Input High Voltage	V_{DD} = 5V	2			V
		V_{DD} = 3.3V	1.5			V
V_{IL}	Input Low Voltage	V_{DD} = 5V			0.6	V
		V_{DD} = 3.3V			0.4	V
I_{IN}	Input Leakage Current	V_{IN} = 0V or V_{DD}		±0.1	±1	μA
C_{IN}	Input Capacitance			1		pF

Electrical Characteristics(continued)

(V_{DD} = 5V, V_{REF} = 5V, C_L = 100pF, R_L = 10kΩ, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{HYS}	Hysteresis Voltage			0.15		V
DYNAMIC PERFORMANCE (Note 8)						
SR	Voltage-Output Slew Rate	Positive and negative		1		V/μs
	Voltage-Output Settling Time	1/4 scale to 3/4 scale, to ≤ 0.5 LSB, 14-bit		14		μs
	Reference -3dB Bandwidth	Hex code = 800 (TPC112S1), Hex code = 2000 (TPC114S1), Hex code = 8000 (TPC116S1)		100		kHz
	Digital Feedthrough	Code = 0, all digital inputs from 0V to VDD, SCLK < 50MHz		0.5		nV • s
	DAC Glitch Impulse	Major code transition		2		nV • s
	Output Noise	10kHz		90		nV/ √ Hz
	Integrated Output Noise	0.1Hz to 10Hz		25		μV_{P-P}
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Supply Current	No load; all digital inputs at 0V or V_{DD}, supply current only; excludes reference input current, midscale		90	120	μA
	Power-Down Supply Current	No load, all digital inputs at 0V or V_{DD}		0.4	1	μA

Note 5: Linearity is tested within 20mV of GND and V_{DD}.

Note 6: Gain and offset is tested within 100mV of GND and V_{DD}.

Note 7: Guaranteed by design; not production tested.

Note 8: All timing specifications measured with $V_{IL} = V_{GND}$, $V_{IH} = V_{DD}$.

Serial Write Operation

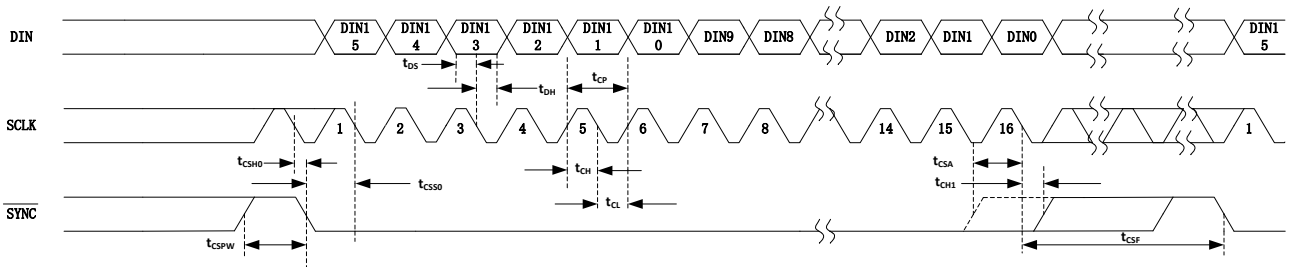


Figure 1. 16-Bit Serial-Interface Timing Diagram (TPC112S1)

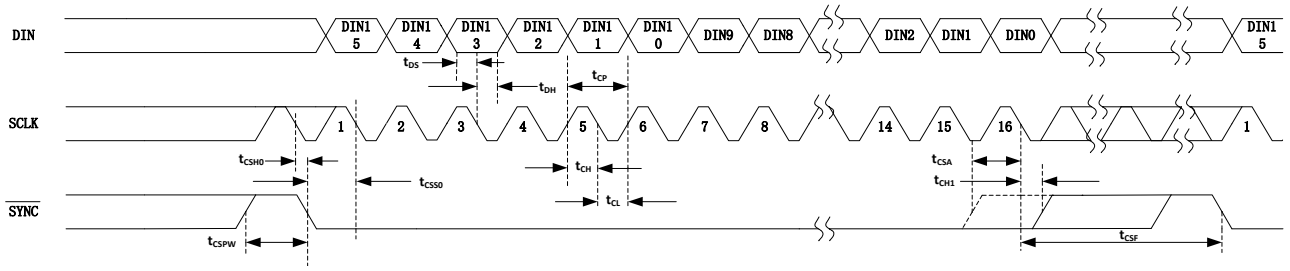


Figure 2. 16-Bit Serial-Interface Timing Diagram (TPC114S1)

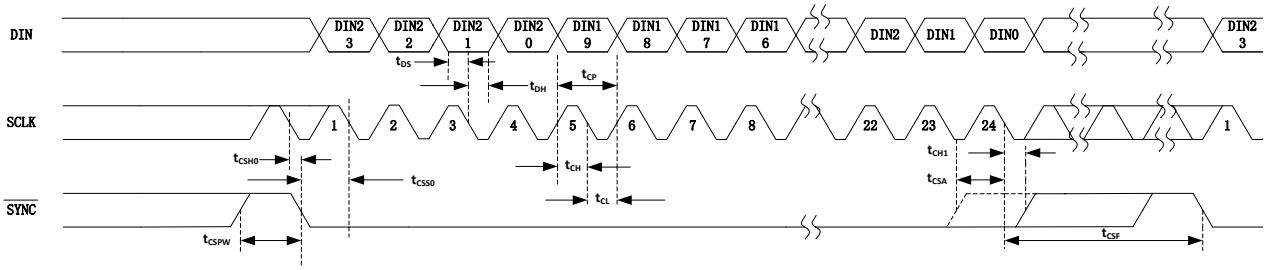


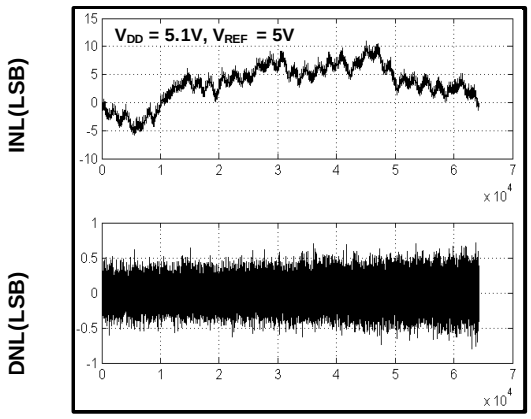
Figure 3. 24-Bit Serial-Interface Timing Diagram (TPC116S1)

TIMING CHARACTERISTICS (Figures 1,2 and 3)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
f_{SCLK}	Serial Clock Frequency		0		30	MHz
t_{CH}	SCLK Pulse-Width High		8			ns
t_{CL}	SCLK Pulse-Width Low		8			ns
t_{CSS0}	$\overline{SYNC}$ Fall to SCLK Fall Setup Time		8			ns
t_{CSH0}	$\overline{SYNC}$ Fall to SCLK Fall Hold Time		0			ns
t_{CSH1}	$\overline{SYNC}$ Rise to SCLK Fall Hold Time		0			ns
t_{CSA}	$\overline{SYNC}$ Rise to SCLK Fall				12	ns
t_{CSF}	SCLK Fall to $\overline{SYNC}$ Fall		100			ns
t_{DS}	DIN to SCLK Fall Setup Time		5			ns
t_{DH}	DIN to SCLK Fall Hold Time		4.5			ns
t_{CSPW}	$\overline{SYNC}$ Pulse-Width High		20			ns
t_{CLPW}	$\overline{SYNC}$ Pulse-Width Low		20			ns
t_{CSC}	$\overline{SYNC}$ Rise to $\overline{SYNC}$ Fall		20			ns

Typical Performance Characteristics

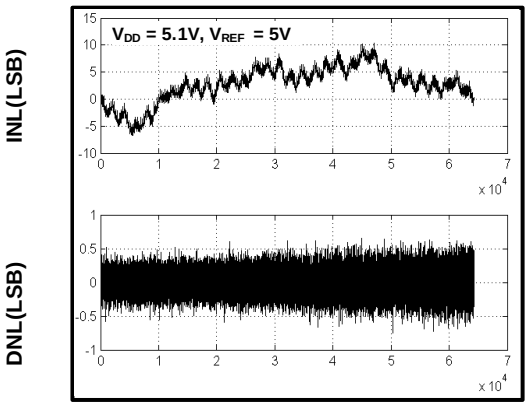
V_S = 5V, At T_A = +25°C, unless otherwise specified

INL and DNL vs. Digital Input Code(+25°C TPC116S1)



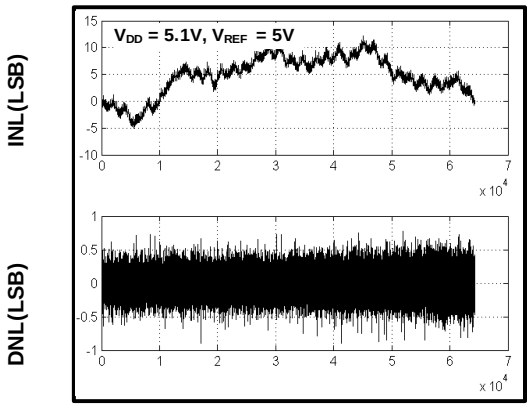
Digital Input Code

INL and DNL vs. Digital Input Code(-40°C TPC116S1)



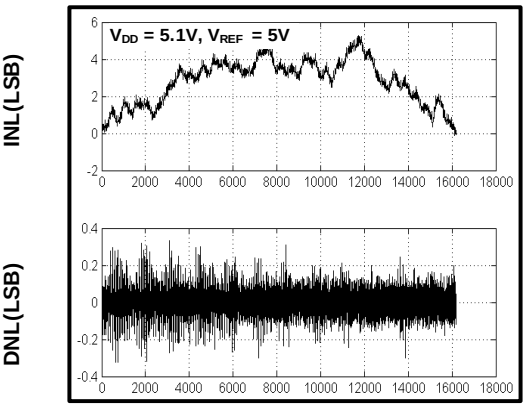
Digital Input Code

INL and DNL vs. Digital Input Code(+105°C TPC116S1)



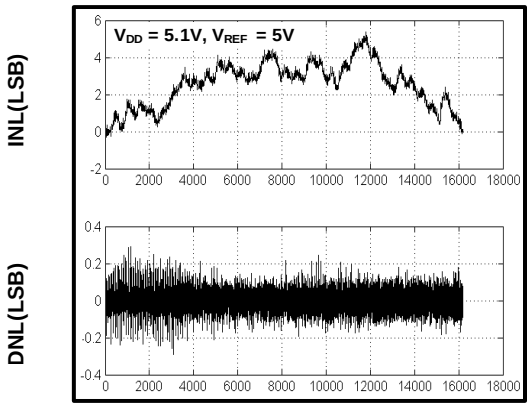
Digital Input Code

INL and DNL vs. Digital Input Code(+25°C TPC114S1)



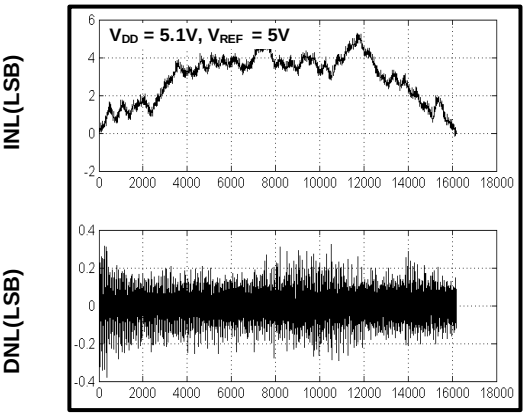
Digital Input Code

INL and DNL vs. Digital Input Code(-40°C TPC114S1)



Digital Input Code

INL and DNL vs. Digital Input Code(+105°C TPC114S1)

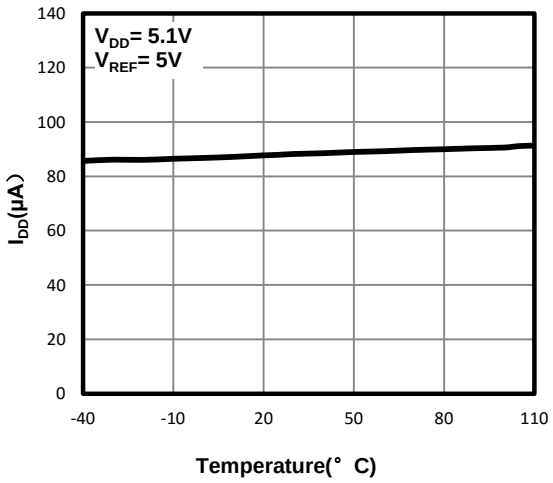


Digital Input Code

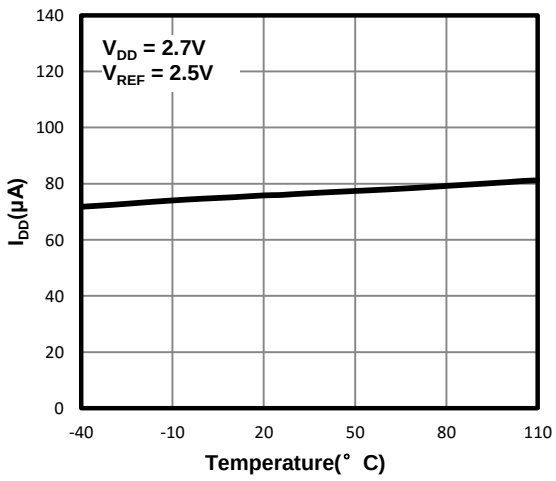
Typical Performance Characteristics

V_S = 5V, At T_A = +25°C, unless otherwise specified

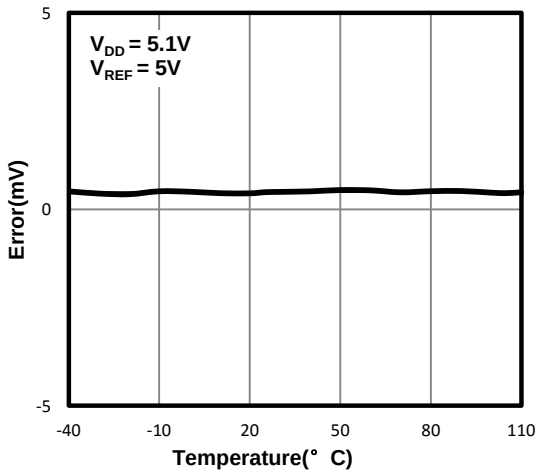
Power-Supply Current vs. Temperature(TPC114S1)



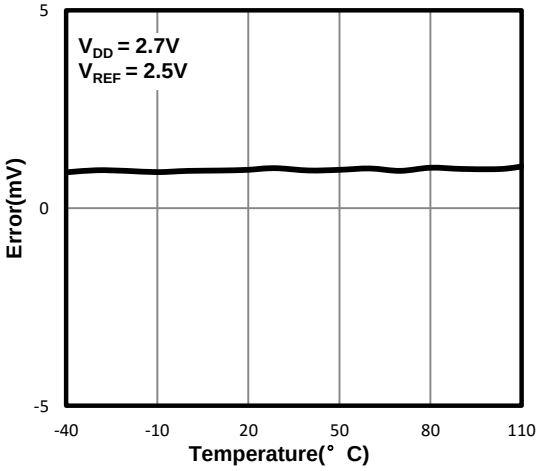
Power-Supply Current vs. Temperature(TPC114S1)



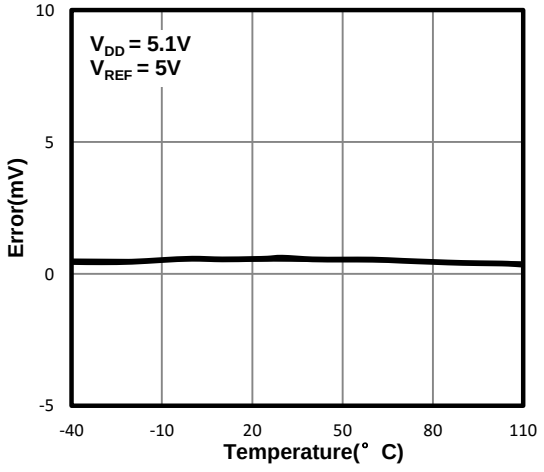
Zero-Scale Error vs. Temperature(TPC114S1)



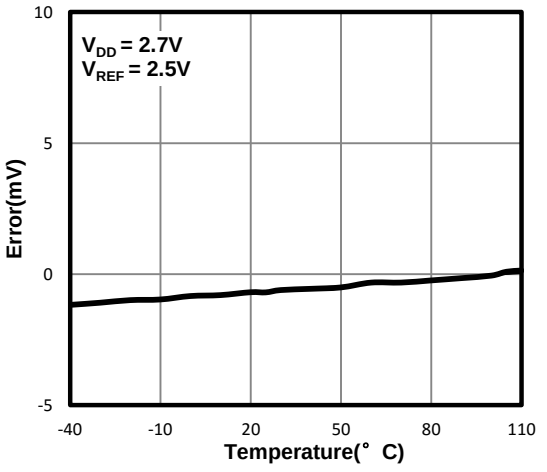
Zero-Scale Error vs. Temperature(TPC114S1)



Full-Scale Error vs. Temperature(TPC114S1)



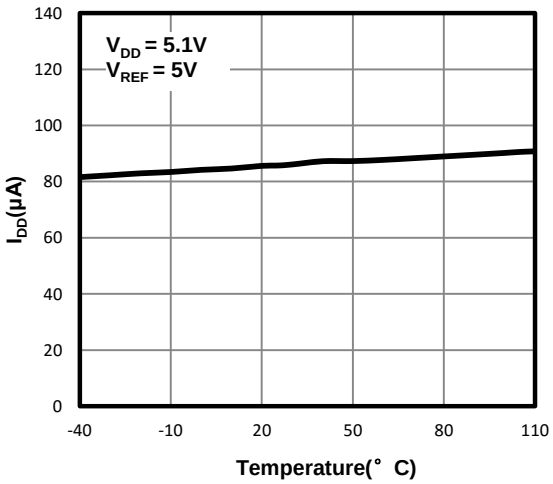
Full-Scale Error vs. Temperature(TPC114S1)



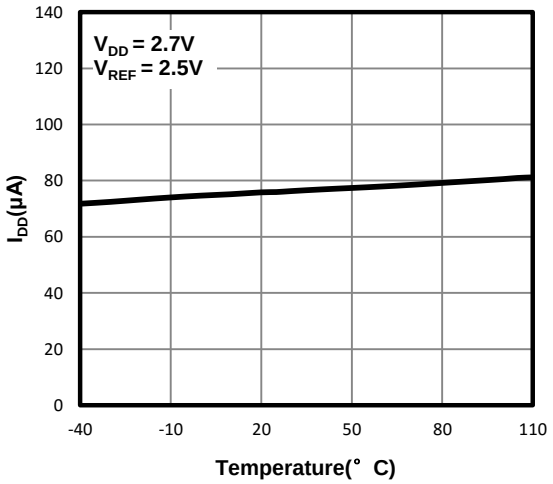
Typical Performance Characteristics

V_S = 5V, At T_A = +25°C, unless otherwise specified

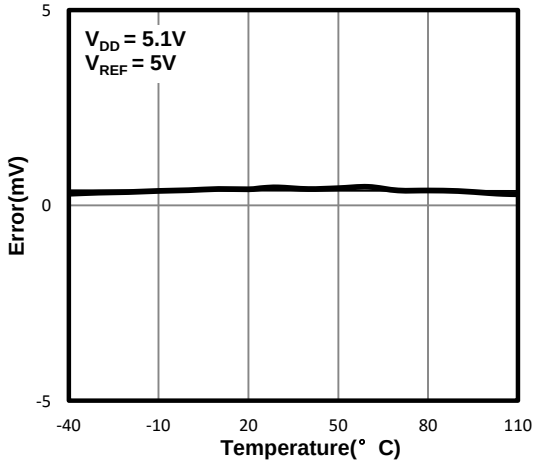
Power-Supply Current vs. Temperature(TPC116S1)



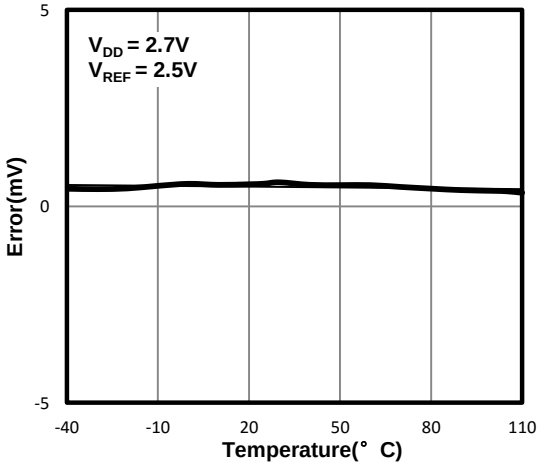
Power-Supply Current vs. Temperature(TPC116S1)



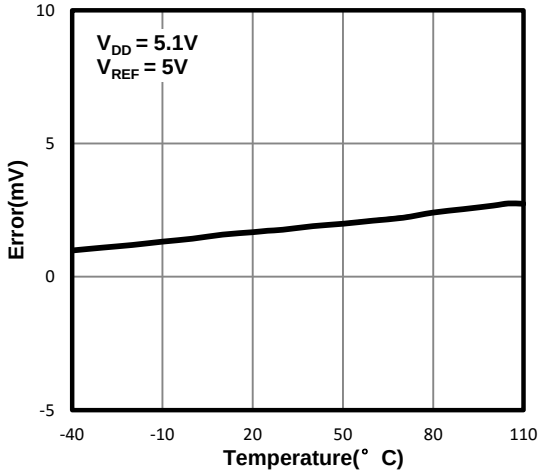
Zero-Scale Error vs. Temperature(TPC116S1)



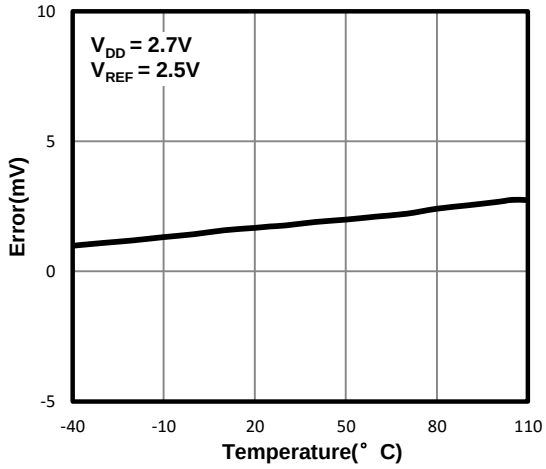
Zero-Scale Error vs. Temperature(TPC116S1)



Full-Scale Error vs. Temperature(TPC116S1)



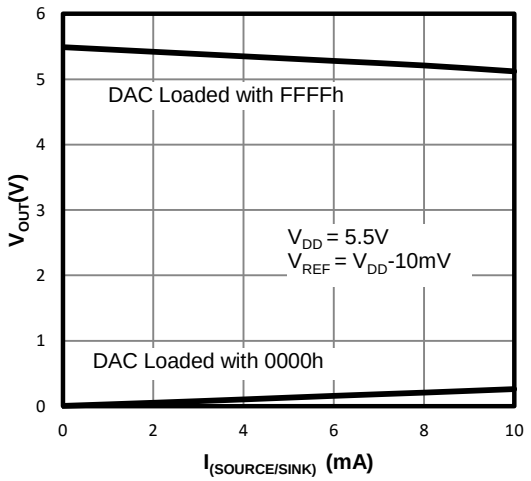
Full-Scale Error vs. Temperature(TPC116S1)



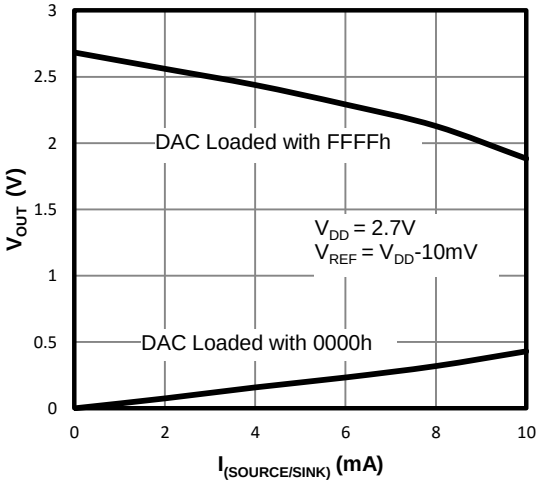
Typical Performance Characteristics

V_S = 5V, At T_A = +25°C, unless otherwise specified

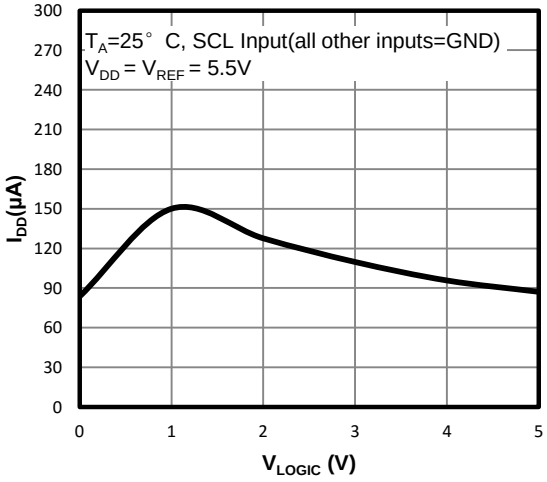
Source and Sink Current Capability(TPC116S1)



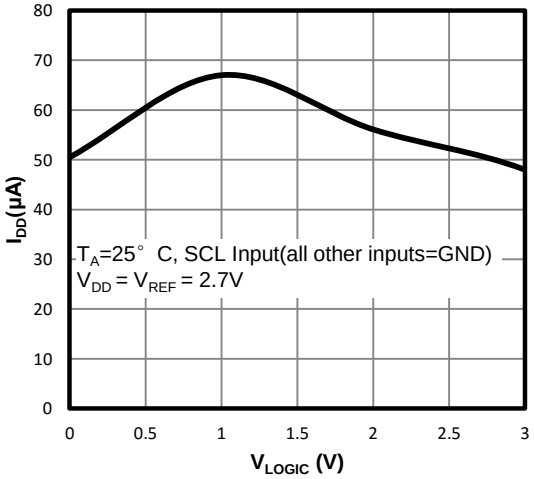
Source and Sink Current Capability(TPC116S1)



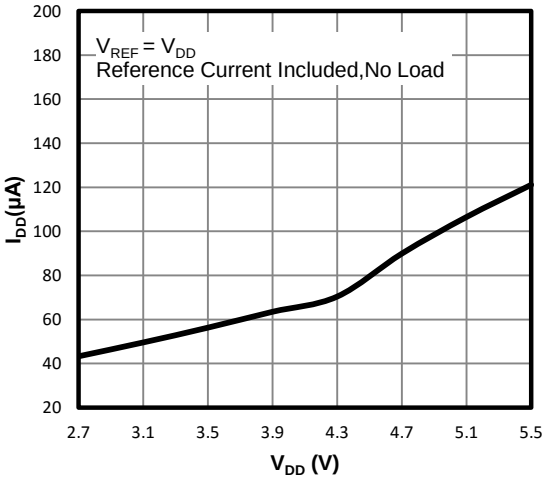
Supply Current vs. Logic Input Voltage(TPC116S1)



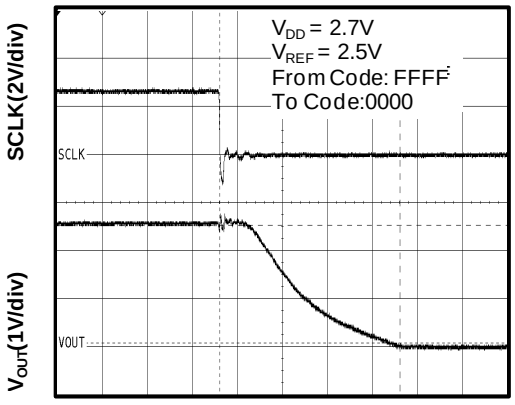
Supply Current vs. Logic Input Voltage(TPC116S1)



Supply Current vs. Supply Voltage(TPC116S1)



Full-Scale Settling Time(2.7V Falling Edge)

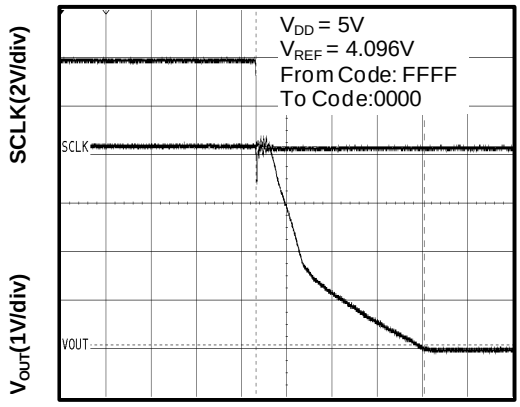


Time (160ns/div)

Typical Performance Characteristics

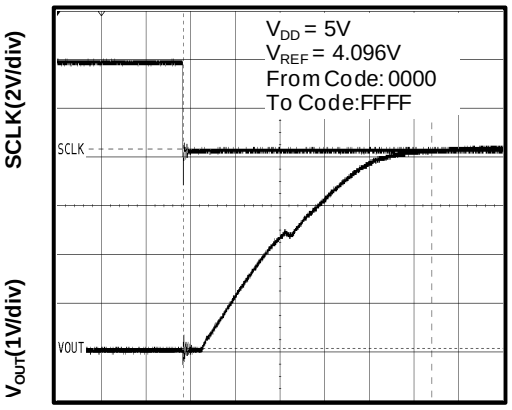
V_S = 5V, At T_A = +25°C, unless otherwise specified

Full-Scale Settling Time(5V Falling Edge)



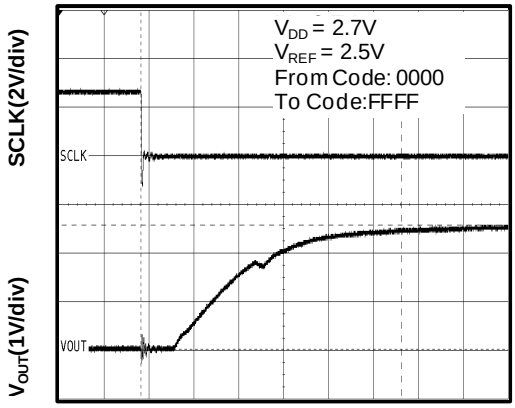
Time (250ns/div)

Full-Scale Settling Time(5V Rising Edge)



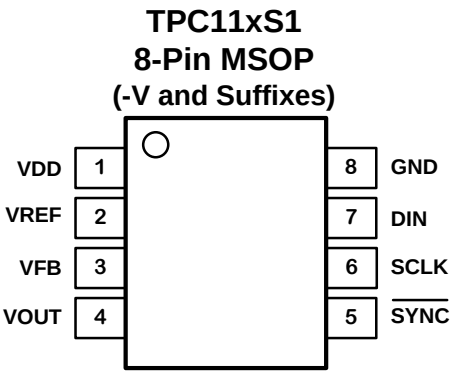
Time (500ns/div)

Full-Scale Settling Time(2.7V Rising Edge)



Time (430ns/div)

Pin Functions



PIN number	PIN name	Function
1	VDD	Power supply input, 2.7V to 5.5V
2	VREF	Reference voltage input.
3	VFB	Feedback connection for the output amplifier. For voltage output operation, tie to VOUT externally.
4	VOUT	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{\text{SYNC}}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th/24th clock (unless $\overline{\text{SYNC}}$ is taken HIGH before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the TPC112S1 and TPC114S1/ TPC116S1). Schmitt-Trigger logic input.
6	SCLK	Serial clock input. Data can be transferred at rates up to 30MHz. Schmitt-Trigger logic input.
7	DIN	Serial data input. Data is clocked into the 16-/24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
8	GND	Ground reference point for all circuitry on the part.

Detailed Description

The TPC116S1/ TPC114S1/TPC112S1 are pin-compatible and software-compatible 12-bit, 14-bit and 16-bit DACs. The TPC116S1/ TPC114S1/TPC112S1 are single-channel, low-power, high-reference input resistance, and buffered voltage-output DACs. The TPC116S1/ TPC114S1/TPC112S1 minimize the digital noise feedthrough from their inputs to their outputs by powering down the SCLK and DIN input buffers after completion of each data frame. The data frames are 16-bit for the TPC114S1/TPC112S1 and 24-bit for the TPC116S1. On power-up, the TPC116S1/ TPC114S1/TPC112S1 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The TPC116S1/ TPC114S1/TPC112S1 contain a segmented resistor string-type DAC, a serial-in/parallel-out shift register, a DAC register, power-on-reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first.

Applications Information

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to V_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 1.8V/μs with a full-scale setting time of 8μs with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin. This configuration allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

DAC Reference (REF)

The external reference input features a typical input impedance of 333kΩ and accepts an input voltage from +2V to VDD. Connect an external voltage supply between REF and GND to apply an external reference.

Serial Interface

The TPC116S1/ TPC114S1/TPC112S1 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSP. The interface provides three inputs: SCLK, $\overline{SYNC}$, and DIN. The chip-select input ($\overline{SYNC}$) frames the serial data loading at DIN. Following a chip-select input high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 16-bit for the TPC114S1/ TPC112S1 and 24-bit for the TPC116S1. The first 2 bits are the control bits followed by 12/14 data bits (MSB first) for the TPC114S1/ TPC112S1 and 22 data bits (MSB first) for the TPC116S1 as shown in Tables 1 and 2. The serial input register transfers its contents to the input registers after loading 16/24 bits of data and updates the DAC output immediately after the data is received on the 16-/24-bit falling edge of the clock. To initiate a new data transfer, drive $\overline{SYNC}$ high and keep $\overline{SYNC}$ high for a minimum of 20ns before the next write sequence. The SCLK can be either high or low between $\overline{SYNC}$ write pulses. Figures 1 and 2 show the timing diagram for the complete 3-wire serial interface transmission. The TPC116S1 DAC code is unipolar binary with VOUT = (code/65,536) x VREF. The TPC114S1 DAC code is unipolar binary with VOUT = (code/16,384) x VREF. The TPC112S1 DAC code is unipolar binary with VOUT = (code/4096) x VREF.

16-BIT WORD																Function
MSB		CONTROL BITS		DATA BITS LSB												
D15	D14	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X	X	0	0	X	X	X	X	X	X	X	X	X	X	X	X	Normal operation
X	X	-	-	X	X	X	X	X	X	X	X	X	X	X	X	Power-down modes
X	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 1kΩ to GND
X	X	1	0	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 100kΩ to GND
X	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	High-Z

Table 1. Operating Mode Truth Table (TPC112S1)

16-BIT WORD																Function
CONTROL BITS		DATA BITS														
MSB		LSB														
PD1	PD0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Normal operation
-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Power-down modes
0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 1kΩ to GND
1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Output typically 100kΩ to GND
1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	High-Z

Table 2. Operating Mode Truth Table (TPC114S1)

24-BIT WORD																Function
CONTROL BITS		DATA BITS														
MSB		LSB														
D23	D22	D21	D20	D19	D18	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D0~D8	
X	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X	Normal operation
X	X	X	X	X	X	-	-	X	X	X	X	X	X	X	X	Power-down modes
X	X	X	X	X	X	0	1	X	X	X	X	X	X	X	X	Output typically 1kΩ to GND
X	X	X	X	X	X	1	0	X	X	X	X	X	X	X	X X	Output typically 100kΩ to GND
X	X	X	X	X	X	1	1	X	X	X	X	X	X	X	X	High-Z

Table 3. Operating Mode Truth Table (TPC116S1)

POWER-ON RESET

The TPC116S1/ TPC114S1/TPC112S1 contains a power-on-reset circuit that controls the output voltage during power up. On power up, the DAC registers are filled with zeros and the output voltages are 0V; they remain that way until a valid write sequence is made to the DAC. The power-on reset is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The TPC116S1/ TPC114S1/TPC112S1 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 1~3 show how the state of the bits corresponds to the mode of operation of the device. When both bits are set to '0', the device works normally with its typical current consumption of 90μA at 5V. However, for the three power-down modes, the supply current falls to 400nA at 5V (250nA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the

amplifier to a resistor network of known values. This configuration has the advantage that the output impedance of the device is known while it is in power-down mode. There are three different options. The output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 4.

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5μs for V_{DD} = 5V, and 5μs for V_{DD} = 3V. See the Typical Characteristics for more information.

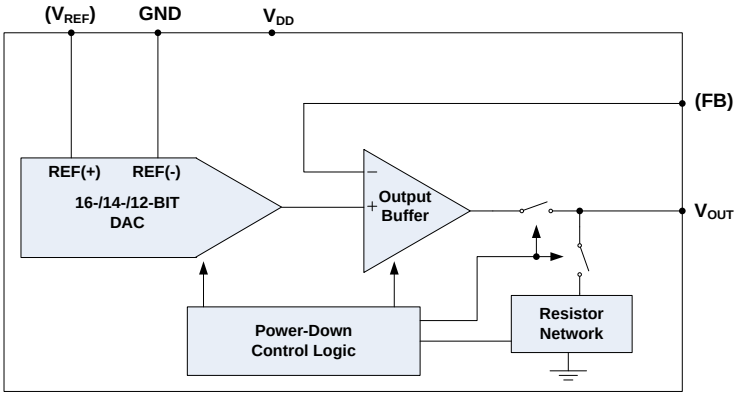
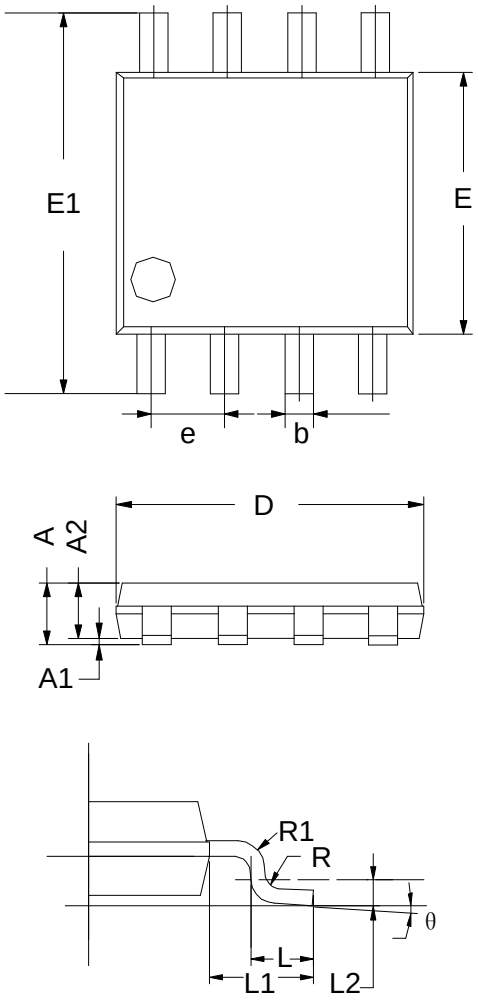


Figure 4. Output Stage During Power-Down

Package Outline Dimensions

MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°