



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Adding PKG type : 32 SOP	Mar.03.2006
Rev. 1.2	Adding PKG type : 32 P-DIP Revised TEST CONDITION of I _{SB1} /I _{DR}	May.14.2007
Rev. 1.3	Deleted L grade Added SL grade Added I _{SB1} /I _{DR} values when T _A = 25°C and T _A = 40°C Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available Added packing type in ORDERING INFORMATION Revised V _{TERM} to V _{T1} and V _{T2} Deleted T _{SOLDER} in ABSOLUTE MAXIMUM RATINGS	Mar.30.2009
Rev. 1.4	Revised PACKAGE OUTLINE DIMENSION in page 10/11/12/13	May.07.2010
Rev. 1.5	Revised ORDERING INFORMATION in page 14	Aug.30.2010
Rev. 1.6	Correct ORDERING INFORMATION Typo.	May.20.2016
Rev. 1.7	Deleted WRITE CYCLE Notes : 1. WE#, CE# must be high or CE2 must be low during all address transitions. in page 7	Jun.28.2016
Rev. 1.8	Revised TEST CONDITION /TYP. /MAX. of I _{CC} Revised to I _{OE} in AC ELECTRICAL CHARACTERISTICS Revised 32-pin SOP & 36-ball TFBGA PACKAGE OUTLINE DIMENSION	May.04.2017

FEATURES

- Fast access time : 45/55/70ns
- Low power consumption:
Operating current : 17/14/11mA (TYP.)
Standby current : 1 μ A (TYP.) LL/SL -version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Green package available**
- Package : 32-pin 450mil SOP
32-pin 600mil PDIP
32-pin 8mm x 20mm TSOP I
32-pin 8mm x 13.4mm sTSP
36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY62L2568 is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

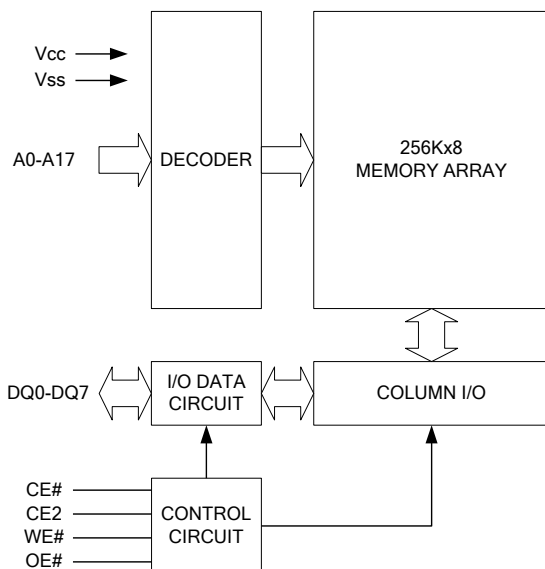
The LY62L2568 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY62L2568 operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible.

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY62L2568	0 ~ 70°C	2.7 ~ 3.6V	45/55/70ns	1 μ A	17/14/11mA
LY62L2568(E)	-20 ~ 80°C	2.7 ~ 3.6V	45/55/70ns	1 μ A	17/14/11mA
LY62L2568(I)	-40 ~ 85°C	2.7 ~ 3.6V	45/55/70ns	1 μ A	17/14/11mA

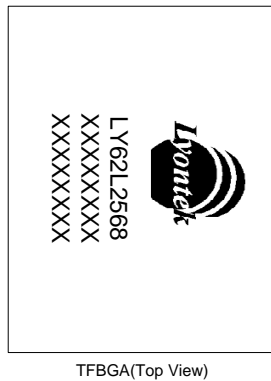
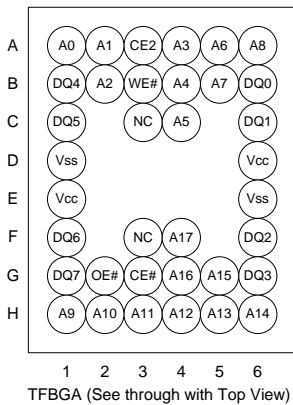
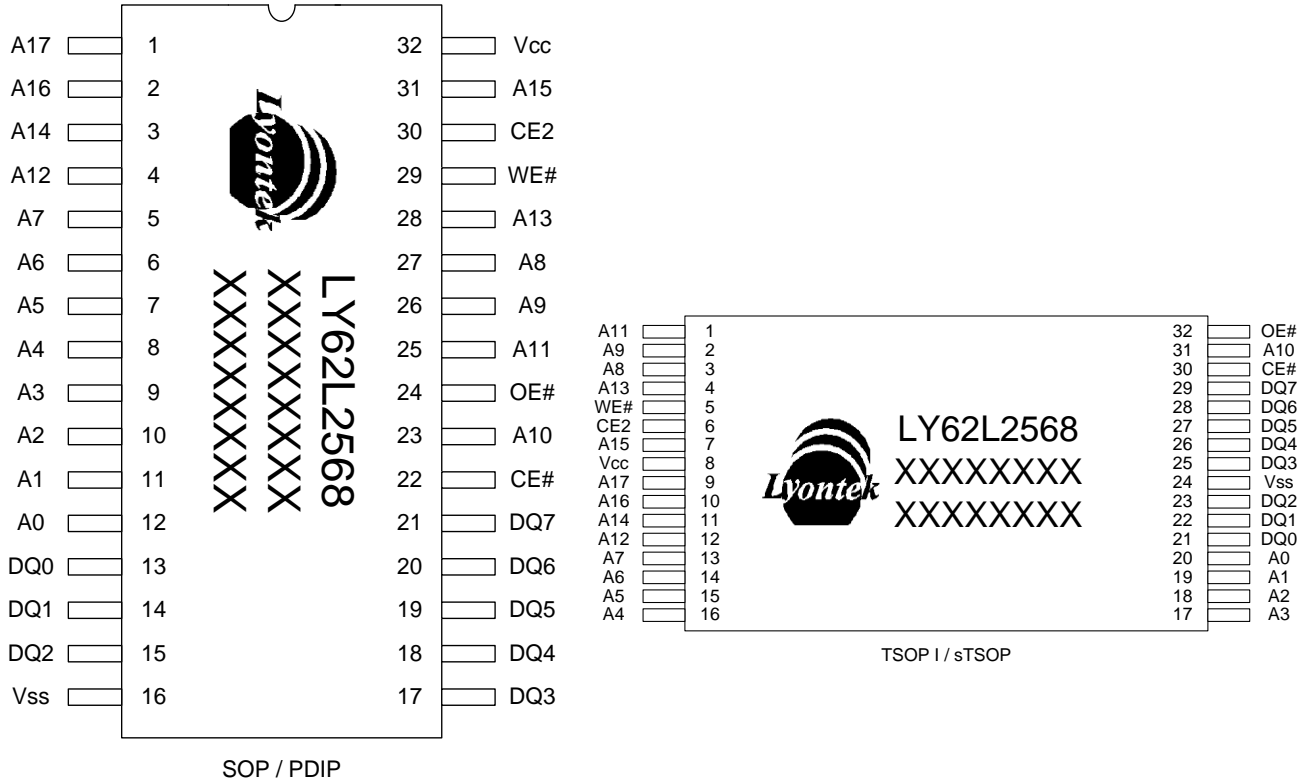
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB} , I _{SB1}
	X	L	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *4	MAX.	UNIT	
Supply Voltage	V _{CC}		2.7	3.0	3.6	V	
Input High Voltage	V _{IH} ^{*1}		2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ^{*2}		- 0.2	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# = 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} - 0.2V	- 45	17	32	mA	
			- 55	14	25	mA	
			- 70	11	20	mA	
	I _{CC1}	Cycle time = 1μs CE# = 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA Other pins at 0.2V or V _{CC} - 0.2V	-	4	5	mA	
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} , other pins at V _{IL} or V _{IH}	-	0.3	0.5	mA	
			I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Others at 0.2V or V _{CC} - 0.2V	LL	1	10
	LLE/LLI	1			20	μA	
	SL ^{*5} SLE ^{*5}	25°C			1	3	μA
	SLI ^{*5}	40°C			1	3	μA
	SL	1	10	μA			
SLE/SLI	1	15	μA				

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
- This parameter is measured at V_{CC} = 3.0V

**CAPACITANCE** ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -1\text{mA}/2\text{mA}$

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	LY62L2568-45		LY62L2568-55		LY62L2568-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	45	-	55	-	70	ns
Chip Enable Access Time	t_{ACE}	-	45	-	55	-	70	ns
Output Enable Access Time	t_{OE}	-	20	-	25	-	30	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	15	-	20	-	25	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

(2) WRITE CYCLE

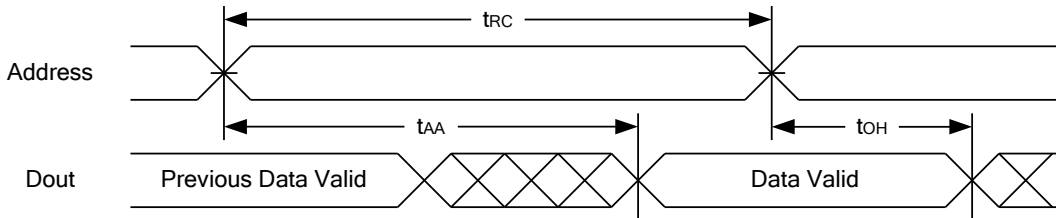
PARAMETER	SYM.	LY62L2568-45		LY62L2568-55		LY62L2568-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	45	-	55	-	70	-	ns
Address Valid to End of Write	t_{AW}	40	-	50	-	60	-	ns
Chip Enable to End of Write	t_{CW}	40	-	50	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	45	-	55	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	15	-	20	-	25	ns

*These parameters are guaranteed by device characterization, but not production tested.

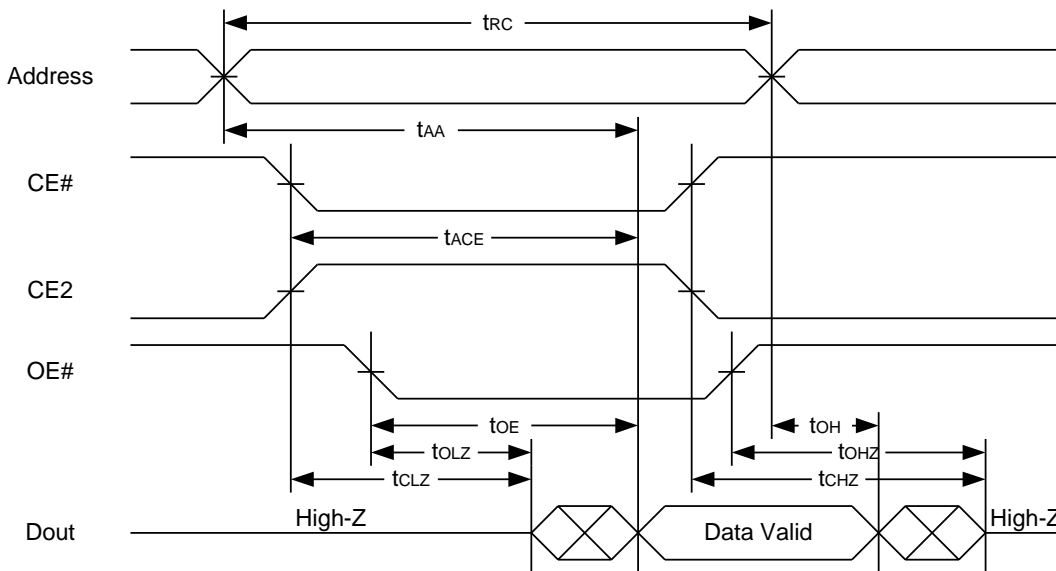


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

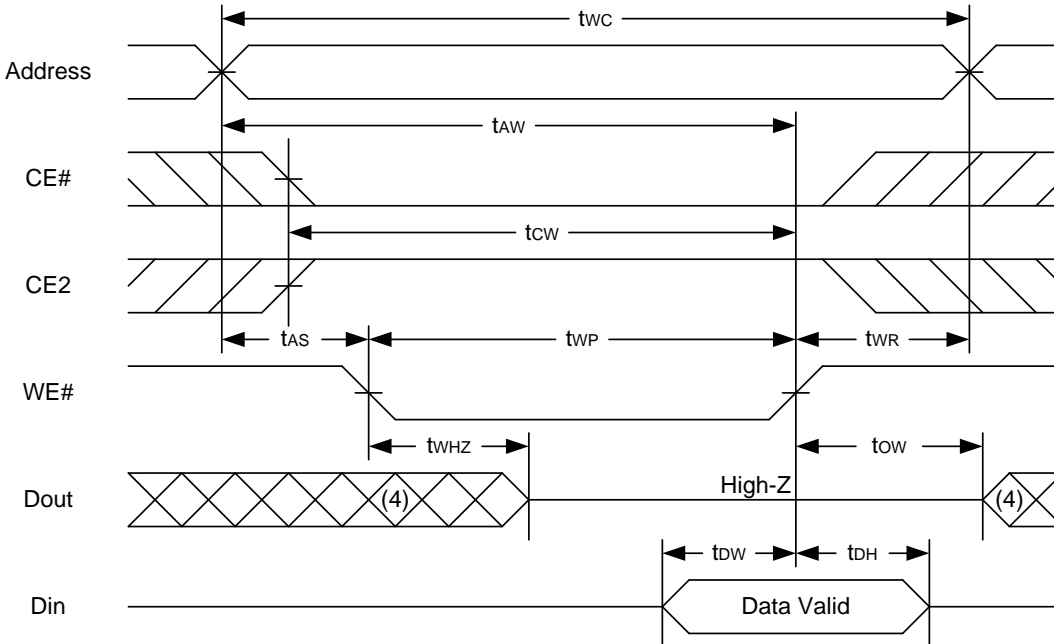
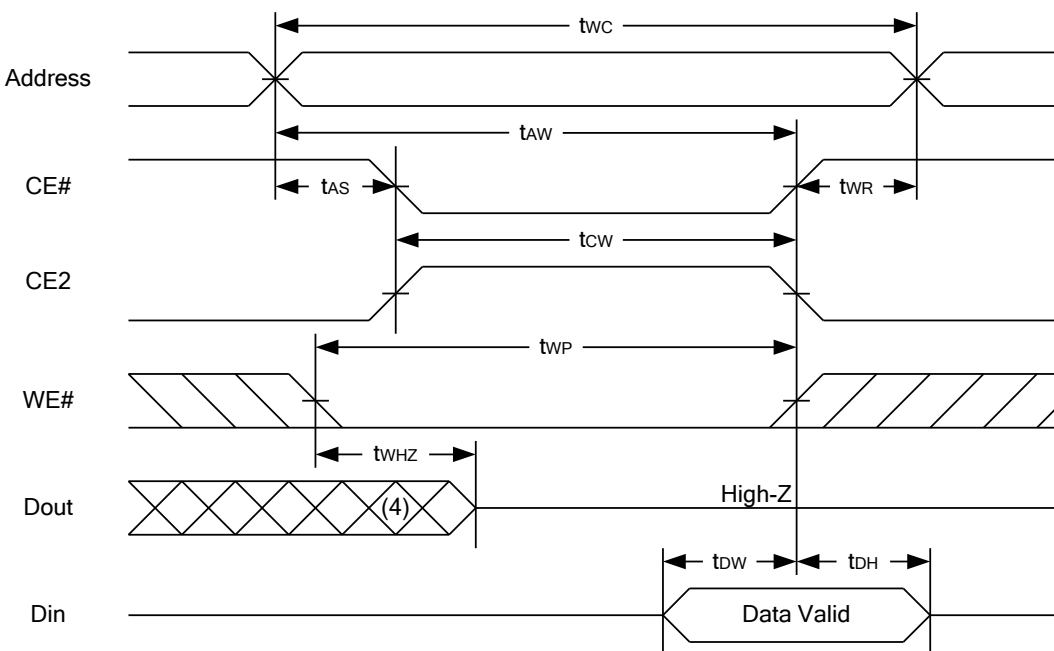


READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

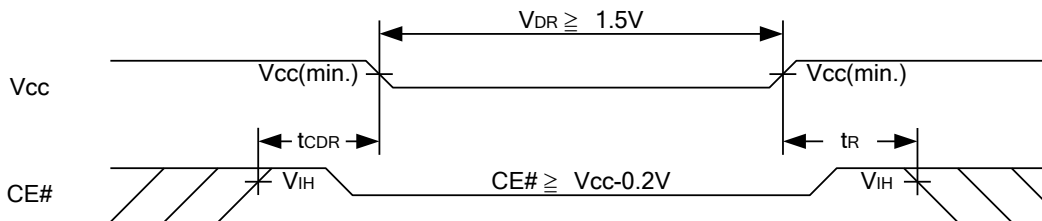
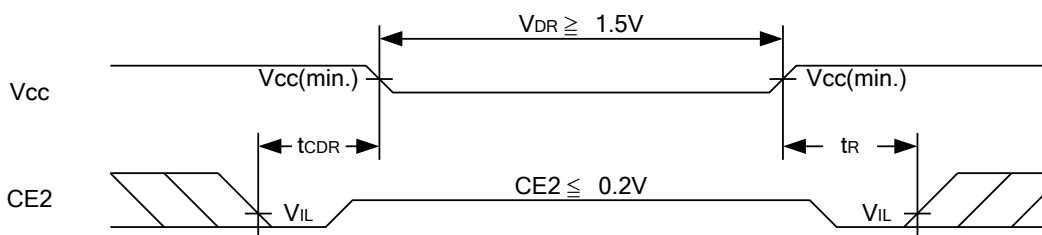
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)

Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	3.6	V		
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	LL	-	0.5	5	μA	
			LLE/LLI	-	0.5	10	μA	
			SL	25°C	-	0.5	3	μA
			SLE	40°C	-	0.5	3	μA
			SLI		-	0.5	5	μA
			SLE/SLI	-	0.5	10	μA	
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns		
Recovery Time	t _R		t _{RC} *	-	-	ns		

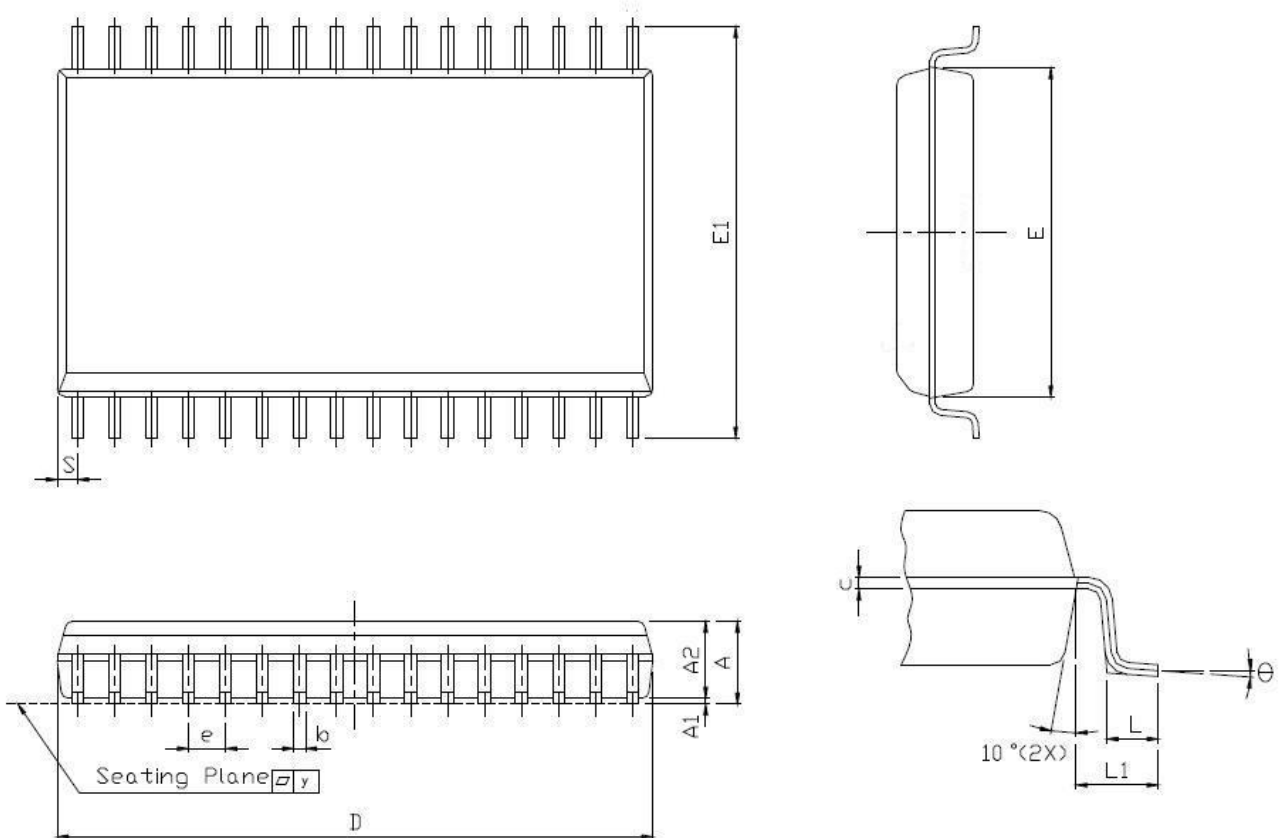
 t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM
Low V_{CC} Data Retention Waveform (1) (CE# controlled)

Low V_{CC} Data Retention Waveform (2) (CE2 controlled)




PACKAGE OUTLINE DIMENSION

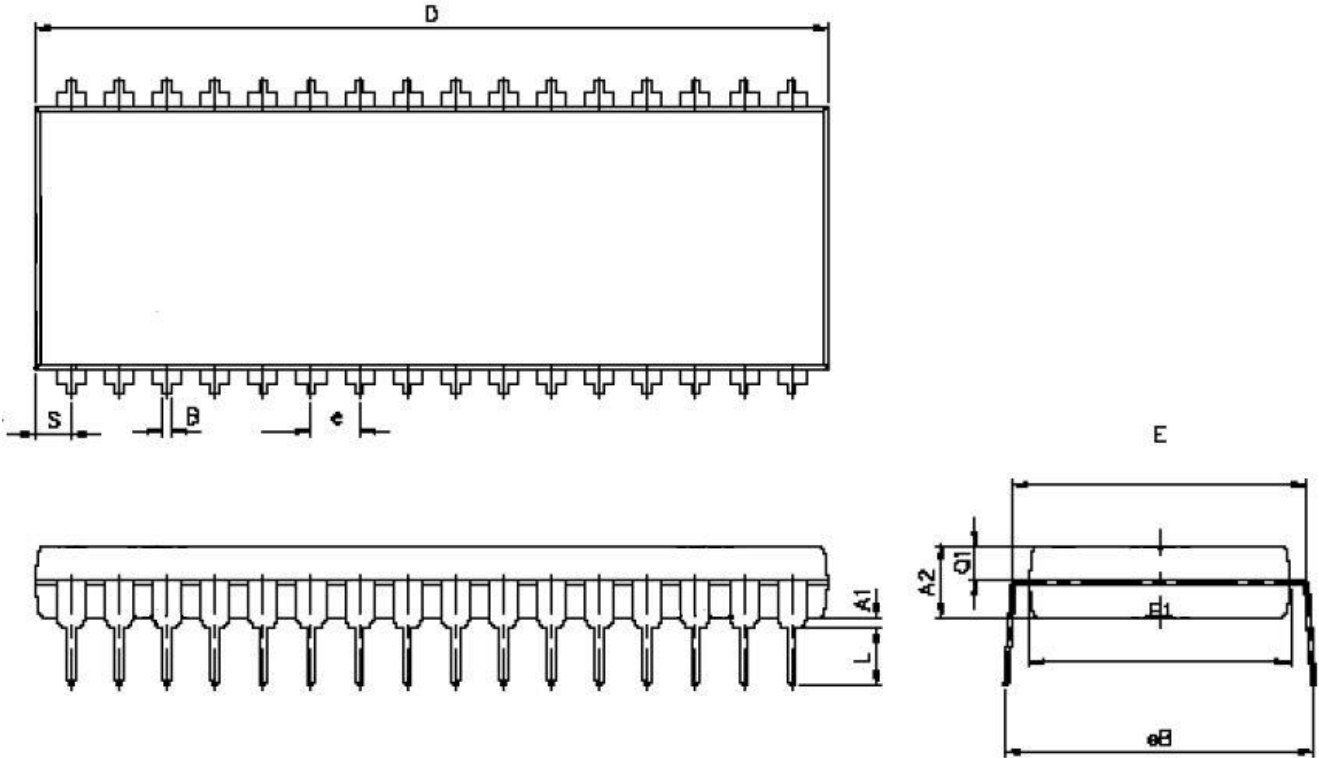
32-pin 450 mil SOP Package Outline Dimension



SYM.	UNIT	
	INCH.(BASE)	MM(REF)
A	0.120(MAX)	3.048(MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.116(MAX)	2.946(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445±0.006	11.303±0.152
E1	0.555±0.025	14.097±0.635
e	0.050(TYP)	1.270(TYP)
L	0.033±0.017	0.838±0.432
L1	0.055±0.008	1.397±0.203
S	0.026(MAX)	0.660(MAX)
y	0.004(MAX)	0.101(MAX)
θ	0° -10°	0° -10°



32-pin 600 mil PDIP Package Outline Dimension

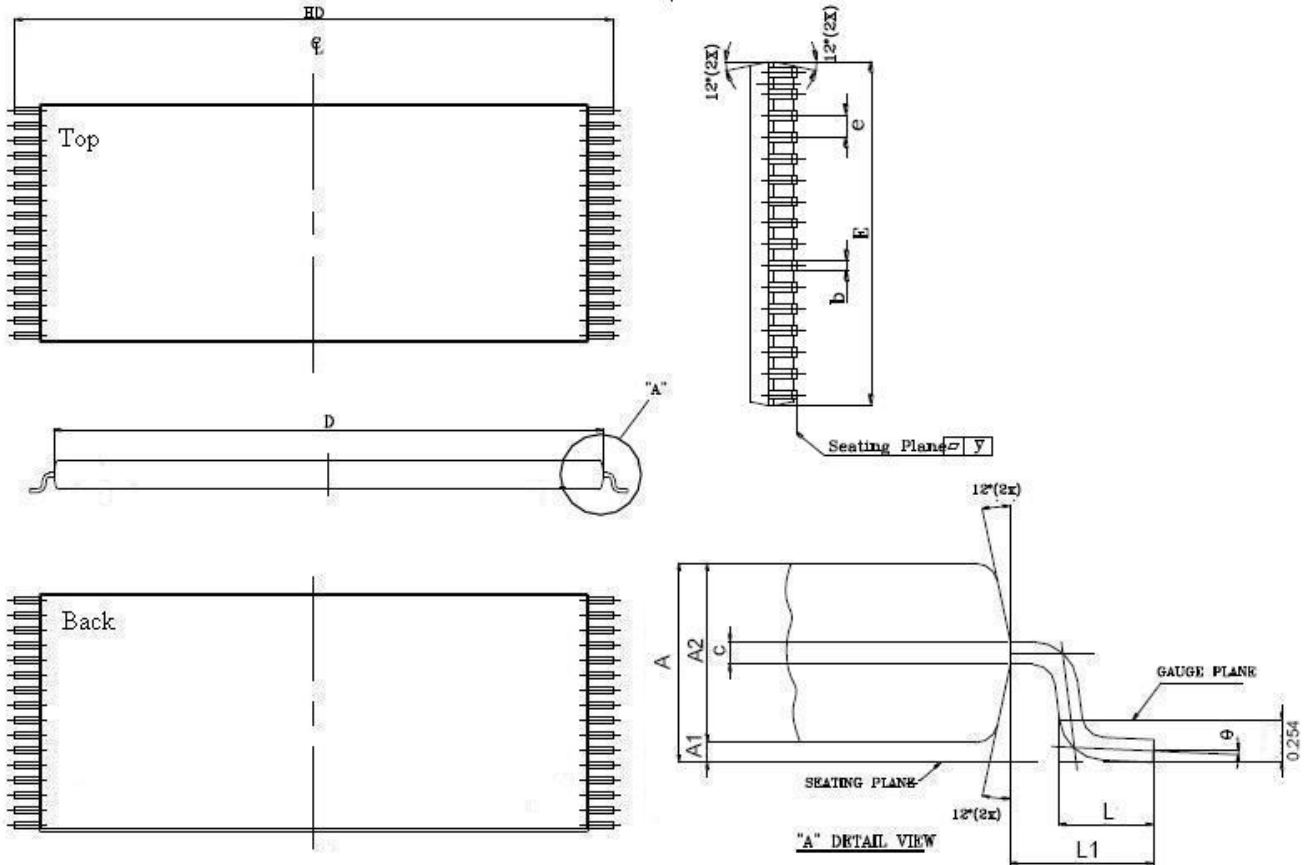


SYM. \ UNIT	INCH(BASE)	MM(REF)
A1	0.015(MIN)	0.381(MIN)
A2	0.155±0.005	3.937±0.127
B	0.018±0.005	0.457±0.127
D	1.650±0.01	41.910±0.254
E	0.600±0.010	15.240±0.254
E1	0.545±0.005	13.843±0.127
e	0.100(TYP)	2.540(TYP)
eB	0.650±0.020	16.510±0.508.
L	0.158±0.043	4.013±1.092
S	0.075±0.010	1.905±0.254
Q1	0.070±0.005	1.778±0.127

Note : D/E1/S dimension do not include mold flash.



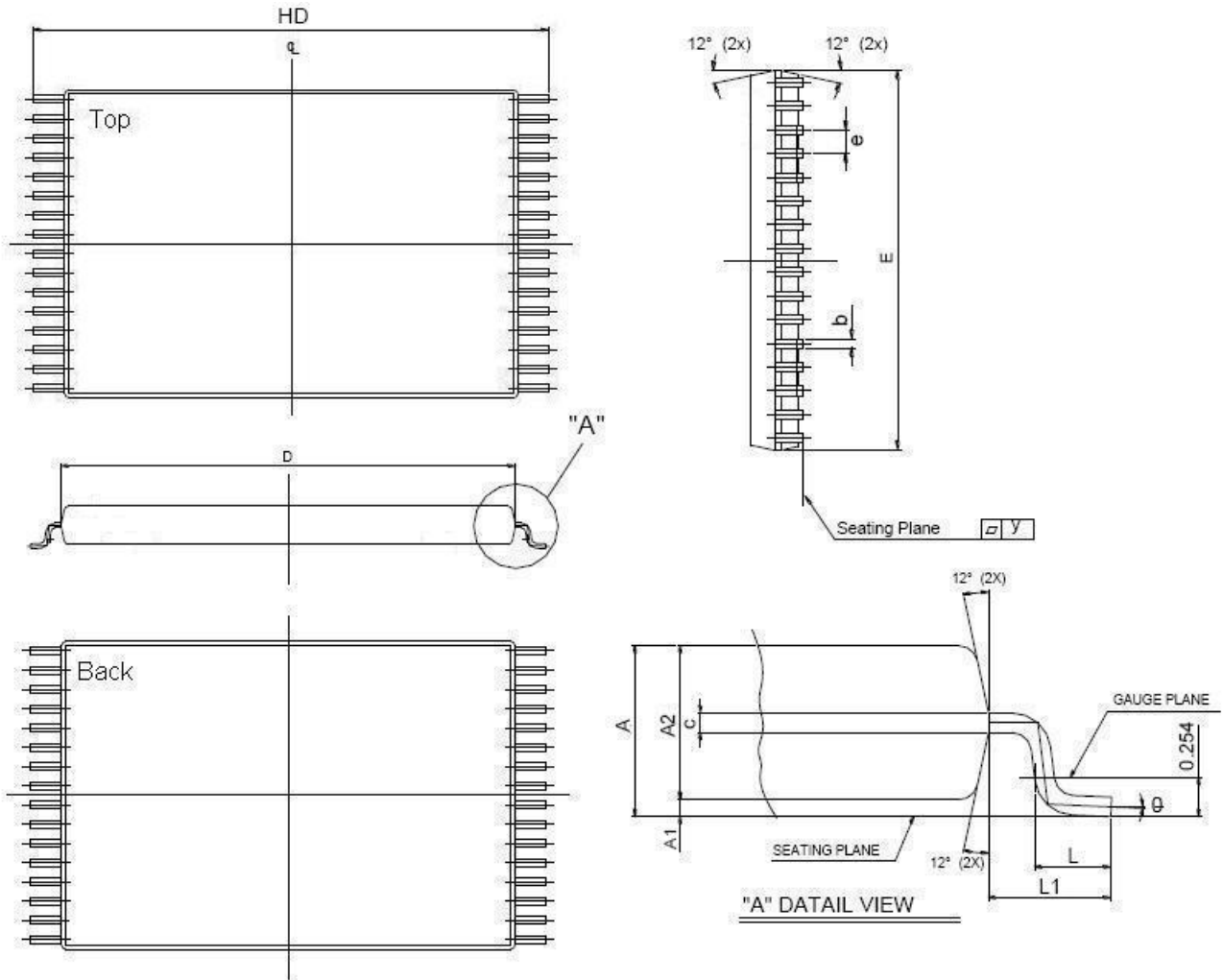
32-pin 8mm x 20mm TSOP I Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.724 ±0.008	18.40 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ±0.008	20.00 ±0.20
L		0.024 ±0.004	0.60 ±0.10
L1		0.0315 ±0.004	0.08 ±0.10
y		0.003 (MAX)	0.08 (MAX)
θ		0°~5°	0°~5°

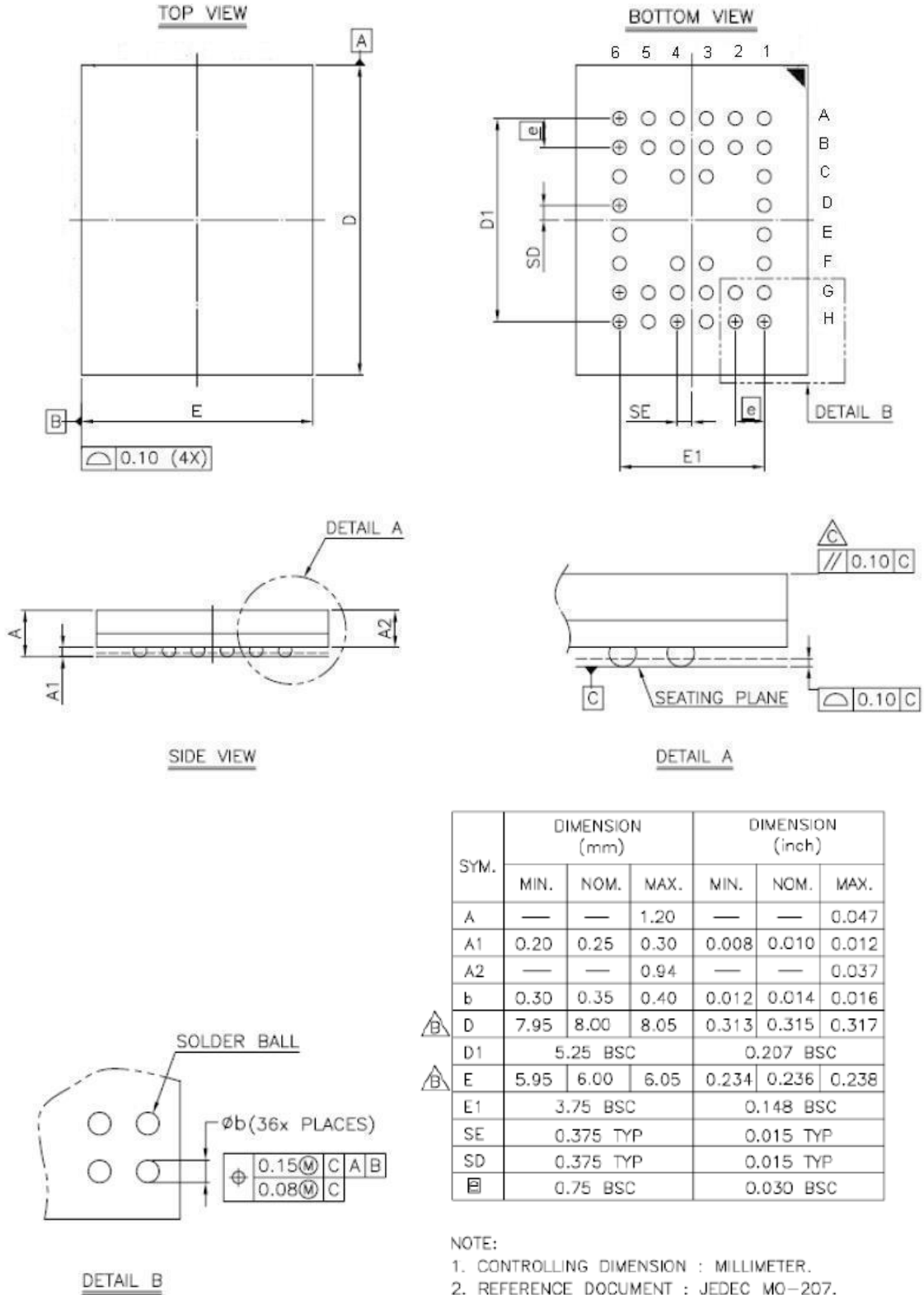


32-pin 8mm x 13.4mm sTSOP Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.009 ±0.002	0.22 ±0.05
c		0.006 ±0.002	0.155 ±0.055
D		0.465 ±0.008	11.80 ±0.20
E		0.315 ±0.008	8.00 ±0.20
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.02 ±0.008	0.50 ±0.20
L1		0.031 ±0.005	0.8 ±0.125
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°

36-ball 6mm x 8mm TFBGA Package Outline Dimension





ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (450mil) SOP	45	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568SL-45SL
				Tape Reel	LY62L2568SL-45SLT
			-20°C~80°C	Tube	LY62L2568SL-45SLE
				Tape Reel	LY62L2568SL-45SLET
			-40°C~85°C	Tube	LY62L2568SL-45SLI
				Tape Reel	LY62L2568SL-45SLIT
		Ultra Low Power	0°C~70°C	Tube	LY62L2568SL-45LL
				Tape Reel	LY62L2568SL-45LLT
			-20°C~80°C	Tube	LY62L2568SL-45LLE
				Tape Reel	LY62L2568SL-45LLET
			-40°C~85°C	Tube	LY62L2568SL-45LLI
				Tape Reel	LY62L2568SL-45LLIT
	55	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568SL-55SL
				Tape Reel	LY62L2568SL-55SLT
			-20°C~80°C	Tube	LY62L2568SL-55SLE
				Tape Reel	LY62L2568SL-55SLET
			-40°C~85°C	Tube	LY62L2568SL-55SLI
				Tape Reel	LY62L2568SL-55SLIT
		Ultra Low Power	0°C~70°C	Tube	LY62L2568SL-55LL
				Tape Reel	LY62L2568SL-55LLT
			-20°C~80°C	Tube	LY62L2568SL-55LLE
				Tape Reel	LY62L2568SL-55LLET
			-40°C~85°C	Tube	LY62L2568SL-55LLI
				Tape Reel	LY62L2568SL-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568SL-70SL	
			Tape Reel	LY62L2568SL-70SLT	
		-20°C~80°C	Tube	LY62L2568SL-70SLE	
			Tape Reel	LY62L2568SL-70SLET	
		-40°C~85°C	Tube	LY62L2568SL-70SLI	
			Tape Reel	LY62L2568SL-70SLIT	
	Ultra Low Power	0°C~70°C	Tube	LY62L2568SL-70LL	
			Tape Reel	LY62L2568SL-70LLT	
		-20°C~80°C	Tube	LY62L2568SL-70LLE	
			Tape Reel	LY62L2568SL-70LLET	
		-40°C~85°C	Tube	LY62L2568SL-70LLI	
			Tape Reel	LY62L2568SL-70LLIT	



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (600mil) PDIP	45	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568PL-45SL
			-20°C~80°C	Tube	LY62L2568PL-45SLE
			-40°C~85°C	Tube	LY62L2568PL-45SLI
		Ultra Low Power	0°C~70°C	Tube	LY62L2568PL-45LL
			-20°C~80°C	Tube	LY62L2568PL-45LLE
			-40°C~85°C	Tube	LY62L2568PL-45LLI
	55	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568PL-55SL
			-20°C~80°C	Tube	LY62L2568PL-55SLE
			-40°C~85°C	Tube	LY62L2568PL-55SLI
		Ultra Low Power	0°C~70°C	Tube	LY62L2568PL-55LL
			-20°C~80°C	Tube	LY62L2568PL-55LLE
			-40°C~85°C	Tube	LY62L2568PL-55LLI
	70	Special Ultra Low Power	0°C~70°C	Tube	LY62L2568PL-70SL
			-20°C~80°C	Tube	LY62L2568PL-70SLE
			-40°C~85°C	Tube	LY62L2568PL-70SLI
Ultra Low Power		0°C~70°C	Tube	LY62L2568PL-70LL	
		-20°C~80°C	Tube	LY62L2568PL-70LLE	
		-40°C~85°C	Tube	LY62L2568PL-70LLI	



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 20mm) TSOP I	45	Special Ultra Low Power	0°C ~70°C	Tray	LY62L2568LL-45SL
				Tape Reel	LY62L2568LL-45SLT
			-20°C ~80°C	Tray	LY62L2568LL-45SLE
				Tape Reel	LY62L2568LL-45SLET
			-40°C ~85°C	Tray	LY62L2568LL-45SLI
				Tape Reel	LY62L2568LL-45SLIT
		Ultra Low Power	0°C ~70°C	Tray	LY62L2568LL-45LL
				Tape Reel	LY62L2568LL-45LLT
			-20°C ~80°C	Tray	LY62L2568LL-45LLE
				Tape Reel	LY62L2568LL-45LLET
			-40°C ~85°C	Tray	LY62L2568LL-45LLI
				Tape Reel	LY62L2568LL-45LLIT
	55	Special Ultra Low Power	0°C ~70°C	Tray	LY62L2568LL-55SL
				Tape Reel	LY62L2568LL-55SLT
			-20°C ~80°C	Tray	LY62L2568LL-55SLE
				Tape Reel	LY62L2568LL-55SLET
			-40°C ~85°C	Tray	LY62L2568LL-55SLI
				Tape Reel	LY62L2568LL-55SLIT
		Ultra Low Power	0°C ~70°C	Tray	LY62L2568LL-55LL
				Tape Reel	LY62L2568LL-55LLT
			-20°C ~80°C	Tray	LY62L2568LL-55LLE
				Tape Reel	LY62L2568LL-55LLET
			-40°C ~85°C	Tray	LY62L2568LL-55LLI
				Tape Reel	LY62L2568LL-55LLIT
70	Special Ultra Low Power	0°C ~70°C	Tray	LY62L2568LL-70SL	
			Tape Reel	LY62L2568LL-70SLT	
		-20°C ~80°C	Tray	LY62L2568LL-70SLE	
			Tape Reel	LY62L2568LL-70SLET	
		-40°C ~85°C	Tray	LY62L2568LL-70SLI	
			Tape Reel	LY62L2568LL-70SLIT	
	Ultra Low Power	0°C ~70°C	Tray	LY62L2568LL-70LL	
			Tape Reel	LY62L2568LL-70LLT	
		-20°C ~80°C	Tray	LY62L2568LL-70LLE	
			Tape Reel	LY62L2568LL-70LLET	
		-40°C ~85°C	Tray	LY62L2568LL-70LLI	
			Tape Reel	LY62L2568LL-70LLIT	



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
32-pin (8mm x 13.4mm) sTSSOP	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568RL-45SL
				Tape Reel	LY62L2568RL-45SLT
			-20°C~80°C	Tray	LY62L2568RL-45SLE
				Tape Reel	LY62L2568RL-45SLET
			-40°C~85°C	Tray	LY62L2568RL-45SLI
				Tape Reel	LY62L2568RL-45SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L2568RL-45LL
				Tape Reel	LY62L2568RL-45LLT
			-20°C~80°C	Tray	LY62L2568RL-45LLE
				Tape Reel	LY62L2568RL-45LLET
			-40°C~85°C	Tray	LY62L2568RL-45LLI
				Tape Reel	LY62L2568RL-45LLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568RL-55SL
				Tape Reel	LY62L2568RL-55SLT
			-20°C~80°C	Tray	LY62L2568RL-55SLE
				Tape Reel	LY62L2568RL-55SLET
			-40°C~85°C	Tray	LY62L2568RL-55SLI
				Tape Reel	LY62L2568RL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L2568RL-55LL
				Tape Reel	LY62L2568RL-55LLT
			-20°C~80°C	Tray	LY62L2568RL-55LLE
				Tape Reel	LY62L2568RL-55LLET
			-40°C~85°C	Tray	LY62L2568RL-55LLI
				Tape Reel	LY62L2568RL-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568RL-70SL	
			Tape Reel	LY62L2568RL-70SLT	
		-20°C~80°C	Tray	LY62L2568RL-70SLE	
			Tape Reel	LY62L2568RL-70SLET	
		-40°C~85°C	Tray	LY62L2568RL-70SLI	
			Tape Reel	LY62L2568RL-70SLIT	
	Ultra Low Power	0°C~70°C	Tray	LY62L2568RL-70LL	
			Tape Reel	LY62L2568RL-70LLT	
		-20°C~80°C	Tray	LY62L2568RL-70LLE	
			Tape Reel	LY62L2568RL-70LLET	
		-40°C~85°C	Tray	LY62L2568RL-70LLI	
			Tape Reel	LY62L2568RL-70LLIT	

**ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
36-ball (6mm x 8mm) TFBGA	45	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568GL-45SL
				Tape Reel	LY62L2568GL-45SLT
			-20°C~80°C	Tray	LY62L2568GL-45SLE
				Tape Reel	LY62L2568GL-45SLET
			-40°C~85°C	Tray	LY62L2568GL-45SLI
				Tape Reel	LY62L2568GL-45SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L2568GL-45LL
				Tape Reel	LY62L2568GL-45LLT
			-20°C~80°C	Tray	LY62L2568GL-45LLE
				Tape Reel	LY62L2568GL-45LLET
			-40°C~85°C	Tray	LY62L2568GL-45LLI
				Tape Reel	LY62L2568GL-45LLIT
	55	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568GL-55SL
				Tape Reel	LY62L2568GL-55SLT
			-20°C~80°C	Tray	LY62L2568GL-55SLE
				Tape Reel	LY62L2568GL-55SLET
			-40°C~85°C	Tray	LY62L2568GL-55SLI
				Tape Reel	LY62L2568GL-55SLIT
		Ultra Low Power	0°C~70°C	Tray	LY62L2568GL-55LL
				Tape Reel	LY62L2568GL-55LLT
			-20°C~80°C	Tray	LY62L2568GL-55LLE
				Tape Reel	LY62L2568GL-55LLET
			-40°C~85°C	Tray	LY62L2568GL-55LLI
				Tape Reel	LY62L2568GL-55LLIT
70	Special Ultra Low Power	0°C~70°C	Tray	LY62L2568GL-70SL	
			Tape Reel	LY62L2568GL-70SLT	
		-20°C~80°C	Tray	LY62L2568GL-70SLE	
			Tape Reel	LY62L2568GL-70SLET	
		-40°C~85°C	Tray	LY62L2568GL-70SLI	
			Tape Reel	LY62L2568GL-70SLIT	
	Ultra Low Power	0°C~70°C	Tray	LY62L2568GL-70LL	
			Tape Reel	LY62L2568GL-70LLT	
		-20°C~80°C	Tray	LY62L2568GL-70LLE	
			Tape Reel	LY62L2568GL-70LLET	
		-40°C~85°C	Tray	LY62L2568GL-70LLI	
			Tape Reel	LY62L2568GL-70LLIT	



Lyontek Inc.

LY62L2568

Rev. 1.8

256K X 8 BIT LOW POWER CMOS SRAM

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