

## P-Channel MOSFET MEM2309S

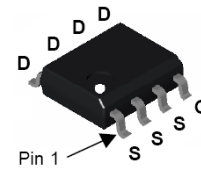
### Description:

MEM2309SG Series P-channel enhancement mode field-effect transistor, produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance.

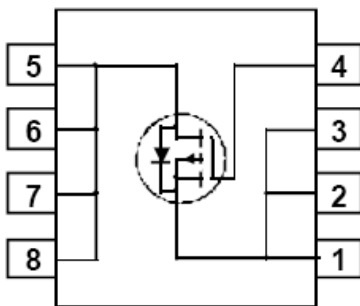
This device particularly suits low voltage applications, and low power dissipation.

### Feature:

- -30V/-6A  
 $R_{DS(ON)} = 53m\Omega @ V_{GS} = -10V, I_D = -6A$   
 $R_{DS(ON)} = 68m\Omega @ V_{GS} = -4.5V, I_D = -4A$
- High Density Cell Design For Ultra Low On-Resistance
- Surface mount package: SOP8



### Pin Configuration:



### Typical Application:

- Power management
- Load switch
- Battery protection

### Absolute Maximum Ratings:

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DSS}$	-30V	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current	$I_D$	$T_A = 25^\circ C$	-6
		$T_A = 70^\circ C$	-3.2
Pulsed Drain Current <sup>1,2</sup>	$I_{DM}$	-30	A
Total Power Dissipation	Pd	$T_A = 25^\circ C$	2
		$T_A = 70^\circ C$	0.8
Operating Temperature Range	$T_{Opr}$	150	$^\circ C$
Storage Temperature Range	$T_{stg}$	-65/150	$^\circ C$

## Thermal Characteristics:

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Ambient <sup>3</sup>	R $\theta$ JA	50	$^{\circ}$ C/W

## Electrical Characteristics:

### MEM2309SG

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250 $\mu$ A	-30	-34		V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 $\mu$ A	-1.1	-1.3	-2	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =20V		5	30	nA
		V <sub>DS</sub> =0V, V <sub>GS</sub> =-20V		-5	-30	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V V <sub>GS</sub> =0V		-6	-300	nA
Static Drain-Source On-Resistance	R <sub>DS(ON)1</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6A	33	53	65	m $\Omega$
	R <sub>DS(ON)2</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	50	68	80	m $\Omega$
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -5.3 A		10		S
Drain-Source Diode Forward Current	I <sub>S</sub>				-2.1	A
Source-drain (diode forward) voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A		-0.8	-1.2	V
Dynamic Characteristics						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0 V, f = 1 MHz		530		pF
Output Capacitance	C <sub>oss</sub>			140		
Reverse Transfer Capacitance	C <sub>rss</sub>			70		
Switching Characteristics						
Turn-On Delay Time	td(on)	V <sub>DD</sub> = -15 V, I <sub>D</sub> =-1 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 6 $\Omega$		8	15	ns
Rise Time	tr			15	25	
Turn-Off Delay Time	td(off)			15	25	
Fall-Time	tf			10	15	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -4A		10	15	nC
Gate-Source Charge	Q <sub>gs</sub>			2.2		
Gate-Drain Charge	Q <sub>gd</sub>			2.0		

- 1、Repetitive rating, pulse width limited by junction temperature.
- 2、Pulse test; pulse width  $\leq$ 300  $\mu$ s, duty cycle  $\leq$ 2%.
- 3、Surface Mounted on FR4 Board, t  $\leq$  10 sec.

## Typical Performance Characteristics:

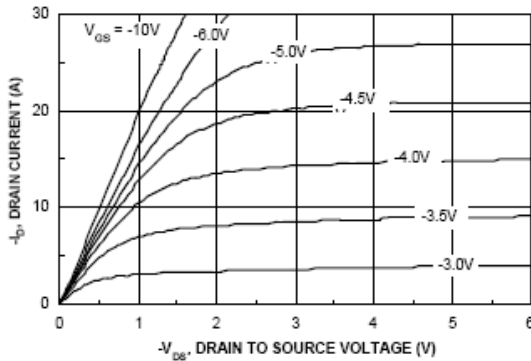


Figure 1. On-Region Characteristics.

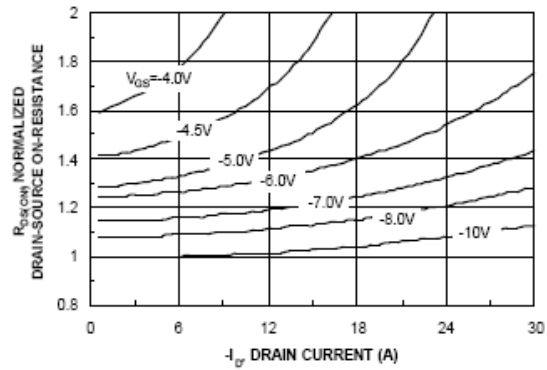


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

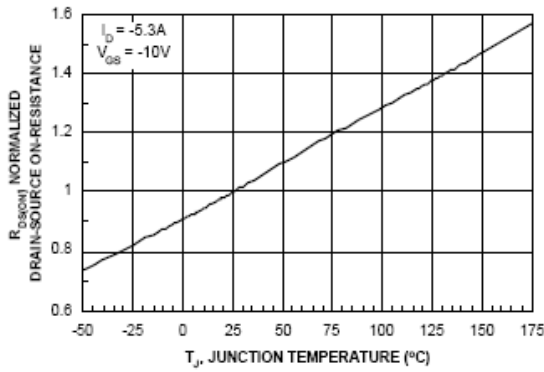


Figure 3. On-Resistance Variation with Temperature.

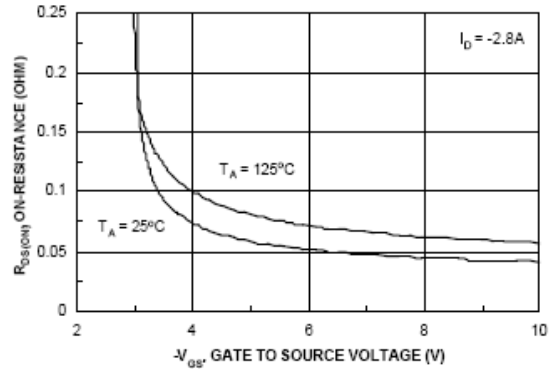


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

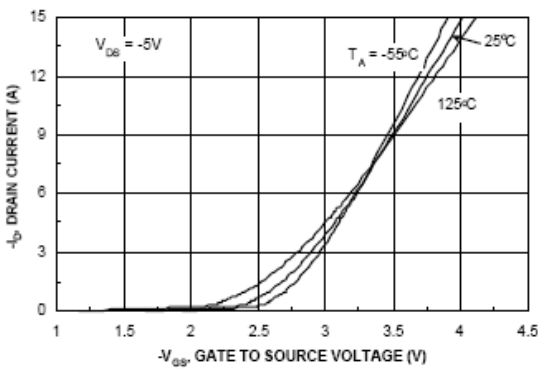


Figure 5. Transfer Characteristics.

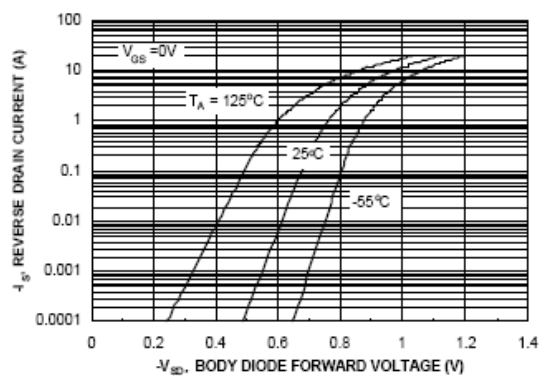
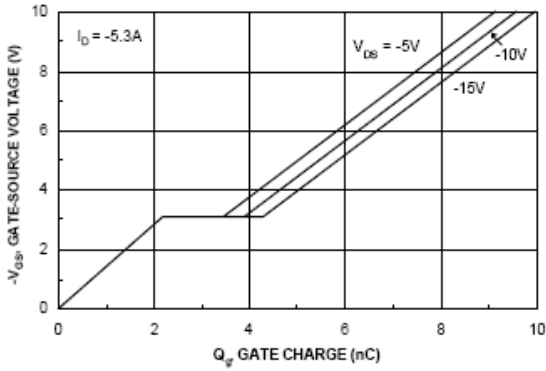
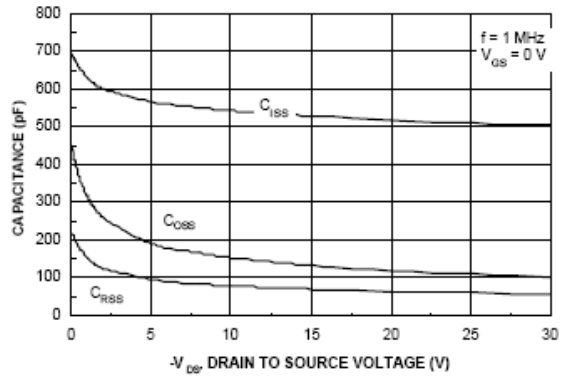


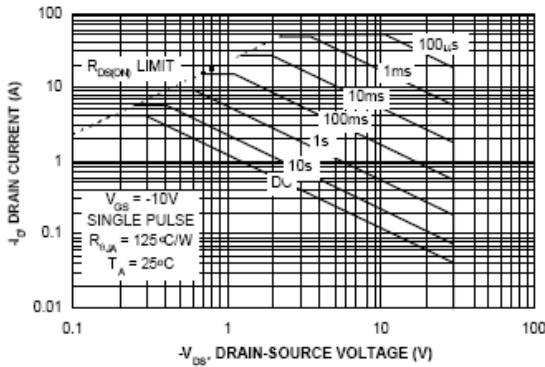
Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.



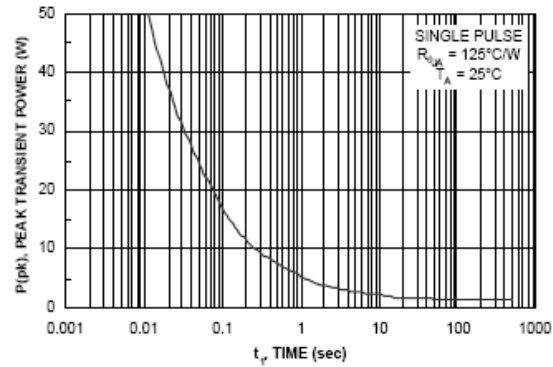
**Figure 7. Gate Charge Characteristics.**



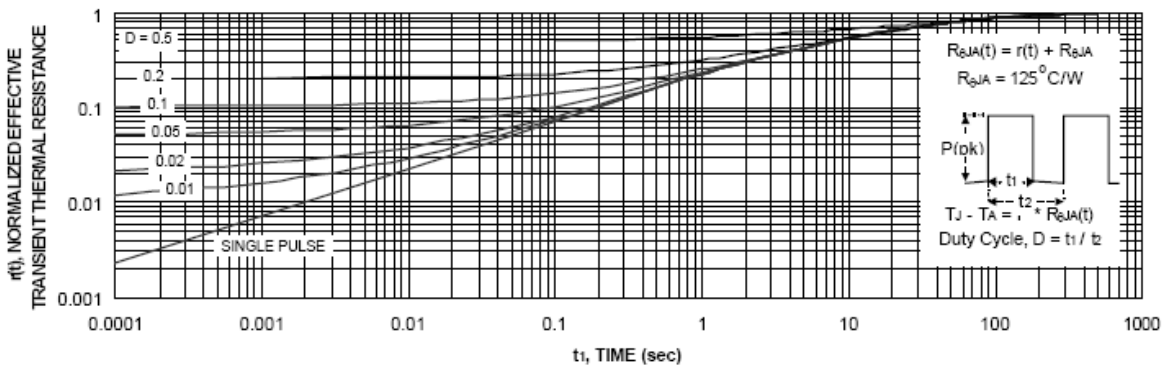
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



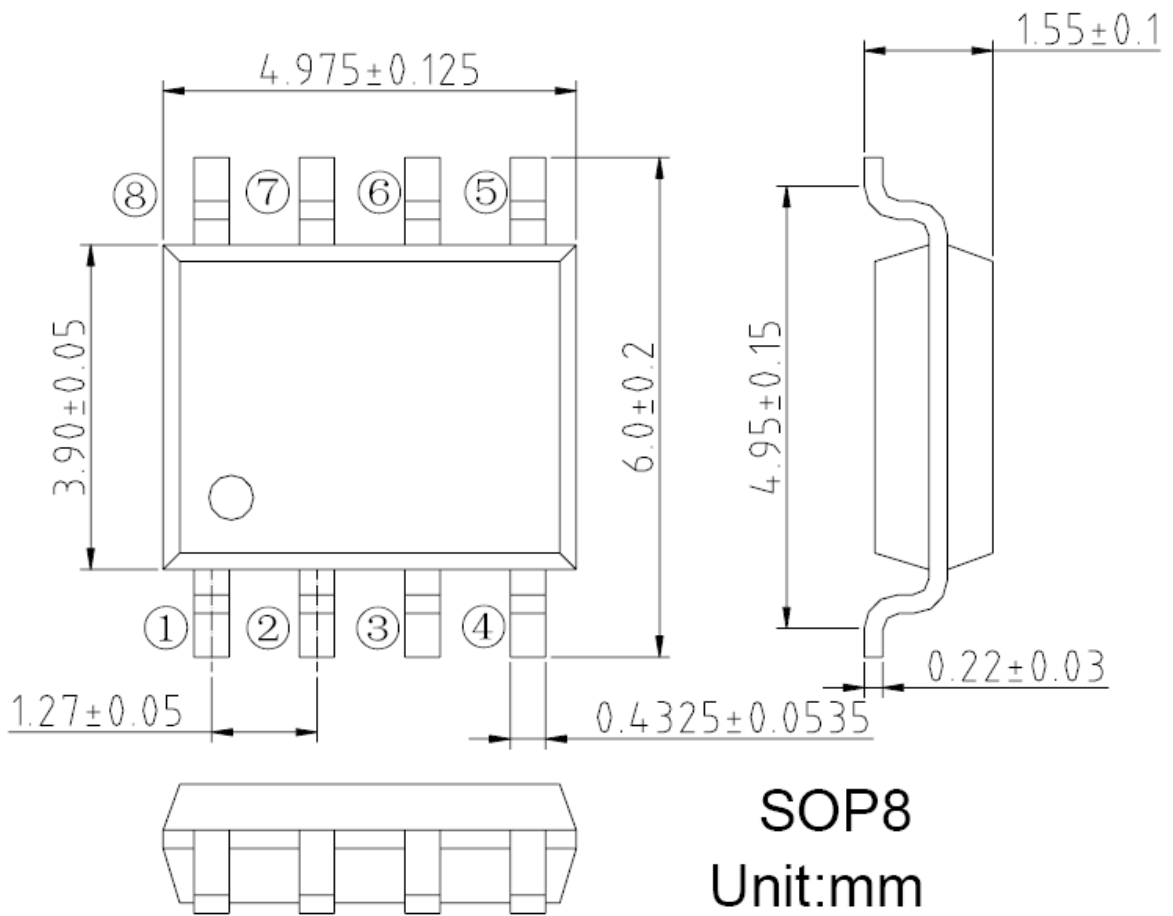
**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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