N3291xUxDN

Data Sheet

ARM926EJ-S Based Media Processor with

Video Decode Accelerator

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1. GENERAL DESCRIPTION

The N3291xUxDN is specially designed for accelerating video stream decoding performance while off-loading the CPU to save power consumption. It is embedded H/W video decoder to deliver high-quality video playback in different formats, like H.264 / MPEG-4 / H.263.

The N3291xUxDN is built on the ARM926EJ-S CPU core and integrated with video encoder, JPEG codec, CMOS image sensor interface, Sound Processing Unit (SPU), ADC, DAC, and TV encoder for meeting various kinds of application needs while saving the BOM cost. The combination of ARM926 @ 300MHz, DDR2, H/W video decoder, and USB2.0 HS Device makes the N3291xU1DN the best choice for high performance media processing devices.

The N3291xU1DN also integrates an AES cipher/de-cipher cryptography engine for stream protection considerations. The stream stored in SD card, SPI NOR Flash, or NAND Flash is encrypted. It is decrypted when the stream is read back and decrypted for playback.

The N32916UxDN is ported with Linux OS to leverage the driver availability of emerging functionalities, like Wi-Fi connectivity. On the other hand, the open source code environment also gives the product development more flexibility. Moreover, hybrid platform is introduced to best utilize the performance advantage at native C programming while enjoying the inherent benefit at application firmware/software development.

Maximum resolution for the N3291xUxDN is D1 (720x480) @ TV output and 1,024x768 @ TFT LCD panel. With increasing popularity of the application image resolution, the N3291xUxDN is the best fit for the application that requires fast turn-around time of development. The N3291xUxDN is well-positioned in the cost effective & high performance media player market where video streams are extensively used.

To reduce system complexity while cutting the BOM cost, the N3291xUxDN is particularly designed with the 128-pin SLQFP MCP (Multi-Chip Package). For N3291xUxDN, the 32Mbitx16 DDR2 chip is stacked inside the MCP to ensure higher performance, lower power consumption and to minimize the system design efforts, like EMI and noise coupling.

The N3291xUxDN is incorporated with a reliable Linux OS kernel and Board Support Package (BSP) to help customers shorten the design cycle time. The fast booting time (under 3 seconds), from power on to application running, is another extra feature to help eliminate power consumption.

1.1 Applications

- e-Reader for kids
- ELA (Educational Learning Aid)
- TV game
- HMI
- Home Applicance
- Advertisement

2. FEATURES

- **CPU**
  - ARM926EJ-S 32-bit RISC CPU with 16KB I-Cache & 16KB D-Cache.
  - Frequency up to 300MHz (worse case).
  - JTAG interface supported for development and debugging.

- **Internal SRAM & ROM**
  - 8KB internal SRAM and 16KB IBR (Internal Booting ROM) supported.
  - IBR booting messages displayed by UART console for debugging.
  - Different system booting modes supported:
    - Memory card
      - SD card
      - SD-to-NAND flash bridge
    - NAND Interface
      - Raw NAND Flash
      - OTP ROM (N23512T / N231GT)
    - SPI Flash
    - USB

- **Memory Controller**
  - SDRAM Interface
    - SDR, DDR, LPDDR & DDR2 type SDRAM supported.
    - Frequency up to 150MHz.
    - 16-bit data bus width supported.
    - 2 external SDRAM banks (2 chip select pins) supported.
    - Total memory size up to 256MB (128MB x 2).

- **EDMA (Enhanced DMA)**
  - Totally 6 DMA channels supported
    - 4 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI.
    - Two dedicated channels for memory-to-memory transfer.
  - Byte, half-word and word data width types supported.
  - Single and burst transfer modes supported.
  - Block transfer supported in memory-to-memory transfer channel.
  - Color format transformation supported in memory-to-memory transfer channel.
    - Source color format could be RGB555, RGB565 and YCbCr422.
    - Destination color format could be RGB555, RGB565 and YCbCr422.
  - Auto reload supported for continuous data transfer.
  - Interrupt generation supported in the half-of-transfer or end-of-transfer.

- **Capture (CMOS Image Sensor I/F)**
  - CCIR601 and CCIR656 interfaces supported for connection to CMOS image sensor.
  - Resolution up to 2M pixels.
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor.
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory.
  - Planar and packet data formats supported for data storing to system memory.
  - Image cropping supported with the cropping window up to 4096x2048.

- Image scaling-down supported.
  - Vertical and horizontal scaling-down for preview mode supported.
    - The scaling factor is N/M.
    - Two pairs of configurable 8-bit N and 8-bit M for vertical and horizontal scaling-down.
    - The value of N has to equal to or less than M.
  - Frame rate control supported.
- Combines two interlace fields to a single frame supported for data in from TV-decoder
- 3 Kinds of color processing effects:
  - Negative picture
  - Sepia picture
  - Posterization

JPEG Codec

- Baseline Sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
- Planar Format
  - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image.
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image.
  - Support to decode YCbCr 4:2:2 transpose format.
  - Support arbitrary width and height image encode and decode.
  - Support three programmable quantization-tables.
  - Support standard default Huffman-table and programmable Huffman-table for decode.
  - Support arbitrarily 1X~8X image up-scaling function for encode mode.
  - Support down-scaling function for encode and decode modes.
  - Support specified window decode mode.
  - Support quantization-table adjustment for bit-rate and quality control in encode mode.
  - Support rotate function in encode mode.
  - Support on-the-Fly interface with video data processor.
- Packet Format
  - Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format.
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image.
  - Support decoded output image RGB555, RGB565 and RGB888 formats.
  - The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards.
  - Support arbitrary width and height image encode and decode.
  - Support three programmable quantization-tables.
  - Support standard default Huffman-table and programmable Huffman-table for decode.
  - Support arbitrarily 1X~8X image up-scaling function for encode mode.
  - Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode.
  - Support specified window decode mode.
  - Support quantization-table adjustment for bit-rate and quality control in encode mode.
  - Support on-the-Fly interface with video data processor.
  - Support Scatter-Gather mode for output frame buffer.

- **Video Decoder**
  - Support H.264 AVC baseline profile level-3 and compliant with ISO/IEC 14496-10 visual standard, SVGA (800x600) @ 30fps.
  - Support MPEG-4 part-II simple profile level-3 decoder and compliant with ISO/IEC 14496-2 visual standard, SVGA (800x600) @ 30fps.
  - Support H.263 P3 decoder, SVGA (800x600) @ 30fps.
  - Support Sorenson Spark decoder, D1 (720x480) @ 30fps.
  - Support real-time 30fps video decompression and resolution can up to 720×480.
  - Error resilience: Slice Resynchronization, Data Partitioning and Reversible VLC.

- **VPOST**
  - 8/16/18/24-bit SYNC type and 8/9/16/18/24-bit MPU type TFT LCD supported.
  - Color format supported:
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in.
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out.
  - XGA (1024x768), SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (320x480) resolution supported.
    - The maximum resolution is up to D1 (720X480) for TV output.
    - The maximum resolution is up to 1024X768 for TFT LCD panel.
  - Display scaler – to fit different size of LCD panels.
    - Horizontal: At most 4.0x scale.
    - Vertical: At most 3.0x scale.
  - For SYNC type LCD:
    - For 8-bit bus
      - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported.
      - CCIR601 RGB Dummy mode (NTSC/PAL) supported.
      - CCIR656 interface supported.
      - RGB Through mode supported.
    - For 16/18/24-bit bus
      - Parallel pixel data output mode (1-pixel/1-clock).
  - NTSC/PAL interlace & non-interlace output supported.
  - Color format transform supported:
    - Color format transform between YCbCr422 and RGB565.
    - Color format transform from YCbCr422 to RGB888.
  - TV encoder supported.
  - Dual screen, outputs to TV and LCDwith same content, supported.
    - LCD panel should be 320X240 MPU-type, or 8-bit SYNC-type LCD panel with TV timing
  - Notch filter for NTSC supported to remove the rainbow color effect.
  - Support OSD function to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

- **SPU (Sound Processing Unit)**
  - 7-bit volume control supported.
  - 5-bit pan control supported.
  - 10-band equalizer supported.
  - 13-bit DFA supported for source sampling rate control.

- **Audio DAC**

- 16-bit stereo DAC supported with headphone driver output.
- H/W volume control supported.
- Built-in PLL for supporting various sampling rate.

- **I2S Controller**
  - I2S interface supported to connect external audio codec.
  - 16/18/20/24-bit data format supported.

- **Storage Interface Controller**
  - Interface to NAND Flash:
    - 8-bit data bus width supported.
    - SLC and MLC type NAND Flash supported.
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported.
    - ECC4, ECC8, ECC12, ECC15 and ECC24 algorithm supported for ECC generation, error detection and error correction.
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards supported.
    - SD-to-NAND flash bridge supported.
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD.

- **USB Device Controller**
  - USB2.0 HS (High-Speed) x 1 port.
  - 6 configurable endpoints supported.
  - Control, Bulk, Interrupt and Isochronous transfers supported.
  - Suspend and remote wakeup supported.

- **USB Host Controller**
  - USB1.1 Host x 2 ports.
  - Fully compliant with USB Revision 1.1 specification.
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible.
  - Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported.
  - Control, Bulk, Interrupt and Isochronous transfers supported.

- **Timer & Watch-Dog Timer**
  - Two 32-bit with 8-bit pre-scalar timers supported.
  - One programmable 24-bit Watch-Dog Timer supported.

- **PWM**
  - 4 PWM channel outputs supported.
  - 16-bit counter supported for each PWM channel.
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels.
  - Two clock-dividers supported and each divider shared by two PWM channels.
  - Two Dead-Zone generators supported and each generator shared by two PWM channels.
  - Auto reloaded mode and one-shot pulse mode supported.
  - Capture function supported.

- **UART**
  - A high speed UART supported:
    - Baud rate is up to 1M bps.
    - 4 signals TX, RX, CTS and RTS supported.
  - A normal UART supported:
    - Baud rate is up to 115.2K bps.
    - 2 signals TX and RX supported only.

- **SPI**
  - Two SPI interfaces are supported.
    - Both master and slave mode are supported in SPI interface 0.
    - Only master mode is supported in SPI interface 1.
      - Byte transfer with configurable stop interval supported.

- **I2C**
  - One I2C channel supported.
  - Compatible with Philips's I^2C standard and only master mode supported.
  - Multi-master operation supported.

- **Advanced Interrupt Controller**
  - Total 32 interrupt source supported.
  - Configurable interrupt type:
    - Low-active level triggered interrupt.
    - High-active level triggered interrupt.
    - Low-active edge (falling edge) triggered interrupt.
    - High-active edge (rising edge) triggered interrupt.
  - Individual interrupt mask bit for each interrupt source.
  - 8 different priority levels supported.
  - Daisy-chain priority mechanism supported for interrupts with same priority level.
  - Low priority interrupt automatic masking supported for interrupt nesting.

- **RTC**
  - Independent power plane supported
  - Dual clock source are supported, accurate 32.768 KHz crystal oscillation circuit and built-in coarse 32KHz RC-oscillator.
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported.
  - Alarm supported (second, minute, hour, day, month and year).
  - 12/24-hour mode and Leap year supported.
  - Alarm to wake chip up from Standby mode or from Power-down mode supported.
  - Wake chip up from Power-down mode by input pin supported.
  - Power-off chip by register setting supported.
  - Power-on timeout is supported for low battery protection.

- **GPIO**
  - 88 programmable general purpose I/Os supported and separated into 5 groups.
  - Individual configuration supported for each I/O signal.
  - Configurable interrupt control functions supported.
  - Configurable de-bounce circuit supported for interrupt function.

- **General-purpose ADC**
  - Multi-channel, 10-bit ADC supported
    - 2 channels dedicated for 4-wire resistive touch sensor inputs.
    - 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor.
    - Input voltage range from 0V ~ 3.3V supported.
  - Maximum 25MHz input clock supported.
  - Maximum 150K/s conversion rate supported.
  - LVR (Low Voltage Reset) supported.

- **Microphone ADC**
  - Built-in Programmable Gain Control (PGC) circuit
  - Built-in Bias circuit
  - 10-bit ADC supported

- **Keypad Interface (KPI)**
  - Matrix Key Pad Interface Supported.
  - Maximum 8x8 and minimum 3x3 keypad matrix supported.
  - Configurable key de-bounce supported.
  - Low power wakeup mode supported.
  - Configurable three-key reset supported.

- **AES (Advance Encryption Standard) Engine**
  - Support both encryption and decryption.
  - Support only CBC (Cipher Block Chaining) mode.
  - All three kinds of key length: 128, 192, 256 bits are supported.
  - Built-in DMA supported.

- **Power Management**
  - Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes.
    - Normal Operating Mode
      - Core power is 1.2V and chip is in normal operation.
    - CPU Standby Mode
      - Core power is 1.2V and only ARM CPU clock is turned OFF.
    - Deep Standby Mode
      - Core power is 1.2V and all IP clocks are turned OFF.
    - Power Down Mode
      - Only the RTC power is ON. Other 3.3V and 1.2V power are OFF.

- **Software Support**
  - Development Tools
    - Bootloader / Diagnostic Program / NAND Writer Program: ADS 1.2 or RVDS 2.x or 3.x
    - Linux Kernel (2.6.17.14) / System Manager: GCC 4.2
    - TurboWriter / Sync Tool: Microsoft VC 6.0
  - NAND Flash File System
    - FAT12, FAT16 and FAT32 with long filename are supported.
    - Hidden disk is supported.
    - RAM disk is supported.

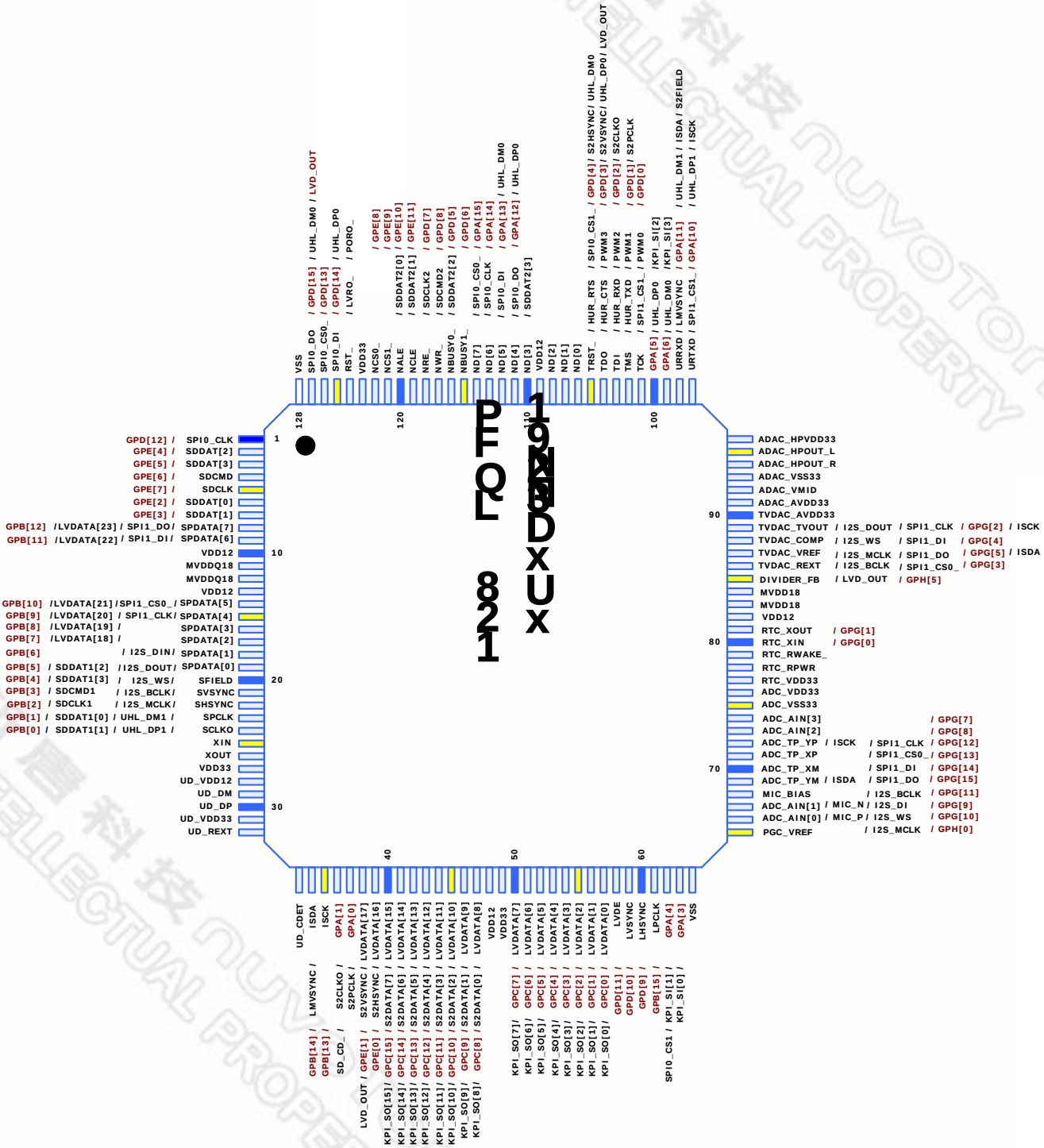
- S/W audio Library
  - Decoders with ADPCM / MP3 / ACC / OGG / WMA format support.
  - 32-polyphony Wavetable MIDI synthesizer.
  - Programmable sampling rate and target bit rate.
- USB Driver
  - MS (Mass Storage) Class
  - HID (Human Interface Device) Class
- Fast Booting Time (From power-on to application running)
  - Within 3 seconds

- **Operating Voltage**
  - I/O: 3.3V
  - Core: 1.2V for 300MHz.

- **Package**
  - LQFP-128 (MCP, stacked with 32Mbx16 DDR2 @ 1.8V)

3. PIN DIAGRAM

3.1 N3291xUxDN (LQFP-128)



4. PIN DESCRIPTION

4.1 Pin Description

PIN NAME	I/O TYPE	DESCRIPTION
Clock & Reset		
XIN	I	27MHz/12MHz Crystal Input
XOUT	O	27MHz/12MHz Crystal Output
RST_	IOSU	System Reset, Input, Low Active Watch-Dog Reset, Output, Low Active
JTAG Interface		
TCK	IOD	JTAG Interface Test Clock, Input
SPI1_CS1_		SPI Port 1 Device Select 1, Output, Low Active
PWM0		PWM Channel 0
GPD[0]		GPIO Port D Bit 0
TMS	IOU	JTAG Interface Test Mode Select, Input
HUR_TXD		High-Speed UART TX Data, Output
PWM1		PWM Channel 1
S2PCLK		CMOS Camera Module Port 2 PCLK Signal
GPD[1]		GPIO Port D Bit 1
TDI	IOU	JTAG Interface Test Data In, Input
HUR_RXD		High-Speed UART RX Data, Input
PWM2		PWM Channel 2
S2CLKO		CMOS Camera Module Port 2 MCLK Signal
GPD[2]		GPIO Port D Bit 2
TDO	IOU	JTAG Interface Test Data Out, Output
HUR_CTS		High-Speed UART Clear-To-Send, Input, Low Active
PWM3		PWM Channel 3

PIN NAME	I/O TYPE	DESCRIPTION
LVD_OUT		Low Voltage Dection Indicator
S2VSYNC		The 2nd CMOS Camera Module VSYNC Signal
UHL_DP0		USB 1.1 Host Like Port 0 D+ Signal
GPD[3]		GPIO Port D Bit 3
TRST_	IOU	JTAG Interface Test Reset, Input, Low Active
HUR_RTS		High-Speed UART Reset-To-Send, Output, Low Active
SPI0_CS1_		SPI Port 0 Device Select 1, Output, Low Active
UHL_DM0		USB 1.1 Host like Port 0 D- Signal
S2HSYNC		The 2nd CMOS Camera Module HSYNC Signal
GPD[4]		GPIO Port D Bit 4
NAND Interface		
NCS0_	IOU	NAND Interface Chip Select 0, Output, Low Active
GPE[8]		GPIO Port E Bit 8
NCS1_	IOU	NAND Interface Chip Select 1, Output, Low Active
GPE[9]		GPIO Port E Bit 9
NALE	IOU	NAND Interface Address-Latch-Enable, Output, High Active
SDDAT2[0]		SD Port 2 Data Bit 0
GPE[10]		GPIO Port E Bit 10
NCLE	IOU	NAND Interface Command-Latch-Enable, Output, High Active
SDDAT2[1]		SD Port 2 Data Bit 1
GPE[11]		GPIO Port E Bit 11
NBUSY0_	IOU	NAND Interface Busy 0, Input, Low Active
SDDAT2[2]		SD Port 2 Data Bit 2
GPD[5]		GPIO Port D Bit 5
NBUSY1_	IOU	NAND Interface Busy 1, Input, Low Active
GPD[6]		GPIO Port D Bit 6
NRE_	IOU	NAND Interface Read Enable, Output, Low Active
SDCLK2		SD Port 2 Clock, Output

PIN NAME	I/O TYPE	DESCRIPTION
GPD[7]		GPIO Port D Bit 7
NWR_	IOU	NAND Interface Write Enable, Output, Low Active
SDCMD2		SD Port 2 Command/Response
GPD[8]		GPIO Port D Bit 8
ND[7]	IOU	NAND Interface Data Bit 7
SPI0_CS0_		SPI Port 0 CS0, Active Low
GPA[15]		GPIO Port A Bit 15
ND[6]	IOU	NAND Interface Data Bit 6
SPI0_CLK		SPI Port 0 Serial Clock Signal
GPA[14]		GPIO Port A Bit 14
ND[5]	IOU	NAND Interface Data Bit 5
SPI0_DI		SPI Port 0 Serial Data Input
UHL_DM0		USB 1.1 Host Like Port 0 D- Signal
GPA[13]		GPIO Port A Bit 13
ND[4]	IOU	NAND Interface Data Bit 4
SPI0_DO		SPI Port 0 Serial Data Output
UHL_DP0		USB 1.1 Host Like Port 0 D+ Signal
GPA[12]		GPIO Port A Bit 12
ND[3]	IOU	NAND Interface Data Bit 3
SDDAT2[3]		SD Port 3 Data Bit 3
ND[2]	IOU	NAND Interface Data Bit 2
ND[1]	IOU	NAND Interface Data Bit 1
ND[0]	IOU	NAND Interface Data Bit 0
Sensor/Video-In Interface		
SCLKO	IOU	Clock to Sensor Module, Output
UHL_DP1		USB Host Like Interface, DP
SDDAT1[1]		SD Port 1 Data Bit 1
GPB[0]		GPIO Port B Bit 0

PIN NAME	I/O TYPE	DESCRIPTION
SPCLK	IOU	Sensor Interface Pixel Clock, Input
UHL_DM1		USB Host Like Interface, DM
SDDAT1[0]		SD Port 1 Data Bit 0
GPB[1]		GPIO Port B Bit 1
SHSYNC	IOU	Sensor Interface HSYNC, Input
I2S_MCLK		Clock to I2S Codec, Output
SDCLK1		SD Port 1 Clock, Output
GPB[2]		GPIO Port B Bit 2
SVSYNC	IOU	Sensor Interface VSYNC, Input
I2S_BCLK		I2S Interface Clock, Input
SDCMD1		SD Port 1 Command/Response
GPB[3]		GPIO Port B Bit 3
SFIELD	IOU	Sensor Interface Even/ODD Field Indicator, Input
I2S_WS		I2S Interface Word Select, Output
SDDAT1[3]		SD Port 1 Data Bit 3
GPB[4]		GPIO Port B Bit 4
SPDATA[0]	IOU	Sensor Interface Data Bit 0, Input
I2S_DOUT		I2S Interface Data Output
SDDAT1[2]		SD Port 1 Data Bit 2
GPB[5]		GPIO Port B Bit 5
SPDATA[1]	IOU	Sensor Interface Data Bit 1, Input
I2S_DIN		I2S Interface Data Input
GPB[6]		GPIO Port B Bit 6
SPDATA[2]	IOU	Sensor Interface Data Bit 2, Input
LVDATA[18]		LCD Interface Data Bit 18
GPB[7]		GPIO Port B Bit 7
SPDATA[3]	IOU	Sensor Interface Data Bit 3, Input
LVDATA[19]		LCD Interface Data Bit 19

PIN NAME	I/O TYPE	DESCRIPTION
GPB[8]		GPIO Port B Bit 8
SPDATA[4]	IOU	Sensor Interface Data Bit 4, Input
SPI1_CLK		SPI Port 1 Clock Output in Master Mode Input in Slave Mode
LVDATA[20]		LCD Interface Data Bit 20
GPB[9]		GPIO Port B Bit 9
SPDATA[5]	IOU	Sensor Interface Data Bit 5, Input
SPI1_CS0_		SPI Port 1 Select 0, Low Active Output in Master Mode Input in Slave Mode
LVDATA[21]		LCD Interface Data Bit 21
GPB[10]		GPIO Port B Bit 10
SPDATA[6]	IOU	Sensor Interface Data Bit 6, Input
SPI1_DI		SPI Port 1 Data Input
LVDATA[22]		LCD Interface Data Bit 22
GPB[11]		GPIO Port B Bit 11
SPDATA[7]	IOU	Sensor Interface Data Bit 7, Input
SPI1_DO		SPI Port 1 Data Output
LVDATA[23]		LCD Interface Data Bit 23
GPB[12]		GPIO Port B Bit 12
I2C Interface		
ISCK	IOU	I2C Interface Clock, Output
GPB[13]		GPIO Port B Bit 13
ISDA	IOU	I2C Interface Data
LMVSYNC		MPU Mode VSYNC, Output
GPB[14]		GPIO Port B Bit 14
LCD/Display Interface		

PIN NAME	I/O TYPE	DESCRIPTION
LPCLK	IOU	LCD Interface Pixel Clock, Output
GPB[15]		GPIO Port B Bit 15
LHSYNC	IOU	LCD Interface HSYNC, Output, High Active
GPD[9]		GPIO Port D Bit 9
LVSYNC	IOU	LCD Interface VSYNC, Output, High Active
GPD[10]		GPIO Port D Bit 10
LVDE	IOU	LCD Interface Data Enable, Output, High Active
GPD[11]		GPIO Port D Bit 11
LVDATA[0]	IOU	LCD Interface Data Bit 0
KPI_SO[0]		KPI Scan Out Bit 0
GPC[0]		GPIO Port C Bit 0
LVDATA[1]	IOU	LCD Interface Data Bit 1
KPI_SO[1]		KPI Scan Out Bit 1
GPC[1]		GPIO Port C Bit 1
LVDATA[2]	IOU	LCD Interface Data Bit 2
KPI_SO[2]		KPI Scan Out Bit 2
GPC[2]		GPIO Port C Bit 2
LVDATA[3]	IOU	LCD Interface Data Bit 3
KPI_SO[3]		KPI Scan Out Bit 3
GPC[3]		GPIO Port C Bit 3
LVDATA[4]	IOU	LCD Interface Data Bit 4
KPI_SO[4]		KPI Scan Out Bit 4
GPC[4]		GPIO Port C Bit 4
LVDATA[5]	IOU	LCD Interface Data Bit 5
KPI_SO[5]		KPI Scan Out Bit 5
GPC[5]		GPIO Port C Bit 5
LVDATA[6]	IOU	LCD Interface Data Bit 6
KPI_SO[6]		KPI Scan Out Bit 6

PIN NAME	I/O TYPE	DESCRIPTION
GPC[6]		GPIO Port C Bit 6
LVDATA[7]	IOU	LCD Interface Data Bit 7
KPI_SO[7]		KPI Scan Out Bit 7
GPC[7]		GPIO Port C Bit 7
LVDATA[8]	IOU	LCD Interface Data Bit 8
KPI_SO[8]		KPI Scan Out Bit 8
SPDATA[0]		Sensor Interface Data Bit 0, Input
GPC[8]		GPIO Port C Bit 8
LVDATA[9]	IOU	LCD Interface Data Bit 9
KPI_SO[9]		KPI Scan Out Bit 9
SPDATA[1]		Sensor Interface Data Bit 1, Input
GPC[9]		GPIO Port C Bit 9
LVDATA[10]	IOU	LCD Interface Data Bit 10
KPI_SO[10]		KPI Scan Out Bit 10
SPDATA[2]		Sensor Interface Data Bit 2, Input
GPC[10]		GPIO Port C Bit 10
LVDATA[11]	IOU	LCD Interface Data Bit 11
KPI_SO[11]		KPI Scan Out Bit 11
SPDATA[3]		Sensor Interface Data Bit 3, Input
GPC[11]		GPIO Port C Bit 11
LVDATA[12]	IOU	LCD Interface Data Bit 12
KPI_SO[12]		KPI Scan Out Bit 12
SPDATA[4]		Sensor Interface Data Bit 4, Input
GPC[12]		GPIO Port C Bit 12
LVDATA[13]	IOU	LCD Interface Data Bit 13
KPI_SO[13]		KPI Scan Out Bit 13
SPDATA[5]		Sensor Interface Data Bit 5, Input
GPC[13]		GPIO Port C Bit 13

PIN NAME	I/O TYPE	DESCRIPTION
LVDATA[14]	IOU	LCD Interface Data Bit 14
KPI_SO[14]		KPI Scan Out Bit 14
SPDATA[6]		Sensor Interface Data Bit 6, Input
GPC[14]		GPIO Port C Bit 14
LVDATA[15]	IOU	LCD Interface Data Bit 15
KPI_SO[15]		KPI Scan Out Bit 15
SPDATA[7]		Sensor Interface Data Bit 7, Input
GPC[15]		GPIO Port C Bit 15
LVDATA[16]	IOU	LCD Interface Data Bit 16
SHSYNC		Sensor Interface HSYNC, Input
GPE[0]		GPIO Port E Bit 0
LVDATA[17]	IOU	LCD Interface Data Bit 17
SVSYNC		Sensor Interface VSYNC, Input
LVD_OUT		Low Voltage Detect Output
GPE[1]		GPIO Port E Bit 1
UART Interface		
URTXD	IOU	UART TX Data, Output
SPI1_CS1_		SPI Port 1 Device Select 1, Output, Low Active
UHL_DP1		USB 1.1 Host Lite Port 1, D+
ISCK		I2C Serial Clock
GPA[10]		GPIO Port A Bit 10
URRXD	IOU	UART RX Data, Input
LMVSYNC		MPU Mode VSYNC, Output
S2FIELD		CMOS Image Sensor Field Indicator
UHL_DM1		USB 1.1 Host Lite Port 1, D-
ISDA		I2C Serial Data
GPA[11]		GPIO Port A Bit 11
SPI 0 Interface		

PIN NAME	I/O TYPE	DESCRIPTION
SPI0_CLK	IOU	SPI Port 0 Clock Output in Master Mode Input in Slave Mode
GPD[12]		GPIO Port D Bit 12
SPI0_CS0_	IOU	SPI Port 0 Device Select 0, Low Active Output in Master Mode Input in Slave Mode
GPD[13]		GPIO Port D Bit 13
SPI0_DI	IOU	SPI Port 0 Data Input
UHL_DP0		USB 1.1 Host Lite Port 0, D+
GPD[14]		GPIO Port D Bit 14
SPI0_DO	IOU	SPI Port 0 Data Output
UHL_DM0		USB 1.1 Host Lite Port 0, D-
LVD_OUT		Low Voltage Detect Output
GPD[15]		GPIO Port D Bit 15
SD Card Interface		
SDCLK	IOU	SD Port 0 Clock, Output
GPE[7]		GPIO Port E Bit 7
SDCMD	IOU	SD Port 0 Command/Response
GPE[6]		GPIO Port E Bit 6
SDDAT[0]	IOU	SD Port 0 Data Bit 0
GPE[2]		GPIO Port E Bit 2
SDDAT[1]	IOU	SD Port 0 Data Bit 1
GPE[3]		GPIO Port E Bit 3
SDDAT[2]	IOU	SD Port 0 Data Bit 2
GPE[4]		GPIO Port E Bit 4
SDDAT[3]	IOU	SD Port 0 Data Bit 3
GPE[5]		GPIO Port E Bit 5

PIN NAME	I/O TYPE	DESCRIPTION
GPIO A		
GPA[0]	IOU	GPIO Port A Bit 0
S2PCLK		CMOS Image Sensor PCLK
GPA[1]	IOU	GPIO Port A Bit 1
S2CLKO		CMOS Image Sensor MCLK
SD_CD_		SD Card Detect, Input, Low Active
GPA[3]	IOU	GPIO Port A Bit 3
KPI_SI[0]		KPI Scan In Bit 0
GPA[4]	IOU	GPIO Port A Bit 4
SPI0_CS1_		SPI Port 0 Chip Select 1
KPI_SI[1]		KPI Scan Out Bit 2
GPA[5]	IOU	GPIO Port A Bit 5
UHL_DP0		USB Host 1.1 Lite Port 0, D+
KPI_SI[2]		KPI Scan In Bit 2
GPA[6]	IOU	GPIO Port A Bit 6
UHL_DM0		USB Host 1.1 Lite Port 0, D-
KPI_SI[3]		KPI Scan In Bit 3
RTC (Real Time Clock)		
RTC_XIN (32768Hz)	I	32768Hz Crystal Input
RTC_XOUT (32768Hz)	O	32768Hz Crystal Output
RTC_RWAKE_	I	Wakeup Enable, Input, Low Active
RTC_RPWR	OD	Power Enable, Open-Drain
USB 2.0 Device Interface		
UD_CDET	I	USB Device Connect Detect, Input, High Active
UD_DP	IO	USB 2.0 Device D+
UD_DM	IO	USB 2.0 Device D-
UD_REXT	IO	External Resistor Connect Recommend to connect 12.1KΩ resistor to ground for USB 2.0 PHY

PIN NAME	I/O TYPE	DESCRIPTION
TV Out		
TVDAC_TVOUT	O	Composite/Chroma Output Connect an external 75Ω resistor to ground of TVDAC as TV terminal impedence
SPI1_CLK	O	SPI Port 1 Serial Clock
I2S_DOUT	O	I2S Serial Data Output
ISCK	IO	I2C Serial Clock
GPG[2]	IO	GPIO Port G bit 2
TVDAC_REXT	IO	External Resistor Connection Recommend to connect 160Ω resistor to ground of TVDAC
SPI1_CS0_	O	SPI Port 1 Chip Select
I2S_BCLK	I	I2S Bit Clock
GPG[3]	IO	GPIO Port G bit 3
TVDAC_COMP	O	External Capacitor Connection Connect 0.1uF capacitor to VDD33 of TVDAC
SPI1_DI	I	SPI Port 1 Serial Data Input
I2S_WS	O	I2S Interface Word Select, Output
GPG[4]	IO	GPIO Port G bit 4
TVDAC_VREF	O	Reference Voltage Output Connect 0.1uF capacitor to ground of TVDAC
SPI1_DO	O	SPI Port 1 Serial Data Output
I2S_MCLK	O	I2S Master Clock
ISDA	IO	I2C Serial Data
GPG[5]	IO	GPIO Port G bit 5
ADC & Touch Panel		
MIC_BIAS	I	MIC ADC Bias Voltage
I2S_BCLK	I	I2S Bit Clock
GPG[11]	I	GPIO Port G bit 11

PIN NAME	I/O TYPE	DESCRIPTION
PGC_VREF	I	PGC Voltage Reference
I2S_MCLK	O	I2S Master Clock
GPH[0]	IO	GPIO Port H bit 0
ADC_AIN[3]	I	ADC Analog Input Channel 3
ADC_AIN[2]	I	ADC Analog Input Channel 2
ADC_AIN[1]	I	ADC Analog Input Channel 1
MIC_N	I	Microphone Negative Input
I2S_DI	I	I2S Serial Data Input
GPG[9]	I	GPIO Port G bit 9
ADC_AIN[0]	I	ADC Analog Input Channel 0
MIC_P	I	Microphone Positive Input
I2S_WS	O	I2S Interface Word Select, Output
GPG[10]	IO	GPIO Port G bit 10
ADC_TP_YP	I	Touch Panel YP
SPI1_CLK	O	SPI Port 1 Serial Clock
ISCK	IO	I2C Serial Clock
GPG[12]	IO	GPIO Port G bit 12
ADC_TP_XP	I	Touch Panel XP
SPI1_CS0_	O	SPI Port 1 Chip Select
GPG[13]	IO	GPIO Port G bit 13
ADC_TP_XM	I	Touch Panel XM
SPI1_DI	I	SPI Port 1 Serial Data Input
GPG[14]	IO	GPIO Port G bit 14
ADC_TP_YM	I	Touch Panel YM
SPI1_DO	O	SPI Port 1 Serial Data Output
ISDA	IO	I2C Serial Data
GPG[15]	IO	GPIO Port G bit 15
Audio DAC		

PIN NAME	I/O TYPE	DESCRIPTION
ADAC_HPOUT_R	O	Audio Headphone Right Channel Output
ADAC_HPOUT_L	O	Audio Headphone Left Channel Output
ADAC_VREF	O	Audio DAC Reference Voltage Output Recommend to connect 1uF capacitor to ground of Audio DAC
Power/Ground		
MVDD18	P	SDRAM I/F Power (1.8V)
MVDDQ18	P	SDRAM I/F Power (1.8V)
RTC_VDD33	P	RTC Core, I/F & 32768Hz Crystal Power
UD_VDD33	P	USB 2.0 PHY Power (3.3V)
UD_VDD12	P	USB 2.0 PHY Power (1.8V)
TVDAC_VDD33	P	TV DAC Power (3.3V)
ADC_VDD33	P	ADC Power (3.3V)
ADC_VSS33	G	ADC Ground (0V)
ADAC_HPVDD33	P	Audio DAC Headphone Driver Power (3.3V)
ADAC_HPVSS33	G	Audio DAC Headphone Driver Ground (0V)
ADAC_AVDD33	P	Audio DAC Power (3.3V)
ADAC_VSS33	G	Audio DAC Ground (0V)
VDD33	P	I/O Power (3.3V)
VDD18	P	Core Logic Power (1.8V)
VSS	G	Ground (0V)

4.2 Pin Type Description

TYPE	DESCRIPTION
I	Input
O	Output
OD	Open Drain output
IO	Input / Output
IOD	Input with pull-Down / Output
IOU	Input with pull-Up / Output
IOSU	Input with Schmitt trigger & pull-Up/ Output
P	Power
G	Ground

5. ELECTRICAL SPECIFICATION

5.1 Absolute Maximum Rating

PARAMETERS	VALUES
Ambient Temperature	-20 °C ~ 85 °C
Storage Temperature	-40 °C ~ 125 °C
Voltage On Any Pin	-0.3V ~ 3.6V
Power Supply Voltage (Core Logic)	-0.5V ~ 1.8V
Power Supply Voltage (I/O Buffer)	-0.5V ~ 4.6V
Injection Current (Latch-Up Testing)	100mA
Crystal Frequency	2MHz ~ 27MHz

5.2 DC Characteristics (Normal I/O)

SYMBOL	PARAMETER		CONDITION	MIN.	TYP.	MAX.	UNIT
VDD33	I/O Buffer Post-Driver Voltage			3.0	3.3	3.6	V
VDD12	Core Logic and I/O Buffer Pre-Driver Voltage	300MHz		1.08	1.2	1.32	V
MVDD18	DRAM Power Voltage			1.7	1.8	1.9	V
RTC_VDD	RTC Power Supply			2.0	-	3.6	V
I_{RTC_VDD}	RTC Supply Current			-	4	-	uA
V_{IH}	Input High Voltage			2.0	-	VDD33+0.3	V
V_{IL}	Input Low Voltage			-0.3	-	0.8	V
V_{T+}	Schmitt Trigger Low to High Threshold Point			1.5	1.7	1.9	V
V_{T-}	Schmitt Trigger High to Low Threshold Point			0.9	1.1	1.2	V

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{CC}	Core Power Supply Current	F_{CPU} = 300MHz, MCLK = 150MHz, VDD12 = 1.2V	-			
				TBD	-	mA
I_L	Input Leakage Current			-	20	mA
I_{OZ}	Tri-State Output Leakage Current			TBD		uA
R_{PU}	Pull-Up Resistor		61	76	112	kΩ
R_{PD}	Pull-Down Resistor		57	80	156	kΩ
V_{OL}	Output Low Voltage		-	-	0.4	V
V_{OH}	Output High Voltage		2.4	-	-	V
I_{OL}	Low Level Output Current	4W I/O, V_{OL} = 0.4V	4.2	6.5	8	mA
		8W I/O, V_{OL} = 0.4V	8.4	13.0	16.0	mA
I_{OH}	High Level Output Current	4W I/O, V_{OH} = 2.4V	4.7	9.6	14.9	mA
		8W I/O, V_{OH} = 2.4V	9.4	19.2	29.8	mA

5.3 Audio DAC Characteristics

Conditions: AVDD:3.3V, VDD:1.2V, T_A:25℃, Fsignal:1KHz, Fsampling:48KHz, MCLK:256xFsampling

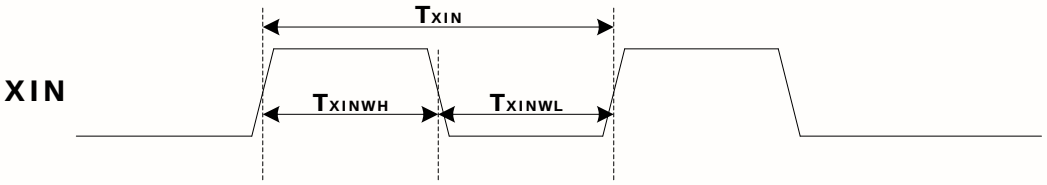
PARAMETER	MIN	TYP	MAX	UNIT
Operating Voltage AVDD	3.0	3.3	3.6	V
Operating Voltage VDD	1.08	1.2	1.34	V
Reference Voltage	-	AVDD/2	-	V
Line Output				
Resolution	-	16	-	Bit
L-Channel Total Harmonic Distortion (THD)	-	-90	-76	dB
R-Channel Total Harmonic Distortion (THD)	-	-90	-76	dB
Dynamic Range (-60dB input, A-weighted)	90	101.6	-	dB
SNR (A-weighted)	90	101.6	-	dB
Channel Separation	-	100	-	dB
Channel Matching	-	0.2	-	dB
Full Scale output voltage	-	AVDD(3.3)	-	Vrms
Load Resistor	10	-	-	Kohm
Load Capacitor	-	-	50	pF
Analog Mute	-	100	-	dB
Headphone Output				
Maximum Output Power (Po) @ 32ohm load	-	-	31	mW
Maximum Output Power (Po) @ 16ohm load	-	-	62	mW
L-Channel SNR (A-weighted)	90	96	-	dB
R-Channel SNR (A-weighted)	90	96	-	dB
L-Channel THD @ 32ohm load, Po=10mW	-	-76	-70	dB
R-Channel THD @ 32ohm load, Po=10mW	-	-76	-70	dB
Power Supply Current in Normal Mode (including PLL, no loading)				
AVDD(3.3V)	-	8.7	-	mW
VDD (1.2V)	-	0.7	-	mW

5.4 ADC Characteristics

PARAMETER	MIN.	TYP.	MAX.	UNIT
SAR ADC Input Voltage Range	3.0	-	3.6	V
Resolution of ADC	-	-	10	bit
Signal-to-Noise Plus Distortion of ADC from Line In	-	-60	-	dB
Integral Non-Linearity of ADC	-	±2.0	-	LSB
Differential Non-Linearity of ADC	-	±0.8	-	LSB
No Missing Code	-	10	-	bit
AD Conversion Rate=ADCCLK/16	-	-	150	KHz

5.5 AC Characteristics (Digital Interface)

5.5.1 Clock Input Characteristics

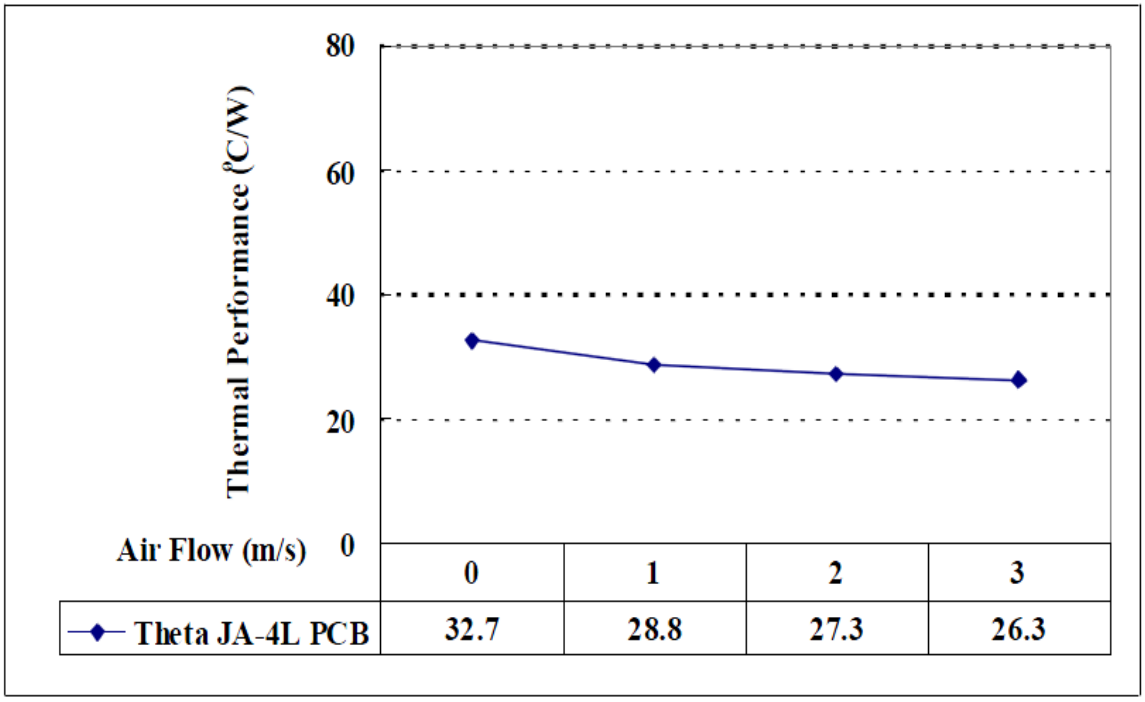


$F_{XIN} = 1 / T_{XIN}$

$XIN_{DUTY} = T_{XINWH} / (T_{XINWH} + T_{XINWL})$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
F_{XIN}	Clock Input Frequency	-	12 / 27	-	MHz
XIN_{DUTY}	Clock Input Duty Cycle	45	50	55	%

5.6 Thermal characteristics of SLQFP-128 Package

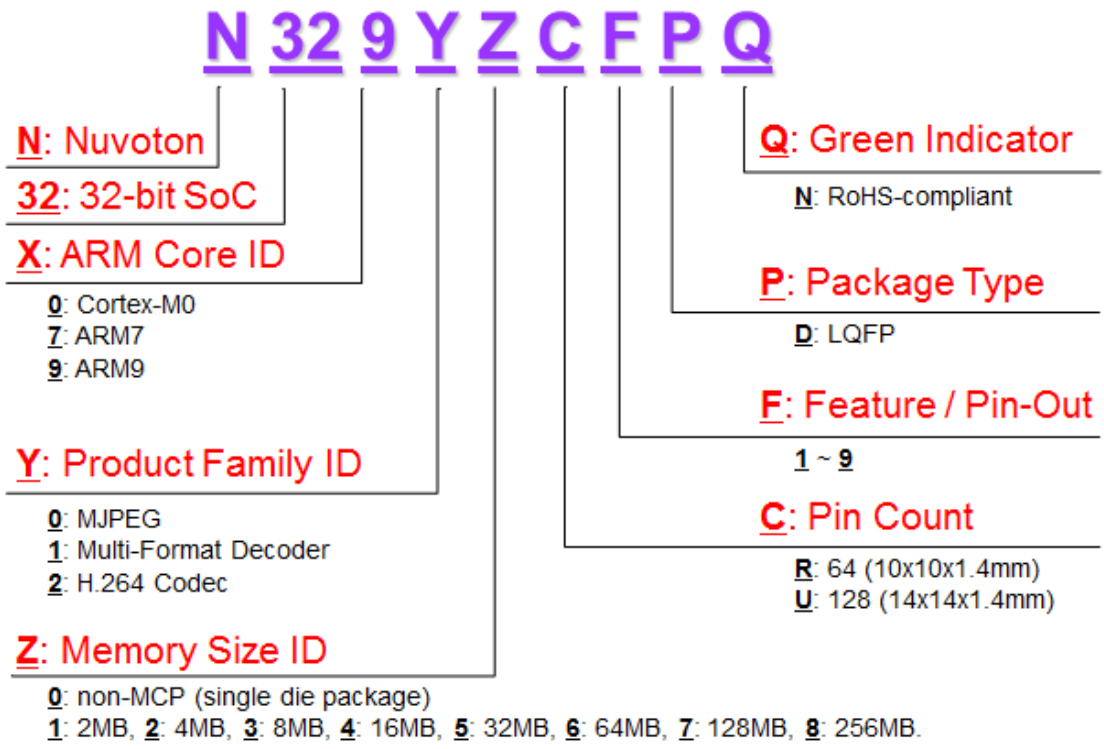


Thermal Performance of SLQFP under Forced Convection

6. ORDERING INFORMATION

PART NO.	PACKAGE TYPE	DESCRIPTION
N32916U1DN	LQFP-128, MCP	Cost-effective package with 32Mbx16 DDR2 inside, without OVG accelerator.
N32916U2DN	LQFP-128, MCP	Cost-effective package with 32Mbx16 DDR2 inside and OVG accelerator.
N32915U3DN	LQFP-128, MCP	Cost-effective package with 16Mbx16 DDR2 inside, without OVG accelerator.
N32915U4DN	LQFP-128, MCP	Cost-effective package with 16Mbx16 DDR2 inside and OVG accelerator.

6.1 Part Number Definition

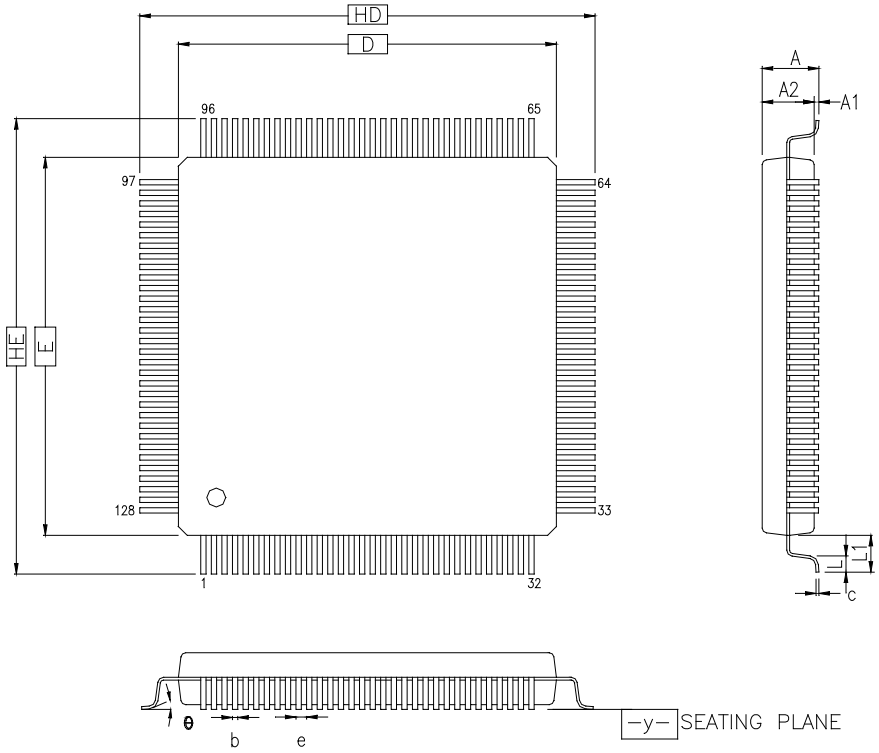


6.2 Difference between N3291xU1(3)DN and N3291xU2(4)DN

	N3291xU1DN/N3291xU3DN	N3291xU2DN/N3291xU4DN
OpenVG(OVG) Accelerator	-	V

7. PACKAGE OUTLINE

7.1 128L LQFP (14X14X1.4mm body, 0.4mm pitch)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
HD		16.00 BSC.	
D		14.00 BSC.	
HE		16.00 BSC.	
E		14.00 BSC.	
b	0.13	0.16	0.23
e		0.40 BSC.	
θ	0°	3.5°	7°
c	0.09	—	0.20
L	0.45	0.60	0.75
L1		1.00 REF	
y	–	–	0.1

8. REVISION HISTORY

Version	Date	Description
A0	Aug. 1, 2012	● Initial release.
A1	Oct. 1, 2012	● Change Operation Temperature Range ● Add N32916U2DN ordering information.
A2	Oct. 25, 2012	● Add Part Number Definition
A3	Jun. 1, 2013	● Add N32915UxDN Parts Information ● Add MVDD18 Votage Range

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.