Non-Isolated Buck APFC Offline LED Power Switch

FEATURES

- Active PFC for High PF and Low THD
- PF>0.9 with Universal Input
- Built-in HV Startup and IC Power Supply Circuit
- Internal 500V Power MOSFET
- Quasi-Resonant for High Efficiency
- ±1% CC Regulation
- Very Low VDD Operation Current
- Excellent Line and Load Regulation
- LED Open/Short Protection
- Build in Protections:
  - Output Over Voltage Protection (OVP)
  - Cycle-by-Cycle Current Limiting (OCP)
  - Leading Edge Blanking (LEB)
  - LED Open/Short Protection
  - On-Chip Thermal Foldback (OTP)
- Available in SOP-7 Package

APPLICATIONS

- LED Bulb Light/Ceiling Light
- LED T5/T8 Tube

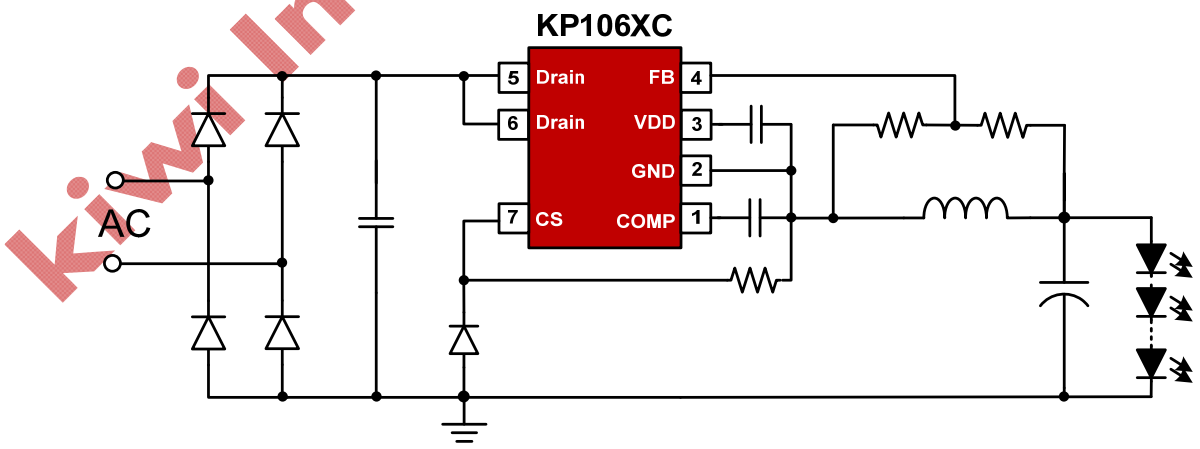
GENERAL DESCRIPTION

KP106XC series are a highly integrated power switch with constant current (CC) control for LED lighting applications. The IC utilizes Quasi-Resonant (QR) Buck topology with active PFC control for high PF, low THD, and high efficiency.

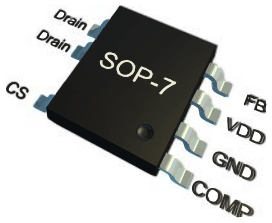
KP106XC integrates 500V power MOSFET with high voltage startup and IC power supply circuit, which requires very few external components. The IC senses the inductor current during the whole switching cycle, which can achieve high precision CC control with excellent line and load regulation.

KP106XC integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Thermal Foldack (OTP), Output Over Voltage Protection (OVP), LED Open/Short Protection, etc.

TYPICAL APPLICATION CIRCUIT



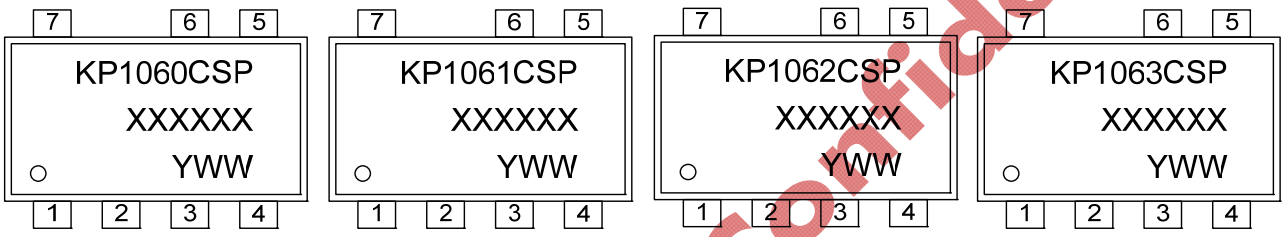
Pin Configuration



SOP-7

Marking Information

XXXXXX: Wafer Lot Code
Y: Year, G for 2017
WW: Working Week, 01-52



SOP-7

Output Power Table

Part Number	Package	Maximum Output Current (90-265Vac)	
		36V output	72V output
KP1060CSPA	SOP-7	200 mA	130 mA
KP1061CSPA	SOP-7	250 mA	200 mA
KP1062CSPA	SOP-7	350 mA	260 mA
KP1063CSPA	SOP-7	420 mA	300 mA

Note: The system actual maximum output power is determined by the test.

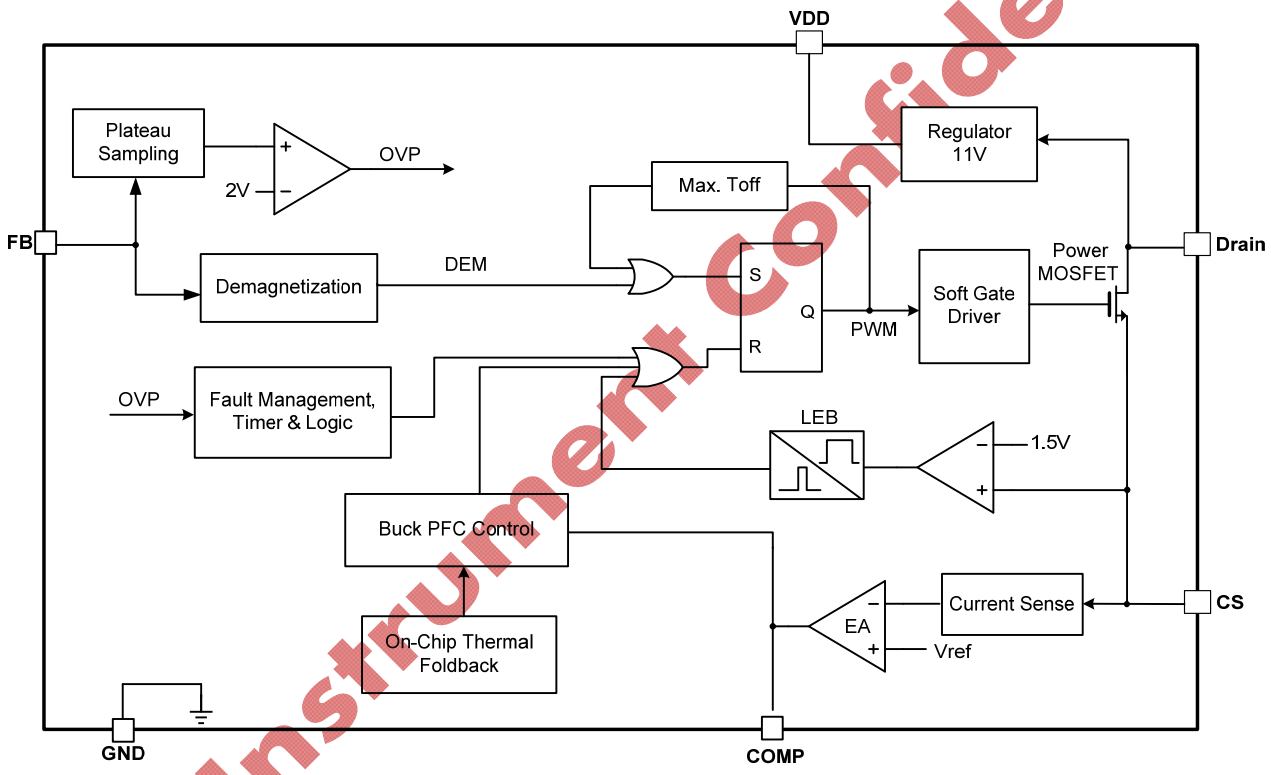
Pin Description

Pin Number	Pin Name	I/O	Description
1	COMP	I	Loop Compensation Pin. Connect a 1-4.7uF Ceramic Capacitor to GND Pin for CC regulation
2	GND	P	IC Ground Pin
3	VDD	P	IC Power Supply Pin. Connect a >2.2uF Ceramic Capacitor to GND Pin
4	FB	I	This pin detects the inductor demagnetization signal and the output voltage
5,6	Drain	P	Internal Power MOSFET Drain Pin
7	CS	I	Current Sense Input Pin

Ordering Information

Part Number	Description
KP1060CSPA	SOP-7, Pb free in T&R, 4000Pcs/Reel
KP1061CSPA	SOP-7, Pb free in T&R, 4000Pcs/Reel
KP1062CSPA	SOP-7, Pb free in T&R, 4000Pcs/Reel
KP1063CSPA	SOP-7, Pb free in T&R, 4000Pcs/Reel

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
Drain Pin Voltage Range	-0.3 to 500	V
VDD DC Supply Voltage	14	V
VDD DC Clamp Current	10	mA
CS, FB, COMP Voltage Range	-0.3 to 7	V
Package Thermal Resistance---Junction to Ambient (SOP-7)	165	°C/W
Maximum Junction Temperature	150	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Operating Ambient Temperature	-40 to 125	°C

Electrical Characteristics (Ta = 25°C, VDD=11V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin	VDD<V_{DD_Op}		300	700	uA
I_{VDD_Op}	Operation Current	Fsw=7KHz	80	150	300	uA
V_{DD_Op}	VDD Operation Voltage		10	11.5	13	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		7	8	9	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	I(V_{DD}) = 5 mA		14		V
Feedback Section (FB Pin)						
V_{FB_DEM}	Demagnetization Comparator Threshold	(Note 3)		0.2		V
V_{FB_OVP}	Over Voltage Protection (OVP) Threshold		1.9	2	2.1	V
T_{off_min}	Minimum OFF time	(Note 3)		2		us

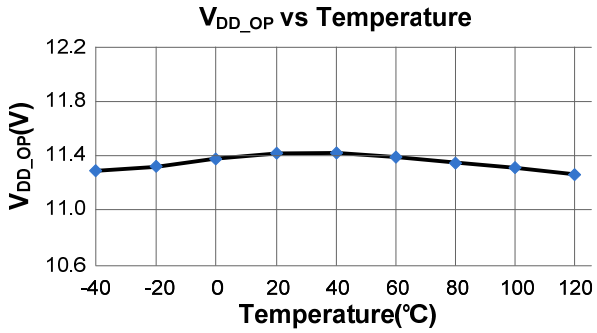
T_{on_max}	Maximum ON time	(Note 3)		40		us
T_{off_max}	Maximum OFF time		195	270	350	us
F_{max}	Max. Switching Frequency			100		KHz
Current Sense Input Section (CS Pin)						
T_{LEB}	OCP Leading Edge Blanking Time			300		ns
$V_{cs(max)}$	Current limiting threshold		1.4	1.5	1.6	V
T_{D_OC}	Over Current Detection and Control Delay			100		ns
V_{CC_REF}	Internal Reference for CC Loop Regulation		194	200	206	mV
CC Loop Compensation Section (COMP Pin)						
V_{comp_H}	COMP High Clamp Voltage			3		V
V_{comp_L}	COMP Low Clamp Voltage			0.7		V
Over Temperature Protection						
T_{SD}	Thermal Foldback Trigger Point	(Note 3)		150		°C
HV Startup and IC Supply Section (Drain Pin)						
I_{HV}	HV Charging Current	Drain =20V		10		mA
I_{HV_leak}	Leakage Current of HV Charging Circuit		10	40	60	uA
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		500			V
R_{dson}	Static Drain-Source On Resistance	KP1060C		8.5		Ω
		KP1061C		5.3		Ω
		KP1062C		2.5		Ω
		KP1063C		1.9		Ω

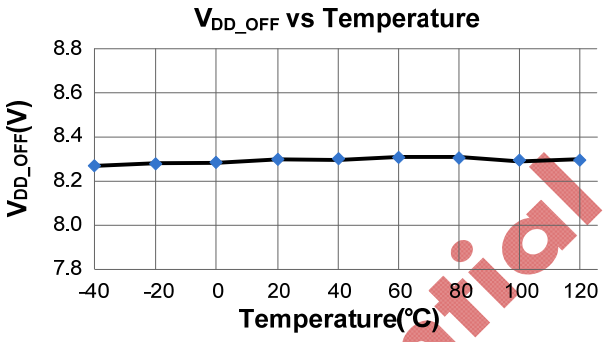
Note 1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

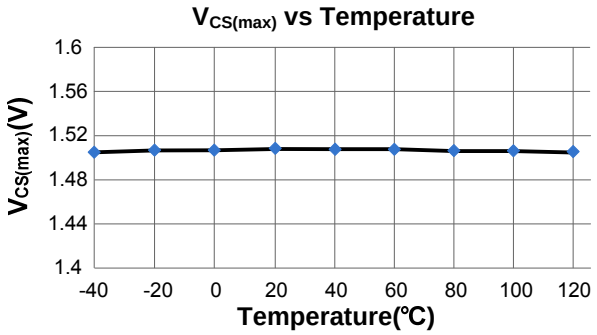
Note 2. The device is not guaranteed to function outside its operating conditions.

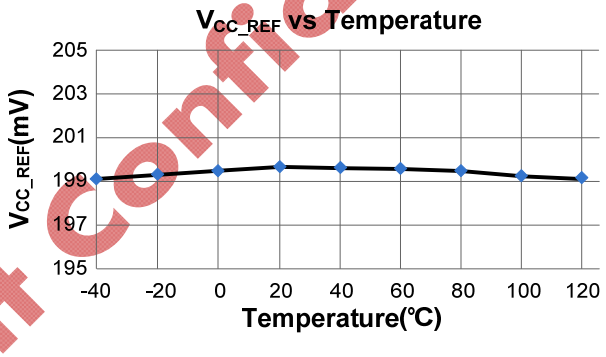
Note 3. Guaranteed by the Design.

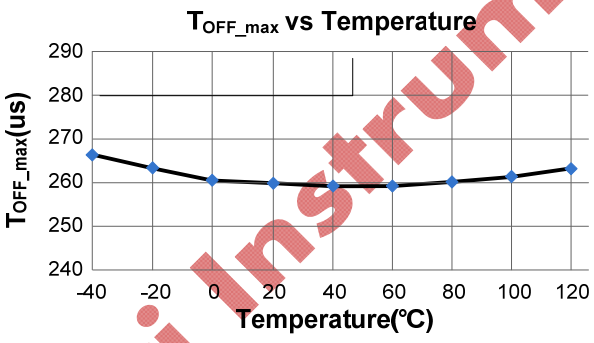
Characterization Plots











Operation Description

KP106XC series are a highly integrated power switch with constant current (CC) control for LED lighting applications. The IC utilizes Quasi-Resonant (QR) Buck topology with active PFC control for high PF, low THD, and high efficiency.

11V Regulator

In KP106XC, the 11V regulator charges VDD hold-up capacitor to 11V by drawing a current from the voltage on the Drain pin, whenever the internal power MOSFET is off. When the power MOSFET is on, the charging device runs off of the energy stored in the VDD hold-up capacitor. Extremely low IC power consumption allows KP106XC to operate continuously from the current drawn from the Drain pin. A capacitor value about 2.2uF is sufficient for both high frequency decoupling and energy storage.

System Start-Up Operation

After system power up, VDD hold up capacitor is charged by the internal HV startup circuit through Drain pin. When VDD pin voltage reaches the turn on threshold, the IC begins working. The COMP pin is pulled up to 0.7V quickly, then the IC begins to work at low switching frequency (typical 3.5KHz), the COMP pin voltage rises up gradually, thus the inductor peak current also rises up. The LED current hence achieves a soft start without over shoot.

Constant Current (CC) Control

KP106XC adopts floating ground structure. The inductor current is sensed during the whole switching cycle. The IC can accurately control the output current by the internal current feedback control loop. The output mean current in constant current (CC) mode can be expressed as:

$$I_{CC\_OUT}(mA) = \frac{V_{CC\_REF}}{R_{CS}} = \frac{200mV}{Rcs(\Omega)}$$

In the equation above,

Rcs--- the sensing resistor connected between CS and GND.

Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (300ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

Demagnetization Detection

KP106XC senses the output current zero crossing information through the external resistor feedback network. If FB pin voltage drops below 0.2V, an internal DEM comparator is triggered and a new switching cycle is initiated following the DEM triggering. The power MOSFET is always turned on with zero inductor current such that the turn-on loss and noise can be minimized.

Minimum and Maximum OFF Time

In KP106XC, a minimum OFF time (typically 2us) is implemented to suppress ringing when the power MOSFET is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance. The maximum OFF time in KP106XC is typically 270us.

Output Over Voltage Protection (OVP)

In KP106XC, the output OVP is integrated by plateau sampling the auxiliary winding in the PWM OFF state. If the sampled plateau voltage exceeds the OVP threshold (2V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 3 cycles, the controller assumes a true OVP and it stops all switching operations, as shown in Fig.1. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP threshold less than 3 successive cycles, the internal counter will be cleared and no fault is asserted. Output OVP is auto-recovery mode protection.

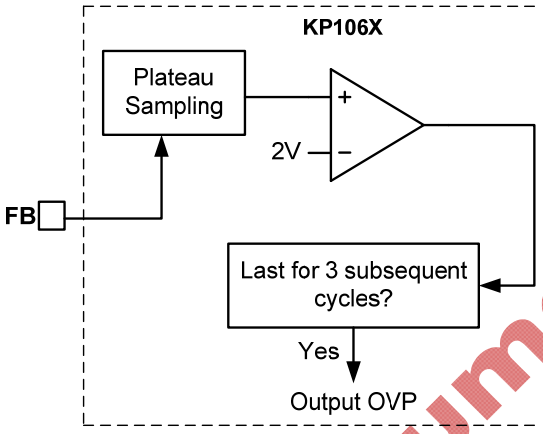


Fig.1

Auto-Restart Protection

In the event of LED open loop condition/output OVP protection, the IC enters into auto-restart and VDD oscillation mode begins, wherein the power MOSFET is disabled. In VDD oscillation mode, the VDD hold-up capacitor voltage will periodically ramp up and down between 11.5V and 8.3V with a digital counter counting the oscillation cycle. When 8 cycles had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system will resume normal operation.

On Chip Thermal Foldback (OTP)

KP106XC integrates thermal foldback function. When the IC temperature is over 150 °C, the system output regulation current is gradually reduced, as shown in Fig.2. Thus, the output power and thermal dissipation are also reduced. In this way, the system temperature is limited and system reliability is also improved.

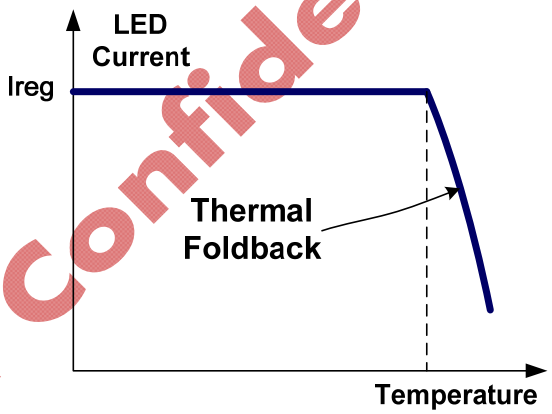


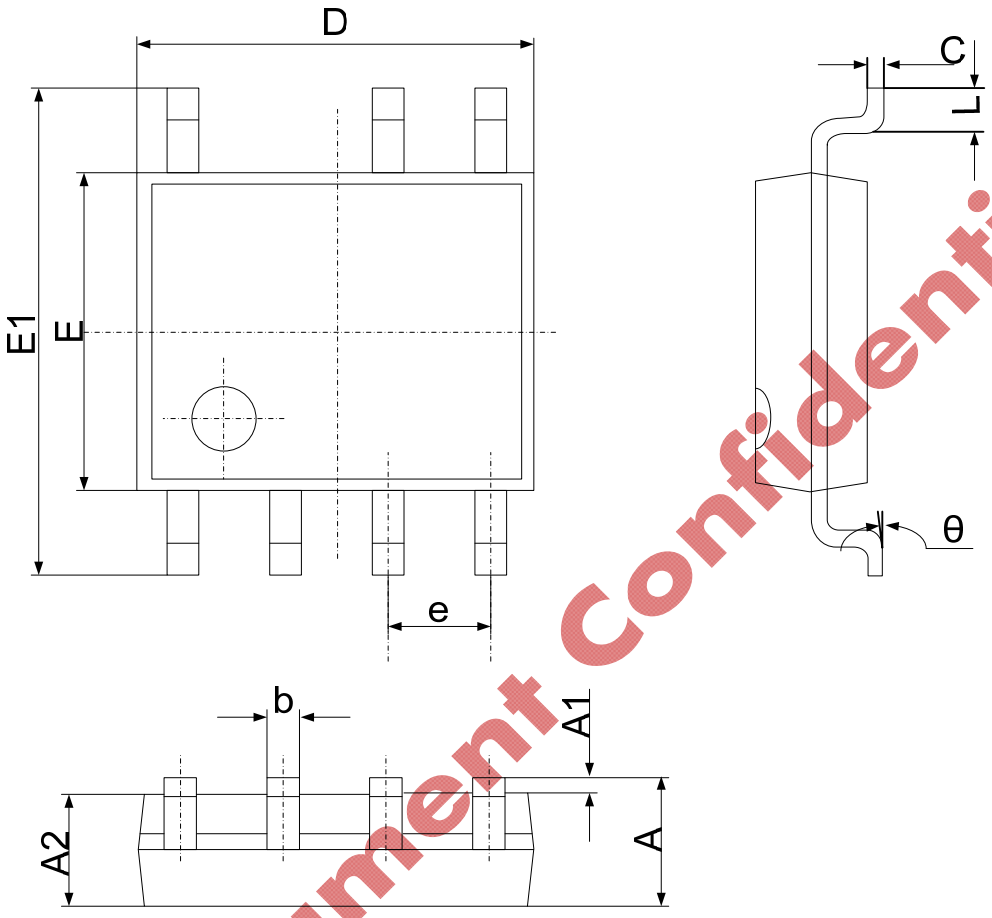
Fig.2

Soft Totem-Pole Gate Driver

KP106XC has a soft totem-pole gate driver with optimized EMI performance.

Package Dimension

SOP-7



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

DATE	REV.	DESCRIPTION
2016/05/10	1.0	First Release
2016/06/24	1.01	1, Update Characterization Plots, VDD_ON: VDD_OP 2,Update address of HangZhou
2016/08/16	1.1	Update the EC Table
2016/10/13	1.11	The recommended value of the VDD capacitor is updated to 2.2 uF
2016/12/16	1.2	Part Number KP1060CSPA is added
2017/02/13	1.3	Update Ordering Information
2017/04/05	1.4	Update the Output power table
2017/08/04	1.5	Update EC table

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