Surface Mount Ceramic Capacitor Products

Ceramic Chip Capacitors

Table of Contents

U Dielectric

X8R/X8L Dielectric

X7R Dielectric

X7S Dielectric

X5R Dielectric

Y5V Dielectric

MLCC Gold Termination (AU Series)

MLCC Tin/Lead Termination (LD Series)

How to Order

Part Number Explanation

Commercial Surface Mount Chips

EXAMPLE: 08055A101JAT2A

* B, C & D tolerance for ≤10 pF values.

Standard Tape and Reel material (Paper/Embossed) depends upon chip size and thickness. See individual part tables for tape material type for each capacitance value.

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers. For Tin/Lead Terminations, please refer to LD Series

High Voltage MLC Chips EXAMPLE: 1808AA271KA11A

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers. For Tin/Lead Terminations, please refer to LD Series

For RoHS compliant products, please select correct termination style.

Part Number Explanation

Capacitor Array

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

Low Inductance Capacitors (LICC) EXAMPLE: 0612ZD105MAT2A

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

Interdigitated Capacitors (IDC) EXAMPLE: W3L16D225MAT3A

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

Low Inductance Decoupling Capacitor Arrays (LICA) EXAMPLE: LICA3T183M3FC4AA

C0G (NP0) Dielectric

RoHS COMPLIANT

General Specifications

C0G (NP0) is the most popular formulation of the

"temperature-compensating," EIA Class I ceramic materials. Modern C0G (NP0) formulations contain neodymium, samarium and other rare earth oxides.

C0G (NP0) ceramics offer one of the most stable capacitor dielectrics available. Capacitance change with temperature is 0 ± 30 ppm/°C which is less than $\pm 0.3\%$ C from -55°C to +125°C. Capacitance drift or hysteresis for C0G (NP0) ceramics is negligible at less than $\pm 0.05\%$ versus up to $\pm 2\%$ for films. Typical capacitance change with life is less than ±0.1% for C0G (NP0), one-fifth that shown by most other dielectrics. C0G (NP0) formulations show no aging characteristics.

PART NUMBER (see page 2 for complete part number explanation)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

Variation of Impedance with Ceramic Formulation f Impedance with Ceramic F
Impedance vs. Frequency
1000 pF - COG (NPO) vs X7R
0805

ANAK

C0G (NP0) Dielectric C0G (NP0) Dielectric

Specifications and Test Methods Specifications and Test Methods

C0G (NP0) Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

PAPER and EMBOSSED available for 01005

C0G (NP0) Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

AVX

RF/Microwave C0G (NP0) Capacitors (RoHS)

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

GENERAL INFORMATION

"U" Series capacitors are C0G (NP0) chip capacitors spe cially designed for "Ultra" low ESR for applications in the communications market. Max ESR and effective capacitance

DIMENSIONS: inches (millimeters)

 $\frac{1}{C}$

J, $\mathsf C$ $\bar{1}$

1210.

are met on each value producing lot to lot uniformity. Sizes available are EIA chip sizes 0402, 0603, 0805, and

inches (mm)

HOW TO ORDER

ELECTRICAL CHARACTERISTICS

Capacitance Values and Tolerances:

Size 0402 - 0.2 pF to 30 pF @ 1 MHz Size 0603 - 1.0 pF to 100 pF @ 1 MHz Size 0805 - 1.6 pF to 160 pF @ 1 MHz Size 1210 - 2.4 pF to 1000 pF @ 1 MHz

Temperature Coefficient of Capacitance (TC):

0±30 ppm/°C (-55° to +125°C)

Insulation Resistance (IR):

10¹² Ω min. @ 25°C and rated WVDC 10¹¹ Ω min. @ 125°C and rated WVDC

Working Voltage (WVDC):

Dielectric Working Voltage (DWV): 250% of rated WVDC

Equivalent Series Resistance Typical (ESR):

ance Options for Specific Part Numbers.

- 0402 See Performance Curve, page 9
0603 See Performance Curve, page 9
- 0603 See Performance Curve, page 9
0805 See Performance Curve, page 9
- 0805 See Performance Curve, page 9
1210 See Performance Curve, page 9
	- See Performance Curve, page 9
- **Marking:** Laser marking EIA J marking standard (except 0603) (capacitance code and tolerance upon request).

MILITARY SPECIFICATIONS

Meets or exceeds the requirements of MIL-C-55681

 \sqrt{N} 120216

RF/Microwave C0G (NP0) Capacitors (RoHS)

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

CAPACITANCE RANGE

ULTRA LOW ESR, "U" SERIES

TYPICAL ESR vs. FREQUENCY 0603 "U" SERIES

ESR Measured on the Boonton 34A

RF/Microwave C0G (NP0) Capacitors

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

Erequency (GHz)

10 **ANYAN** 120216

RF/Microwave C0G (NP0) Capacitors (Sn/Pb)

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

GENERAL INFORMATION

"U" Series capacitors are C0G (NP0) chip capacitors specially designed for "Ultra" low ESR for applications in the communications market. Max ESR and effective capacitance are met on each value producing lot to lot uniformity. Sizes available are EIA chip sizes 0402, 0603, 0805, and 1210.

DIMENSIONS: inches (millimeters)

inches (mm)

HOW TO ORDER

Not RoHS Compliant *

ELECTRICAL CHARACTERISTICS

Capacitance Values and Tolerances:

Size 0402 - 0.2 pF to 22 pF @ 1 MHz Size 0603 - 1.0 pF to 100 pF @ 1 MHz Size 0805 - 1.6 pF to 160 pF @ 1 MHz Size 1210 - 2.4 pF to 1000 pF @ 1 MHz

Temperature Coefficient of Capacitance (TC): 0±30 ppm/°C (-55° to +125°C)

Insulation Resistance (IR): 10¹² Ω min. @ 25°C and rated WVDC

10¹¹ Ω min. @ 125°C and rated WVDC

Working Voltage (WVDC):

Dielectric Working Voltage (DWV): 250% of rated WVDC

Equivalent Series Resistance Typical (ESR):

- 0402 See Performance Curve, page 12
0603 See Performance Curve, page 12
- 0603 See Performance Curve, page 12
0805 See Performance Curve, page 12
- 0805 See Performance Curve, page 12
1210 See Performance Curve, page 12
- See Performance Curve, page 12

Marking: Laser marking EIA J marking standard (except 0603) (capacitance code and tolerance upon request).

MILITARY SPECIFICATIONS

Meets or exceeds the requirements of MIL-C-55681

RF/Microwave C0G (NP0) Capacitors (Sn/Pb)

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

CAPACITANCE RANGE

ULTRA LOW ESR, "U" SERIES

TYPICAL ESR vs. FREQUENCY 0603 "U" SERIES

ESR Measured on the Boonton 34A

12 REV 1

RF/Microwave Automotive C0G (NP0) Capacitors (RoHS), AEC Q200 Qualified

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

GENERAL INFORMATION

Automotive "U" Series capacitors are C0G (NP0) chip capacitors specially designed for "Ultra" low ESR for applications in the automotive market. Max ESR and effective capacitance are met on each value producing lot to lot uniformity. Sizes available are EIA chip sizes 0402 and 0603.

DIMENSIONS: mm (inches)

ELECTRICAL CHARACTERISTICS

Capacitance Values and Tolerances:

Size 0402 - 0.2 pF to 22 pF @ 1 MHz Size 0603 - 1.0 pF to 100 pF @ 1 MHz

Temperature Coefficient of Capacitance (TC): 0±30 ppm/°C (-55° to +125°C)

Insulation Resistance (IR):

10¹² Ω min. @ 25°C and rated WVDC 10¹¹ Ω min. @ 125°C and rated WVDC

Working Voltage (WVDC):
Size Working Voltage

Working Voltage 0402 - 50, 25 WVDC 0603 - 200, 100, 50 WVDC

Dielectric Working Voltage (DWV):

250% of rated WVDC

Equivalent Series Resistance Typical (ESR):

0402 - See Performance Curve 0603 - See Performance Curve

Automotive Specifications

Meets or exceeds the requirements of AEC Q200

RF/Microwave Automotive C0G (NP0)

Capacitors (RoHS), AEC Q200 Qualified

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

CAPACITANCE RANGE

ULTRA LOW ESR, "U" SERIES

TYPICAL ESR vs. FREQUENCY 0603 "U" SERIES

TYPICAL SERIES RESONANT FREQUENCY "U" SERIES CHIP

Designer Kits

Communication Kits "U" Series

"U" SERIES KITS

*****25 each of 15 values**

*****25 each of 24 values**

0805

*****25 each of 30 values**

*****25 each of 30 values**

X8R/X8L Dielectric General Specifications

AVX has developed a range of multilayer ceramic capacitors designed for use in applications up to 150°C. These capacitors are manufactured with an X8R and an X8L dielectric material. X8R material has capacitance variation of ± 15% between -55°C and +150°C. The X8L material has capacitance variation of ±15% between -55°C to 125°C to 125°C and +15/40% from +125°C to +150°C.

The need for X8R and X8L performance has been driven by customer requirements for parts that operate at elevated temperatures. They provide a highly reliable capacitor with low loss and stable capacitance over temperature.

They are ideal for automotive under the hood sensors, and various industrial applications. Typical industrial application would be drilling monitoring system. They can also be used as bulk capacitors for high temperature camera modules.

Both X8R and X8L dielectric capacitors are automotive AEC-Q200 qualified. Optional termination systems, tin, FLEXITERM® and conductive epoxy for hybrid applications are available. Providing this series with our FLEXITERM® termination system provides further advantage to customers by way of enhanced resistance to both, temperature cycling and mechanical damage.

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

X8R/X8L Dielectric

General Specifications

APPLICATIONS FOR X8R AND X8L CAPACITORS

- All market sectors with a 150°C requirement
- Automotive on engine applications
- Oil exploration applications
- Hybrid automotive applications
	- Battery control
	- Inverter / converter circuits
	- Motor control applications
	- Water pump
- Hybrid commercial applications
	- Emergency circuits
	- Sensors
	- Temperature regulation

ADVANTAGES OF X8R AND X8L MLC CAPACITORS

- Both ranges are qualified to the highest automotive AEC-Q200 standards
- Excellent reliability compared to other capacitor technologies
- RoHS compliant
- Low ESR / ESL compared to other technologies
- Tin solder finish
- FLEXITERM® available
- Epoxy termination for hybrid available
- 100V range available

ENGINEERING TOOLS FOR HIGH VOLTAGE MLC CAPACITORS

- Samples
- Technical Articles
- Application Engineering
- Application Support

X8R/X8L Dielectric

Specifications and Test Methods

X7R Dielectric

General Specifications

X7R formulations are called "temperature stable" ceramics and fall into EIA Class II materials. X7R is the most popular of these intermediate dielectric constant materials. Its temperature variation of capacitance is within ±15% from -55°C to +125°C. This capacitance change is non-linear.

Capacitance for X7R varies under the influence of electrical operating con-ditions such as voltage and frequency.

X7R dielectric chip usage covers the broad spectrum of industrial applications where known changes in capacitance due to applied voltages are acceptable.

PART NUMBER (see page 2 for complete part number explanation)

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

ANAK

X7R Dielectric

Specifications and Test Methods

X7R Dielectric Capacitance Range

PREFERRED SIZES ARE SHADED

PAPER and EMBOSSED available for 01005

NOTE: Contact factory for non-specified capacitance values

*EIA 01005 **Contact Factory for Specifications

X7R Dielectric

Capacitance Range

AVAK

PREFERRED SIZES ARE SHADED

NOTE: Contact factory for non-specified capacitance values

X7S Dielectric

General Specifications

GENERAL DESCRIPTION

X7S formulations are called "temperature stable" ceramics and fall into EIA Class II materials. Its temperature variation of capacitance s within $\pm 22\%$ from -55° C to $+125^{\circ}$ C. This capacitance change is non-linear.

Capacitance for X7S varies under the influence of electrical operating conditions such as voltage and frequency.

X7S dielectric chip usage covers the broad spectrum of industrial applications where known changes in capacitance due to applied voltages are acceptable.

PART NUMBER (see page 2 for complete part number explanation)

NOTE: Contact factory for availability of Tolerance Options for Specific Part Numbers.

TYPICAL ELECTRICAL CHARACTERISTICS

Variation of Impedance with Chip Size Impedance vs. Frequency 100,000 pF - X7S

 101316 23

X7S Dielectric

Specifications and Test Methods

X7S Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

*Contact Factory for Specifications

X5R Dielectric

General Specifications

GENERAL DESCRIPTION

- General Purpose Dielectric for Ceramic Capacitors
- EIA Class II Dielectric
- Temperature variation of capacitance is within ±15% from -55°C to +85°C
- Well suited for decoupling and filtering applications
- Available in High Capacitance values (up to 100µF)

PART NUMBER (see page 2 for complete part number explanation)

NOTE: Contact factory for availability of Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

TYPICAL ELECTRICAL CHARACTERISTICS

X5R Dielectric C0G (NP0) Dielectric

Specifications and Test Methods Specifications and Test Methods

PREFERRED SIZES ARE SHADED

PAPER and EMBOSSED available for 01005

NOTE: Contact factory for non-specified capacitance values *EIA 01005

PREFERRED SIZES ARE SHADED

PAPER and EMBOSSED available for 01005

NOTE: Contact factory for non-specified capacitance values *EIA 01005

Y5V Dielectric

General Specifications

Y5V formulations are for general-purpose use in a limited temperature range. They have a wide temperature characteristic of +22% –82% capacitance change over the operating temperature range of –30°C to +85°C.

These characteristics make Y5V ideal for decoupling applications within limited temperature range.

PART NUMBER (see page 2 for complete part number explanation)

 $50V = 5$

3

Dielectric $Y5V = G$

G

Capacitance Code (In pF) 2 Sig. Digits + Number of Zeros

Z

Failure Rate $A = Not$ Applicable

A

Terminations T = Plated Ni and Sn **Packaging** $2 = 7"$ Reel $4 = 13"$ Reel

2

T

A

 $\frac{\Delta}{\delta}$ $+20$
 $+10$
 -10
 -20
 -30
 -40
 -50 $+10 0 -$ -55 -35 -15 +5 +25 +45 +65 +85 +105 +125 Temperature °C **Temperature Coefficient** -60 -50 -40 -30 -20 -10 -70 -80

 $J \sim V J \sim$ 101316

Y5V Dielectric

Specifications and Test Methods

Y5V Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

MLCC Gold Termination – AU Series

General Specifications

AVX Corporation will support those customers for commercial and military Multilayer Ceramic Capacitors with a termination consisting of Gold. This termination is indicated by the use of a "7" or "G" in the 12th position of the AVX Catalog Part Number. This fulfills AVX's commitment to providing a full range of products to our customers. Please contact the factory if you require additional information on our MLCC Gold Termination.

PART NUMBER

* Contact factory for availability.

MLCC Gold Termination – AU Series

Capacitance Range (NP0 Dielectric)

PREFERRED SIZES ARE SHADED

MLCC Gold Termination – AU Series

Capacitance Range (NP0 Dielectric)

PREFERRED SIZES ARE SHADED \Box \Box \Box **SIZE AU10 AU12 AU13 AU14** Preflow/Epoxy/ Reflow/Epoxy/ Reflow/Epoxy/ Reflow/Epoxy/ Reflow/Epoxy/ Wire Bond* Wire Bon **Soldering** Reflow/Epoxy/ I Reflow/Epoxy/ Reflow/Epoxy/ Reflow/Epoxy/ Reflow/Epoxy/ Reflow/Epoxy/ **Packaging I** Paper/Embossed I All Embossed All Embossed All Embossed All Embossed All Embossed (L) Length mm 3.20 ± 0.20 4.50 ± 0.30 ± 0.30 ± 0.30 ± 0.30 ± 0.30 ± 0.27 ± 0.250 ± 0.30 ± 0.30 ± 0.30 ± 0.30 ±
(L) Length m.s. 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.31 = 0.3 (in.) (0.126 ± 0.008) (0.177 ± 0.012) (0.177 ± 0.012) (0.225 ± 0.010) (M) Width mm 2.50 ± 0.20 ± 0.20 ± 0.20 ± 0.20 ± 0.40 ± 0.40 ± 0.25 ± 0.25 ± 0.25 ± 0.25 ± 0.25 ± 0.25 ± 0.25
M) Width Mars Monet (in.) (0.098 ± 0.008) (0.126 ± 0.008) (0.252 ± 0.016) (0.250 ± 0.010) (t) Terminal mm 10.50± 0.50 ± 0.35 ± 0.36 ± 0.36 ± 0.36 ± 0.36 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± 0.39
(t) Terminal m 10.025 0.04 ± 0.021 ± 0.021 ± 0.021 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± 0.39 ± (in.) (0.020 ± 0.010) (0.024 ± 0.014) (0.024 ± 0.014) (0.025 ± 0.015) WVDC | 25 | 50 | 100 | 200 | 500 | 25 | 50 | 100 | 200 | 500 | 50 | 100 | 200 | 50 | 100 | 200 Cap 0.5 (pF) 1.0 1.2 1.5 1.8 2.2 ٠W 2.7 \mathbb{F} 3.3 3.9 4.7 5.6 ł۳ 6.8 8.2 10 J J J J 12 J J J J 15 J J J J 18 J 22 July 22 July 22 July 2014 27 J J J J 33 J 39 J 47 J J J J 56 J J J J J 68 J 82 J J J J J 100 J J J J 120 J J J J J 150 J J J J 180 J J J J J J 220 J J J J J 270 J 330 J 390 M 470 M 560 J J J J M 680 J J J J M 820 J J J J M 1000 J J J J M K K K K M M M M M M P 1200 J J J M M K K K K M M M M M M P 1500 J J J J J M J M J K | K | K | M J M J M J M J M J M J P 1800 J J J M K K K K M M M M M M P 2200 J J J J Q J J K | K | K | K | P | M | M | M | M | M | M | P 2700 J J J J J Q H K K K P Q M M M M M M M M P 3300 J J J J J J H K | K | K | P | Q | M | M | M | M | M | M | M 3900 J J J J M J H K | K | K | P | Q | M | M | M | M | M | M | P 4700 | J | J | M | K | K | K | P | Q | M | M | M | M | M | M | P 5600 J J J J J J J K | K | K | M | P | X | M | M | M | M | M | M | P 6800 J J J J J J | K | K | M | X | I M | M | M | M | M | M | M | P 8200 J J K M M M M M M P Cap 0.010 J J K M M M M M M P (μF) 0.012 J J K M M M M M P 0.015 **| | | | | | M | M | M | M | M | M | M** | Y 0.018 M M P M M M Y 0.022 **| | | | | | M | M | | | | | | | | P** | | | | | | | M | | Y | | Y 0.027 M M P P Y Y 0.033 M M P P 0.039 M M P P 0.047 M M P P 0.068 M M P 0.082 **| | | | | | | | | | | | | | | | | |** | Q 0.1 | | | | | | | | | | | | | | | Q WVDC | 25 | 50 | 100 | 200 | 500 | 25 | 50 | 100 | 200 | 500 | 50 | 100 | 200 | 50 | 100 | 200 **SIZE AU10 AU12 AU13 AU14** * Contact factory

MLCC Gold Termination - AU Series Capacitance Range (X7R Dielectric)

PREFERRED SIZES ARE SHADED

ANAK

PREFERRED SIZES ARE SHADED

ANAK

MLCC Gold Termination – AU Series

Capacitance Range (X5R Dielectric)

PREFERRED SIZES ARE SHADED

= *Optional Specifications – **Contact factory**

NOTE: Contact factory for non-specified capacitance values

MLCC Gold Termination – AU Series

AU16/AU17/AU18

PHYSICAL DIMENSIONS AND PAD LAYOUT

PHYSICAL DIMENSIONS mm (in)

T - See Range Chart for Thickness and Codes

PAD LAYOUT DIMENSIONS mm (in)

Solid = X7R = X5R = X7S

C0G (NP0) – General Specifications

AVX Corporation will support those customers for commercial and military Multilayer Ceramic Capacitors with a termination consisting of 5% minimum lead. This termination is indicated by the use of a "B" in the 12th position of the AVX Catalog Part Number. This fulfills AVX's commitment to providing a full range of products to our customers. AVX has provided in the following pages a full range of values that we are currently offering in this special "B" termination. Please contact the factory if you require additional information on our MLCC Tin/Lead Termination "B" products.

Not RoHS Compliant

See FLEXITERM® section for CV options

PART NUMBER (see page 2 for complete part number explanation)

*LD04 has the same CV ranges as LD03.

NOTE: Contact factory for availability of Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

C0G (NP0) – Specifications and Test Methods

Capacitance Range (NP0 Dielectric)

PREFERRED SIZES ARE SHADED

Capacitance Range (NP0 Dielectric)

PREFERRED SIZES ARE SHADED

X8R – General Specifications

AVX Corporation will support those customers for commercial and military Multilayer Ceramic Capacitors with a termination consisting of 5% minimum lead. This termination is indicated by the use of a "B" in the 12th position of the AVX Catalog Part Number. This fulfills AVX's commitment to providing a full range of products to our customers. AVX has provided in the following pages a full range of values that we are currently offering in this special "B" termination. Please contact the factory if you require additional information on our MLCC Tin/Lead Termination "B" products.

Not RoHS Compliant

PART NUMBER (see page 2 for complete part number explanation)

*LD04 has the same CV ranges as LD03.

See FLEXITERM® section for CV options

NOTE: Contact factory for availability of Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

X8R – Specifications and Test Methods

Capacitance Range (X8R Dielectric)

X7R – General Specifications

AVX Corporation will support those customers for commercial and military Multilayer Ceramic Capacitors with a termination consisting of 5% minimum lead. This termination is indicated by the use of a "B" in the 12th position of the AVX Catalog Part Number. This fulfills AVX's commitment to providing a full range of products to our customers. AVX has provided in the following pages a full range of values that we are currently offering in this special "B" termination. Please contact the factory if you require additional information on our MLCC Tin/Lead Termination "B" products.

Not RoHS Compliant

PART NUMBER (see page 2 for complete part number explanation)

*LD04 has the same CV ranges as LD03.

NOTE: Contact factory for availability of Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

Variation of Impedance with Chip Size Impedance vs. Frequency
10,000 pF - X7R 10 1206 0805 Impedance, 0 1.0 $\mathbf{0}$. $.01$ $1,000$ 10 100 Frequency, MHz

See FLEXITERM® section for CV options

Variation of Impedance with Chip Size Impedance vs. Frequency 100,000 pF X7R

X7R – Specifications and Test Methods

Capacitance Range (X7R Dielectric)

PREFERRED SIZES ARE SHADED

= Under Development

Capacitance Range (X7R Dielectric)

PREFERRED SIZES ARE SHADED

X5R – General Specifications

AVX Corporation will support those customers for commercial and military Multilayer Ceramic Capacitors with a termination consisting of 5% minimum lead. This termination is indicated by the use of a "B" in the 12th position of the AVX Catalog Part Number. This fulfills AVX's commitment to providing a full range of products to our customers. AVX has provided in the following pages a full range of values that we are currently offering in this special "B" termination. Please contact the factory if you require additional information on our MLCC Tin/Lead Termination "B" products.

Not RoHS Compliant

PART NUMBER (see page 2 for complete part number explanation)

*LD04 has the same CV ranges as LD03.

See FLEXITERM® section for CV options

NOTE: Contact factory for availability of Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.

TYPICAL ELECTRICAL CHARACTERISTICS

X5R – Specifications and Test Methods

Capacitance Range (X5R Dielectric)

PREFERRED SIZES ARE SHADED

***Optional Specifications** – **Contact factory**

NOTE: Contact factory for non-specified capacitance values

MLCC Low Profile

General Specifications

GENERAL DESCRIPTION

AVX introduces the LT series comprising a range of low profile products in our X5R and X7R dielectric. X5R is a Class II dielectric with temperature varation of capacitance within $\pm 15\%$ from -55° C to $+85^{\circ}$ C. Offerings include 0201, 0402, 0603, 0805 1206, and 1210 packages in compact, low profile designs. The LT series is ideal for decoupling and filtering applications where height clearance is limited.

AVX is also expanding the low profile products in our X7R dielectric. X7R is a Class II dielectric with temperature variation of capacitance within ±15% from -55ºC to +125ºC. Please contact the factory for availability of any additional values not listed.

PART NUMBER (see page 2 for complete part number explanation)

NOTE: Contact factory for availability of tolerance options for specific part numbers.

GENERAL DESCRIPTON

AVX Corporation has supported the Automotive Industry requirments for Multilayer Ceramic Capacitors consistently for more than 10 years. Products have been developed and tested specifically for automotive applications and all manufacturing facilities are QS9000 and VDA 6.4 approved.

As part of our sustained investment in capacity and state of the art technology, we are now transitioning from the established Pd/Ag electrode system to a Base Metal Electrode system (BME).

AVX is using AECQ200 as the qualification vehicle for this transition. A detailed qualification package is available on request and contains results on a range of part numbers including:

- X7R dielectric components containing BME electrode and copper terminations with a Ni/Sn plated overcoat
- X7R dielectric components, BME electrode with epoxy finish for conductive glue mounting

AVAK

HOW TO ORDE

Contact factory for availability of Tolerance Options for Specific Part Numbers.

NOTE: Contact factory for non-specified capacitance values 0402 case size available in T termination only.

COMMERCIAL VS AUTOMOTIVE MLCC PROCESS COMPARISON

All Tests have Accept/Reject Criteria 0/1

Automotive MLCC NP0/X7R Dielectric

FLEXITERM FEATURES

- a) Bend Test
	- The capacitor is soldered to the PC Board as shown:

Typical bend test results are shown below:

- b) Temperature Cycle testing
	- FLEXITERM® has the ability to withstand at least 1000 cycles between -55°C and +125°C

Automotive MLCC-NP0 Capacitance Range

Automotive MLCC - X7R Capacitance Range

Automotive MLCC - X8R Capacitance Range

APS COTS+ for High Reliability Applications Surface Mount NP0, X7R and X8R/L MLCCs

AVX's APS COTS+ series of multilayer ceramic capacitors offers the customer a high reliability solution with an ultralow failure rate, ≤1ppb, in a variety of case sizes and voltages. The APS range encompasses a wide range of dielectric types to meet the customer's requirements from low temperature/voltage capacitance change dielectric, NP0, to high preforming capacitance voltage X7R to high temperature reliability dielectrics, X8R/L.

APS capacitors have a wider capacitance range than MIL spec parts that satisfies the need for higher CV demands and board space saving requirements. Each production lot is extensively tested and removes the requirement for customer specific drawings. The testing regime uses many of the MIL-STD test methods as per MIL-PRF-55681 and has a field failure rate of less than 1 ppb. The APS testing series uses AVX's unique in-house maverick testing detection system that eliminates infant mortality failures.

Applications suitable for APS include Industrial, Telecommunications, Aviation, and Military. The APS is available with a range of different termination finishes, Flexiterm®, Nickel / Tin and Tin with Pb1. Flexiterm® technology delivers improved thermo-mechanical stress resistance.

AVX'S APS RELIABILITY TEST SUMMARY

- 100% Visual Inspection
- DPA
- IR, DF, Cap, DWV
- Maverick Lot Review
- Thermal Shocl
- 85/85 Testing
- Life Testing 125°C 2xRV
- C of C with every Order
- Quarterly Data Package

FEATURES

- The APS range has been extensively reliability tested as standard resulting in an ultralow failure rate, ≤1ppb
- The APS range is available with Flexiterm[®] that deliver's high thermo-mechanical stress resistance.
- High CV range enabling board space saving requirements.

HOW TO ORDER

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Number.

APS COTS+ NP0 Series

Capacitance Range

TS 16949, ISO 9001Certified

APS COTS+ X7R Series

Capacitance Range

TS 16949, ISO 9001Certified

APS COTS+ X8R/L Series

Capacitance Range

TS 16949, ISO 9001Certified

General Specifications

GENERAL DESCRIPTION

With increased requirements from the automotive industry for additional component robustness, AVX recognized the need to produce a MLCC with enhanced mechanical strength. It was noted that many components may be subject to severe flexing and vibration when used in various under the hood automotive and other harsh environment applications.

To satisfy the requirement for enhanced mechanical strength, AVX had to find a way of ensuring electrical integrity is maintained whilst external forces are being applied to the component. It was found that the structure of the termination needed to be flexible and after much research and development, AVX launched FLEXITERM®. FLEXITERM® is designed to enhance the mechanical flexure and temperature cycling performance of a standard ceramic capacitor with an X7R dielectric. **The industry standard for flexure is 2mm minimum. Using FLEXITERM**®**, AVX provides up to 5mm of flexure without internal cracks. Beyond 5mm, the capacitor will generally fail "open".**

As well as for automotive applications FLEXITERM® will provide Design Engineers with a satisfactory solution when designing PCB's which may be subject to high levels of board flexure.

PRODUCT ADVANTAGES

- High mechanical performance able to withstand, 5mm bend test guaranteed.
- Increased temperature cycling performance, 3000 cycles and beyond.
- Flexible termination system.
- Reduction in circuit board flex failures.
- Base metal electrode system.
- Automotive or commercial grade products available.

APPLICATIONS

High Flexure Stress Circuit Boards

• e.g. Depanelization: Components near edges of board.

Variable Temperature Applications

- Soft termination offers improved reliability performance in applications where there is temperature variation.
- e.g. All kind of engine sensors: Direct connection to battery rail.

Automotive Applications

- Improved reliability.
- Excellent mechanical performance and thermo mechanical performance.

HOW TO ORDER

NOTE: Contact factory for availability of Tolerance Options for Specific Part Numbers.

Specifications and Test Methods

AEC-Q200 Qualification:

- Created by the Automotive Electronics Council
- Specification defining stress test qualification for passive components

Testing:

Key tests used to compare soft termination to AEC-Q200 qualification:

• Bend Test

• Temperature Cycle Test

BOARD BEND TEST RESULTS

AEC-Q200 Vrs AVX FLEXITERM® Bend Test

TABLE SUMMARY

Typical bend test results are shown below:

TEMPERATURE CYCLE TEST PROCEDURE

Test Procedure as per AEC-Q200:

The test is conducted to determine the resistance of the component when it is exposed to extremes of alternating high and low temperatures.

- Sample lot size quantity 77 pieces
- TC chamber cycle from -55ºC to +125ºC for 1000 cycles
- Interim electrical measurements at 250, 500, 1000 cycles
- Measure parameter capacitance dissipation factor, insulation resistance

PERFORMANCE TESTING BOARD BEND TEST PROCEDURE

According to AEC-Q200

Test Procedure as per AEC-Q200: Sample size: 20 components

Span: 90mm Minimum deflection spec: 2 mm

- Components soldered onto FR4 PCB (Figure 1)
- Board connected electrically to the test equipment (Figure 2)

BEND TESTPLATE

Fig 1 - PCB layout with electrical connections

Fig 2 - Board Bend test equipment

AVX ENHANCED SOFT TERMINATION BEND TEST PROCEDURE

CONTROL PANEL

CONNECTOR

Bend Test

The capacitor is soldered to the printed circuit board as shown and is bent up to 10mm at 1mm per second:

- The board is placed on 2 supports 90mm apart (capacitor side down)
- The row of capacitors is aligned with the load stressing knife

- The load is applied and the deflection where the part starts to crack is recorded (Note: Equipment detects the start of the crack using a highly sensitive current detection circuit)
- The maximum deflection capability is 10mm

Specifications and Test Methods

BEYOND 1000 CYCLES: TEMPERATURE CYCLE TEST RESULTS

Soft Term - No Defects up to 3000 cycles

FLEXITERM® TEST SUMMARY

- Qualified to AEC-Q200 test/specification with the exception of using AVX 3000 temperature cycles (up to +150°C bend test guaranteed greater than 5mm).
- FLEXITERM® provides improved performance compared to standard termination systems.
- **AEC-Q200 specification states 1000 cycles compared to AVX 3000 temperature cycles.**
- Board bend test improvement by a factor of 2 to 4 times.
- Temperature Cycling:
	- 0% Failure up to 3000 cycles
	- No ESR change up to 3000 cycles

WITHOUT SOFT TERMINATION WITH SOFT TERMINATION

X8R Dielectric Capacitance Range

AEC-Q200 Qualified

X7R Dielectric Capacitance Range

 \sqrt{N} 020117

FLEXISAFE MLC Chips

For Ultra Safety Critical Applications

AVX have developed a range of components specifically for safety critical applications.

Utilizing the award-winning FLEXITERM™ layer in conjunction with the cascade design previously used for high voltage MLCCs, a range of ceramic capacitors is now available for customers who require components designed with an industry leading set of safety features.

The FLEXITERM™ layer protects the component from any damage to the ceramic resulting from mechanical stress during PCB assembly or use with end customers. Board flexure type mechanical damage accounts for the majority of MLCC failures. The addition of the cascade structure protects the component from low insulation resistance failure resulting from other common causes for failure; thermal stress damage, repetitive strike ESD damage and placement damage. With the inclusion of the cascade design structure to complement the FLEXITERM™ layer, the FLEXISAFE range of capacitors has unbeatable safety features.

HOW TO ORDER

Capacitance Tolerance $J = \pm 5\%$ $K = \pm 10\%$ $M = \pm 20\%$

K

Failure Rate A = Commercial 4 = Automotive $Q = APS$

Q

Terminations $Z = FLEXITERM^{TM}$ * X = FLEXITERMTM with 5% min lead

*Not RoHS Compliant

Z

2 Packaging 2 = 7" Reel 4 = 13" Reel

A Special Code A = Std. Product

FLEXISAFE X7R RANGE

Qualified

Capacitor Array

Capacitor Array (IPC)

BENEFITS OF USING CAPACITOR

ARRAYS

AVX capacitor arrays offer designers the opportunity to lower placement costs, increase assembly line output through lower component count per board and to reduce real estate requirements.

Reduced Costs

Placement costs are greatly reduced by effectively placing one device instead of four or two. This results in increased throughput and translates into savings on machine time. Inventory levels are lowered and further savings are made on solder materials, etc.

Space Saving

Space savings can be quite dramatic when compared to the use of discrete chip capacitors. As an example, the 0508 4-element array offers a space reduction of >40% vs. 4 x 0402 discrete capacitors and of >70% vs. 4 x 0603 discrete capacitors. (This calculation is dependent on the spacing of the discrete components.)

Increased Throughput

Assuming that there are 220 passive components placed in a mobile phone:

A reduction in the passive count to 200 (by replacing discrete components with arrays) results in an increase in throughput of approximately 9%.

A reduction of 40 placements increases throughput by 18%.

For high volume users of cap arrays using the very latest placement equipment capable of placing 10 components per second, the increase in throughput can be very significant and can have the overall effect of reducing the number of placement machines required to mount components:

If 120 million 2-element arrays or 40 million 4-element arrays were placed in a year, the requirement for placement equipment would be reduced by one machine.

During a 20Hr operational day a machine places 720K components. Over a working year of 167 days the machine can place approximately 120 million. If 2-element arrays are mounted instead of discrete components, then the number of placements is reduced by a factor of two and in the scenario where 120 million 2-element arrays are placed there is a saving of one pick and place machine.

Smaller volume users can also benefit from replacing discrete components with arrays. The total number of placements is reduced thus creating spare capacity on placement machines. This in turn generates the opportunity to increase overall production output without further investment in new equipment.

W2A (0508) Capacitor Arrays

The 0508 4-element capacitor array gives a PCB space saving of over 40% vs four 0402 discretes and over 70% vs four 0603 discrete capacitors.

The 0612 4-element capacitor array gives a PCB space saving of over 50% vs four 0603 discretes and over 70% vs four 0805 discrete capacitors.

Capacitor Array

Capacitor Array (IPC)

GENERAL DESCRIPTION

AVX is the market leader in the development and manufacture of capacitor arrays. The array family of products also includes the 0612 4-element device as well as 0508 2-element and 4-element series, all of which have received widespread acceptance in the marketplace.

AVX capacitor arrays are available in X5R, X7R and NP0 (C0G) ceramic dielectrics to cover a broad range of capacitance values. Voltage ratings from 6.3 Volts up to 100 Volts are offered. AVX also now offers a range of automotive capacitor arrays qualified to AEC-Q200 (see separate table).

Key markets for capacitor arrays are Mobile and Cordless Phones, Digital Set Top Boxes, Computer Motherboards and Peripherals as well as Automotive applications, RF Modems, Networking Products, etc.

HOW TO ORDER

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.
Capacitor Array Capacitance Range – NP0/C0G

Supported Values

Capacitor Array

Capacitance Range – X7R

Automotive Capacitor Array (IPC)

As the market leader in the development and manufacture of capacitor arrays AVX is pleased to offer a range of AEC-Q200 qualified arrays to compliment our product offering to the Automotive industry. Both the AVX 0612 and 0508 4-element capacitor array styles are qualified to the AEC-Q200 automotive specifications.

AEC-Q200 is the Automotive Industry qualification standard and a detailed qualification package is available on request.

All AVX automotive capacitor array production facilities are certified to ISO/TS 16949:2002.

HOW TO ORDER

*Contact factory for availability by part number for $K = \pm 10\%$ and $J = \pm 5\%$ tolerance.

Not RoHS Compliant

For RoHS compliant products, please select correct termination style.

(1000)

Capacitor Array

PART & PAD LAYOUT DIMENSIONS millimeters (inches)

PART DIMENSIONS

0508 - 2 Element

0612 - 4 Element

PAD LAYOUT DIMENSIONS 0508 - 2 Element

0612 - 4 Element

Low Inductance Capacitors

Introduction

The signal integrity characteristics of a Power Delivery Network (PDN) are becoming critical aspects of board level and semiconductor package designs due to higher operating frequencies, larger power demands, and the ever shrinking lower and upper voltage limits around low operating voltages. These power system challenges are coming from mainstream designs with operating frequencies of 300MHz or greater, modest ICs with power demand of 15 watts or more, and operating voltages below 3 volts.

The classic PDN topology is comprised of a series of capacitor stages. Figure 1 is an example of this architecture with multiple capacitor stages.

An ideal capacitor can transfer all its stored energy to a load instantly. A real capacitor has parasitics that prevent instantaneous transfer of a capacitor's stored energy. The true nature of a capacitor can be modeled as an RLC equivalent circuit. For most simulation purposes, it is possible to model the characteristics of a real capacitor with one

capacitor, one resistor, and one inductor. The RLC values in this model are commonly referred to as equivalent series capacitance (ESC), equivalent series resistance (ESR), and equivalent series inductance (ESL).

The ESL of a capacitor determines the speed of energy transfer to a load. The lower the ESL of a capacitor, the faster that energy can be transferred to a load. Historically, there has been a tradeoff between energy storage (capacitance) and inductance (speed of energy delivery). Low ESL devices typically have low capacitance. Likewise, higher capacitance devices typically have higher ESLs. This tradeoff between ESL (speed of energy delivery) and capacitance (energy storage) drives the PDN design topology that places the fastest low ESL capacitors as close to the load as possible. Low Inductance MLCCs are found on semiconductor packages and on boards as close as possible to the load.

Figure 1 Classic Power Delivery Network (PDN) Architecture

LOW INDUCTANCE CHIP CAPACITORS

The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL. A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer side of its rectangular shape.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL then an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC versus a standard MLCC.

INTERDIGITATED CAPACITORS

The size of a current loop has the greatest impact on the ESL characteristics of a surface mount capacitor. There is a secondary method for decreasing the ESL of a capacitor. This secondary method uses adjacent opposing current loops to reduce ESL. The InterDigitated Capacitor (IDC) utilizes both primary and secondary methods of reducing inductance. The IDC architecture shrinks the distance between terminations to minimize the current loop size, then further reduces inductance by creating adjacent opposing current loops.

An IDC is one single capacitor with an internal structure that has been optimized for low ESL. Similar to standard MLCC versus LICCs, the reduction in ESL varies by EIA case size. Typically, for the same EIA size, an IDC delivers an ESL that is at least 80% lower than an MLCC.

Low Inductance Capacitors

Introduction

LAND GRID ARRAY (LGA) CAPACITORS

Land Grid Array (LGA) capacitors are based on the first Low ESL MLCC technology created to specifically address the design needs of current day Power Delivery Networks (PDNs). This is the 3rd low inductance capacitor technology developed by AVX. LGA technology provides engineers with new options. The LGA internal structure and manufacturing technology eliminates the historic need for a device to be physically small to create small current loops to minimize inductance.

The first family of LGA products are 2 terminal devices. A 2 terminal 0306 LGA delivers ESL performance that is equal to or better than an 0306 8 terminal IDC. The 2 terminal 0805 LGA delivers ESL performance that approaches the 0508 8 terminal IDC. New designs that would have used 8 terminal IDCs are moving to 2 terminal LGAs because the layout is easier for a 2 terminal device and manufacturing yield is better for a 2 terminal LGA versus an 8 terminal IDC.

LGA technology is also used in a 4 terminal family of products that AVX is sampling and will formerly introduce in 2008. Beyond 2008, there are new multi-terminal LGA product families that will provide even more attractive options for PDN designers.

LOW INDUCTANCE CHIP ARRAYS (LICA®)

The LICA® product family is the result of a joint development effort between AVX and IBM to develop a high performance MLCC family of decoupling capacitors. LICA was introduced in the 1980s and remains the leading choice of designers in high performance semiconductor packages and high reliability board level decoupling applications.

LICA® products are used in 99.999% uptime semiconductor package applications on both ceramic and organic substrates. The C4 solder ball termination option is the perfect compliment to flip-chip packaging technology. Mainframe class CPUs, ultimate performance multi-chip modules, and communications systems that must have the reliability of 5 9's use LICA®.

LICA® products with either Sn/Pb or Pb-free solder balls are used for decoupling in high reliability military and aerospace applications. These LICA® devices are used for decoupling of large pin count FPGAs, ASICs, CPUs, and other high power ICs with low operating voltages.

When high reliability decoupling applications require the very lowest ESL capacitors, LICA® products are the best option.

470 nF 0306 Impedance Comparison

Figure 2 MLCC, LICC, IDC, and LGA technologies deliver different levels of equivalent series inductance (ESL).

Low Inductance Ceramic Capacitors LICC

0306/0508/0612 RoHS Compliant

GENERAL DESCRIPTION

The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL.

A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer sides of its rectangular shape. The image on the right shows the termination differences between an MLCC and an LICC.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL then an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC versus a standard MLCC.

AVX LICC products are available with a lead-free finish of plated Nickel/Tin.

HOW TO ORDER

PERFORMANCE CHARACTERISTICS

***See the thickness tables on the next page.**

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

TYPICAL IMPEDANCE CHARACTERISTICS

Low Inductance Ceramic Capacitors LICC

0306/0508/0612 RoHS Compliant

 \exists = X6S

PHYSICAL DIMENSIONS AND PAD LAYOUT

PHYSICAL DIMENSIONS

T - See Range Chart for Thickness and Codes

PAD LAYOUT DIMENSIONS

 \mathbf{r}

Low Inductance Capacitors with SnPb Terminations

LD16/LD17/LD18 Tin-Lead Termination "B"

GENERAL DESCRIPTION

The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL.

A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer sides of its rectangular shape. The image on the right shows the termination differences between an MLCC and an LICC.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL then an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC versus a standard MLCC.

AVX LICC products are available with a lead termination for high reliability military and aerospace applications that must avoid tin whisker reliability issues.

Not RoHS Compliant

MLCC LICC

PERFORMANCE CHARACTERISTICS

HOW TO ORDER

***See the thickness tables on the next page.**

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

TYPICAL IMPEDANCE CHARACTERISTICS

Low Inductance Capacitors with SnPb Terminations

LD16/LD17/LD18 Tin-Lead Termination "B"

PHYSICAL DIMENSIONS AND PAD LAYOUT

PHYSICAL DIMENSIONS

T - See Range Chart for Thickness and Codes

PAD LAYOUT DIMENSIONS

Solid = X7R = X5R

= X6S

W 1.02 (0.040) **A** 1.27 (0.050) **mm (in)**

IDC Low Inductance Capacitors (RoHS)

0306/0612/0508 IDC (InterDigitated Capacitors)

GENERAL DESCRIPTION

Inter-Digitated Capacitors (IDCs) are used for both semiconductor package and board level decoupling. The equivalent series inductance (ESL) of a single capacitor or an array of capacitors in parallel determines the response time of a Power Delivery Network (PDN). The lower the ESL of a PDN, the faster the response time. A designer can use many standard MLCCs in parallel to reduce ESL or a low ESL Inter-Digitated Capacitor (IDC) device. These IDC devices are available in versions with a maximum height of 0.95mm or 0.55mm.

IDCs are typically used on packages of semiconductor products with power levels of 15 watts or greater. Inter-Digitated Capacitors are used on CPU, GPU, ASIC, and ASSP devices produced on 0.13μ, 90nm, 65nm, and 45nm processes. IDC devices are used on both ceramic and organic package substrates. These low ESL surface mount capacitors can be placed on the bottom side or the top side of a package substrate. The low profile 0.55mm maximum height IDCs can easily be used on the bottom side of BGA packages or on the die side of packages under a heat spreader.

IDCs are used for board level decoupling of systems with speeds of 300MHz or greater. Low ESL IDCs free up valuable board space by reducing the number of capacitors required versus standard MLCCs. There are additional benefits to reducing the number of capacitors beyond saving board space including higher reliability from a reduction in the number of components and lower placement costs based on the need for fewer capacitors.

The Inter-Digitated Capacitor (IDC) technology was developed by AVX. This is the second family of Low Inductance MLCC products created by AVX. IDCs are a cost effective alternative to AVX's first generation low ESL family for high-reliability applications known as LICA (Low Inductance Chip Array).

AVX IDC products are available with a lead-free finish of plated Nickel/Tin.

HOW TO ORDER

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

PERFORMANCE CHARACTERISTICS

0612

+ – + –

+ – + –

0508

TYPICAL IMPEDANCE

IDC Low Inductance Capacitors (RoHS)

0306/0612/0508 IDC (InterDigitated Capacitors)

PHYSICAL DIMENSIONS AND PAD LAYOUT

PHYSICAL CHIP DIMENSIONS millimeters (inches)

Consult factory for additional requirements

PAD LAYOUT DIMENSIONS

IDC Low Inductance Capacitors (SnPb)

0306/0612/0508 IDC with Sn/Pb Termination

GENERAL DESCRIPTION

Inter-Digitated Capacitors (IDCs) are used for both semiconductor package and board level decoupling. The equivalent series inductance (ESL) of a single capacitor or an array of capacitors in parallel determines the response time of a Power Delivery Network (PDN). The lower the ESL of a PDN, the faster the response time. A designer can use many standard MLCCs in parallel to reduce ESL or a low ESL Inter-Digitated Capacitor (IDC) device. These IDC devices are available in versions with a maximum height of 0.95mm or 0.55mm.

IDCs are typically used on packages of semiconductor products with power levels of 15 watts or greater. Inter-Digitated Capacitors are used on CPU, GPU, ASIC, and ASSP devices produced on 0.13μ, 90nm, 65nm, and 45nm processes. IDC devices are used on both ceramic and organic package substrates. These low ESL surface mount capacitors can be placed on the bottom side or the top side of a package substrate. The low profile 0.55mm maximum height IDCs can easily be used on the bottom side of BGA packages or on the die side of packages under a heat spreader.

IDCs are used for board level decoupling of systems with speeds of 300MHz or greater. Low ESL IDCs free up valuable board space by reducing the number of capacitors required versus standard MLCCs. There are additional benefits to reducing the number of capacitors beyond saving board space including higher reliability from a reduction in the number of components and lower placement costs based on the need for fewer capacitors.

The Inter-Digitated Capacitor (IDC) technology was developed by AVX. This is the second family of Low Inductance MLCC products created by AVX. IDCs are a cost effective alternative to AVX's first generation low ESL family for high-reliability applications known as LICA (Low Inductance Chip Array).

AVX IDC products are available with a lead termination for high reliability military and aerospace applications that must avoid tin whisker reliability issues.

HOW TO ORDER

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

PERFORMANCE CHARACTERISTICS

TYPICAL IMPEDANCE

0306

0612

+ – + –

+ – + –

0508

IDC Low Inductance Capacitors (SnPb)

0306/0612/0508 IDC with Sn/Pb Termination

PHYSICAL DIMENSIONS AND PAD LAYOUT

PHYSICAL CHIP DIMENSIONS millimeters (inches)

Consult factory for additional requirements

PAD LAYOUT DIMENSIONS

LGA Low Inductance Capacitors

0204/0306 Land Grid Array

APPLICATIONS

Semiconductor Packages

- Microprocessors/CPUs
- Graphics Processors/GPUs
- Chipsets
- FPGAs
- ASICs

Land Grid Array (LGA) capacitors are the latest family of low inductance MLCCs from AVX. These new LGA products are the third low inductance family developed by AVX. The innovative LGA technology sets a new standard for low inductance MLCC performance.

Our initial 2 terminal versions of LGA technology deliver the performance of an 8 terminal IDC low inductance MLCC with a number of advantages including:

- Simplified layout of 2 large solder pads compared to 8 small pads for IDCs
- Opportunity to reduce PCB or substrate contribution to system ESL by using multiple parallel vias in solder pads
- Advanced FCT manufacturing process used to create uniformly flat terminations on the capacitor that resist "tombstoning"
- Better solder joint reliability

Board Level Device Decoupling

- Frequencies of 300 MHz or more
- ICs drawing 15W or more
- Low voltages
- High speed buses

0306 2 TERMINAL LGA COMPARISON WITH 0306 8 TERMINAL IDC

LGA Low Inductance Capacitors

0204/0306 Land Grid Array

PART DIMENSIONS mm (inches)

RECOMMENDED SOLDER PAD DIMENSIONS mm (inches)

PW1

PL

LGA Low Inductance Capacitors

0204/0306 Land Grid Array – Tin/Lead Termination "B"

PART DIMENSIONS mm (inches)

RECOMMENDED SOLDER PAD DIMENSIONS mm (inches)

PL

PW1

Present military specifications, as well as a majority of commercial applications, require a maximum operating temperature of 125°C. However, the emerging market for high temperature electronics demands capacitors operating reliably at temperatures beyond 125°C. AVX's high temperature chip capacitor product line, has been extended with the BME C0G chip. All AT chips have verified capabilities of long term operation up to 250°C for applications in both military and commercial businesses. These capacitors demonstrate high volumetric efficiency, high insulation resistance and low ESR/ESL for the most demanding applications, such as "down-hole" oil exploration and aerospace programs.

HOW TO ORDER

ELECTRICAL SPECIFICATIONS

Temperature Coefficient

PME C0G 0±30ppm/°C, -55C to 250°C BME C0G 0±30ppm/°C, -55C to 200°C See TCC Plot for +250°C

VHT: T ±15%, -55°C to +150°C See TCC Plot for +250°C

Capacitance Test (MIL-STD-202, Method 305) 25°C, 1.0 \pm 0.2 Vrms (open circuit voltage) @ 1kHz

Dissipation factor 25°C

C0G: 0.15% Max at 1.0 ± 0.2 Vrms (open circuit voltage) @ 1kHz VHT: 2.5% Max at 1.0 ± 0.2 Vrms (open circuit voltage) @ 1kHz

Insulation Resistance 25°C (MIL-STD-202, Method 302) 100GΩ or 1000MΩ-μF (whichever is less)

Insulation Resistance 125°C (MIL-STD-202, Method 302) 10GΩ or 100MΩ-μF (whichever is less)

Insulation Resistance 200°C (MIL-STD-202, Method 302) 1GΩ or 10MΩ-μF (whichever is less)

Insulation Resistance 250°C (MIL-STD-202, Method 302) 100MΩ or 1MΩ-μF (whichever is less)

Direct Withstanding Voltage 25°C (Flash Test) 250% rated voltage for 5 seconds with 50mA max charging current

DIMENSIONS millimeters (inches)

AT Series

High Temperature MLCC – 200ºC & 250°C Rated

PERFORMANCE CHARACTERISTICS

Typical Temperature Coefficient of Capacitance (VHT Dielectric) Typical Temperature Coefficient of Capacitance (C0G Dielectric)

Typical RC vs Temperature (VHT Dielectric) Typical RC vs Temperature (C0G Dielectric)

Typical Voltage Coefficient of Capacitance (VHT Dielectric) Typical Voltage Coefficient of Capacitance (C0G Dielectric)

RELIABILITY

*Typical 1210, 1812, 2225 Failure Rate Analysis based on 250°C testing and voltage ratings specified on the following page.

FREQUENCY RESPONSE

*Typical 1812 and 2225 Failure Rate Analysis based on 250°C testing and voltage ratings specified on the following page.

Impedance Frequency Response (C0G Dielectric)

ESR Frequency Response (C0G Dielectric)

PREFERRED SIZES ARE SHADED CAPACITANCE RANGE

VHT Temp. Coefficient: 4 200ºC Rated

Voltage rating per table. Capacitance values specified at 25ºC, derate capacitance value based on TCC and VCC Plots on page 90. NOTE: Contact factory for non-specified capacitance values.

PREFERRED SIZES ARE SHADED CAPACITANCE RANGE

BME C0G Temp. Coefficient: 3 200ºC Rated

Voltage rating per table. Capacitance values specified at 25ºC, derate capacitance value based on TCC and VCC Plots on page 90.

NOTE: Contact factory for non-specified capacitance values.

PREFERRED SIZES ARE SHADED CAPACITANCE RANGE

PME C0G Temp. Coefficient: 2 200ºC Rated

Voltage rating per table. Capacitance values specified at 25ºC, derate capacitance value based on TCC and VCC Plots on page 90. NOTE: Contact factory for non-specified capacitance values.

For 600V to 5000V Applications

NEW 630V RANGE

High value, low leakage and small size are difficult parameters to obtain in capacitors for high voltage systems. AVX special high voltage MLC chip capacitors meet these performance characteristics and are designed for applications such as snubbers in high frequency power converters, resonators in SMPS, and high voltage coupling/dc blocking. These high voltage chip designs exhibit low ESRs at high frequencies.

Larger physical sizes than normally encountered chips are used to make high voltage MLC chip products. Special precautions must be taken in applying these chips in surface mount assemblies. The temperature gradient during heating or cooling cycles should not exceed 4ºC per second. The preheat temperature must be within 50ºC of the peak temperature reached by the ceramic bodies through the soldering process. Chip sizes 1210 and larger should be reflow soldered only. Capacitors may require protective surface coating to prevent external arcing.

For 1825, 2225 and 3640 sizes, AVX offers leaded version in either thru-hole or SMT configurations (for details see section on high voltage leaded MLC chips).

HOW TO ORDER

Notes: Capacitors with X7R dielectrics are not intended for applications across AC supply mains or AC line filtering with polarity reversal. Contact plant for recommendations. Contact factory for availability of Termination and Tolerance options for Specific Part Numbers.

****** The 3640 Style is not available on 7" Reels.

******* AVX offers nonstandard chip sizes. Contact factory for details.

DIMENSIONS millimeters (inches)

*Reflow Soldering Only

For 600V to 5000V Applications

NP0 (C0G) Dielectric

Performance Characteristics

NP0 (C0G) CAPACITANCE RANGE – PREFERRED SIZES ARE SHADED

For 600V to 5000V Applications

NP0 (C0G) CAPACITANCE RANGE – PREFERRED SIZES ARE SHADED

For 600V to 5000V Applications

X7R Dielectric

Performance Characteristics

X7R CAPACITANCE RANGE – PREFERRED SIZES ARE SHADED

Max. 0.813 1.448 1.8034 2.2098 2.794 0.940 3.30 **Thickness** (0.032) (0.057) (0.071) (0.087) (0.110) (0.037) (0.130)

For 600V to 5000V Applications

X7R CAPACITANCE RANGE PREFERRED SIZES ARE SHADED

High Voltage MLC Chips Tin/Lead Termination "B"

For 600V to 5000V Applications

NEW 630V RANGE

AVX Corporation will support those customers for commercial and military Multilayer Ceramic Capacitors with a termination consisting of 5% minimum lead. This termination is indicated by the use of a "B" in the 12th position of the AVX Catalog Part Number. This fulfills AVX's commitment to providing a full range of products to our customers. AVX has provided in the following pages, a full range of values that we are offering in this "B" termination.

Larger physical sizes than normally encountered chips are used to make high voltage MLC chip product. Special precautions must be taken in applying these chips in surface mount assemblies. The temperature gradient during heating or cooling cycles should not exceed 4ºC per second. The preheat temperature must be within 50ºC of the peak temperature reached by the ceramic bodies through the soldering process. Chip sizes 1210 and larger should be reflow soldered only. Capacitors may require protective surface coating to prevent external arcing.

For 1825, 2225 and 3640 sizes, AVX offers leaded version in either thru-hole or SMT configurations (for details see section on high voltage leaded MLC chips).

HOW TO ORDER

Notes: Capacitors with X7R dielectrics are not intended for applications across AC supply mains or AC line filtering with polarity reversal. Contact plant for recommendations. Contact factory for availability of Termination and Tolerance options for Specific Part Numbers.

- ***** FLEXITERM is not available in the LD40 Style
- ****** The LD40 Style is not available on 7" Reels.
- *** AVX offers nonstandard chip sizes. Contact factory for details.

Not RoHS Compliant

DIMENSIONS millimeters (inches)

* Reflow soldering only.

Performance of SMPS capacitors can be simulated by downloading SpiCalci software program - http://www.avx.com/SpiApps/default.asp#spicalci Custom values, ratings and configurations are also available.

High Voltage MLC Chips Tin/Lead Termination "B"

For 600V to 5000V Applications

C0G Dielectric

Performance Characteristics

HIGH VOLTAGE C0G CAPACITANCE VALUES

X7R Dielectric Performance Characteristics

HIGH VOLTAGE X7R MAXIMUM CAPACITANCE VALUES

High Voltage MLC Chips FLEXITERM®

For 600V to 5000V Applications

High value, low leakage and small size are difficult parameters to obtain in capacitors for high voltage systems. AVX special high voltage MLC chips capacitors meet these performance characteristics and are designed for applications such as snubbers in high frequency power converters, resonators in SMPS, and high voltage coupling/DC blocking. These high voltage chip designs exhibit low ESRs at high frequencies.

To make high voltage chips, larger physical sizes than are normally encountered are necessary. These larger sizes require that special precautions be taken in applying these chips in surface mount assemblies. In response to this, and to follow from the success of the FLEXITERM® range of low voltage parts, AVX is delighted to offer a FLEXITERM® high voltage range of capacitors, FLEXITERM®.

The FLEXITERM® layer is designed to enhance the mechanical flexure and temperature cycling performance of a standard ceramic capacitor, giving customers a solution where board flexure or temperature cycle damage are concerns.

HOW TO ORDER

Notes: Capacitors with X7R dielectrics are not intended for applications across AC supply mains or AC line filtering with polarity reversal. Contact plant for recommendations. Contact factory for availability of Termination and Tolerance options for Specific Part Numbers.

*** AVX offers nonstandard chip sizes. Contact factory for details.

*Reflow Soldering Only

Performance of SMPS capacitors can be simulated by downloading SpiCalci software program - http://www.avx.com/SpiApps/default.asp#spicalci Custom values, ratings and configurations are also available.

High Voltage MLC Chips FLEXITERM®

For 600V to 5000V Applications

NP0 (C0G) Dielectric

Performance Characteristics

NP0 (C0G) CAPACITANCE RANGE PREFERRED SIZES ARE SHADED

High Voltage MLC Chips FLEXITERM® **For 600V to 5000V Applications**

X7R CAPACITANCE RANGE PREFERRED SIZES ARE SHADED

Letter | A | C | E | F | G | X **Max.** 0.813 1.448 1.803 2.210 2.794 0.940 **Thickness** (0.032) (0.057) (0.071) (0.087) (0.110) (0.037) NOTE: Contact factory for non-specified capacitance

High Voltage MLC Chips FLEXITERM®

For 600V to 5000V Applications

X7R Dielectric

Performance Characteristics

X7R CAPACITANCE RANGE PREFERRED SIZES ARE SHADED

High Voltage MLC Chips FLEXITERM®

For 600V to 5000V Applications

X7R CAPACITANCE RANGE PREFERRED SIZES ARE SHADED

nacitance values

High Voltage MLC Chip Capacitors For 600V to 3000V Automotive Applications - AEC-Q200

HOW TO ORDER

Modern automotive electronics could require components capable to work with high voltage (e.g. xenon lamp circuits or power converters in hybrid cards). AVX offers high voltage ceramic capacitors qualified according to AEC-Q200 standard.

High value, low leakage and small size are diffocult parameters to obtain in cpacitors for high voltage systems. AVX special hgih voltage MLC chip capacitors meet these performance characteristics and are designed for applications such as snubbers in high frequency power converters, resonators in SMPS, and high voltage coupling/dc blocking. These high voltage chip designs exhibit low ESRs at high frequencies.

Due to high voltage nature, larger physical dimensions are necessary. These larger sizes require special precautions to be taken in applying of MLC chips. The temperature gradient during heating or cooling cycles should not exceed 4°C per second. The preheat temperature must be within 50°C of the peak temperature reached by the ceramic bodies through the soldering process. Chip sizes 1210 and larger should be reflow soldered only. Capacitors may require protective surface coating to prevent external arcing.

To improve mechanical and thermal resistance, AVX recommend to use flexible terminations system - FLEXITERM®.

Notes: Capacitors with X7R dielectrics are not indeded for applications across AC supply mains or AC line filtering with polarity reversal. Please contact AVX for recommendations

CHIP DIMENSIONS DESCRIPTION (See capacitance range chart on page 109)

 $L =$ Length $W = W$ idth T = Thickness t = Terminal

X7R DIELECTRIC PERFORMANCE CHARACTERISTICS

High Voltage MLC Chips FLEXITERM® **For 600V to 3000V Automotive Applications – AEC-Q200**

X7R CAPACITANCE RANGE PREFERRED SIZES ARE SHADED

NOTE: Contact factory for non-specified capacitance values

MIL-PRF-55681/Chips Part Number Example CDR01 thru CDR06

MILITARY DESIGNATION PER MIL-PRF-55681

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

MIL Style: CDR01, CDR02, CDR03, CDR04, CDR05, CDR06

Voltage Temperature Limits:

- $BP = 0 \pm 30$ ppm/°C without voltage; 0 ± 30 ppm/°C with rated voltage from -55°C to +125°C
- $BX = ±15%$ without voltage; $+15 25%$ with rated voltage from -55° C to $+125^{\circ}$ C

Capacitance: Two digit figures followed by multiplier (number of zeros to be added) e.g., $101 = 100$ pF

Rated Voltage: $A = 50V$, $B = 100V$

Capacitance Tolerance: $J \pm 5\%$, $K \pm 10\%$, $M \pm 20\%$

Not RoHS Compliant

Termination Finish:

- M = Palladium silver
- N = Silver-nickel-gold
- S = Solder coated final with a minimum of 4 percent lead
- $T =$ Silver
- U = Base metallization-barrier metal-solder coated (tin/lead alloy, with a minimum of 4 percent lead)
- W = Base metallization-barrier metal-tinned (tin or tin/lead alloy)
- Y = Base metallization-barrier metal-tin (100 percent)
- $Z =$ Base metallization-barrier metal-tinned (tin/lead alloy, with a minimum of 4 percent lead)

*See MIL-PRF-55681 Specification for more details

Failure Rate Level: $M = 1.0\%$, $P = .1\%$, $R = .01\%$, $S = .001\%$

Packaging: Bulk is standard packaging. Tape and reel per RS481 is available upon request.

CROSS REFERENCE: AVX/MIL-PRF-55681/CDR01 THRU CDR06*

*For CDR11, 12, 13, and 14 see AVX Microwave Chip Capacitor Catalog

MIL-PRF-55681/Chips Military Part Number Identification CDR01 thru CDR06

Add appropriate failure rate

Add appropriate termination finish

- Capacitance Tolerance

MIL-PRF-55681/Chips Part Number Example CDR31 thru CDR35

MILITARY DESIGNATION PER MIL-PRF-55681

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

MIL Style: CDR31, CDR32, CDR33, CDR34, CDR35

Voltage Temperature Limits:

- $BP = 0 \pm 30$ ppm/°C without voltage; 0 ± 30 ppm/°C with rated voltage from -55°C to +125°C
- $BX = ±15%$ without voltage; $+15 -25%$ with rated voltage from -55° C to $+125^{\circ}$ C

Capacitance: Two digit figures followed by multiplier (number of zeros to be added) e.g., $101 = 100$ pF

Rated Voltage: $A = 50V$, $B = 100V$

Capacitance Tolerance: $B \pm .10$ pF, $C \pm .25$ pF, $D \pm .5$ pF, $F \pm 1\%$, $J \pm 5\%$, $K \pm 10\%$, $M \pm 20\%$

Not RoHS Compliant

Termination Finish: Termination Finish:

- M = Palladium silver
- N = Silver-nickel-gold
- S = Solder coated final with a minimum of 4 percent lead $T =$ Silver
- U = Base metallization-barrier metal-solder coated (tin/lead alloy, with a minimum of 4 percent lead)
- W = Base metallization-barrier metal-tinned (tin or tin/lead alloy)
- Y = Base metallization-barrier metal-tin (100 percent)
- $Z =$ Base metallization-barrier metal-tinned (tin/lead alloy, with a minimum of 4 percent lead)

*See MIL-PRF-55681 Specification for more details

Failure Rate Level: $M = 1.0\%$, $P = .1\%$, $R = .01\%$, $S = .001\%$

Packaging: Bulk is standard packaging. Tape and reel per RS481 is available upon request.

CROSS REFERENCE: AVX/MIL-PRF-55681/CDR31 THRU CDR35

MIL-PRF-55681/Chips

Military Part Number Identification CDR31

Add appropriate failure rate

Add appropriate termination finish

Capacitance Tolerance

1/ The complete part number will include additional symbols to indicate capacitance tolerance, termination and failure rate level.

Capacitance Tolerance

MIL-PRF-55681/Chips

Military Part Number Identification CDR32

Add appropriate failure rate

Add appropriate termination finish

Capacitance Tolerance

 $1/$ The complete part number will include additional symbols to indicate capacitance tolerance, termination and failure rate level. Add appropriate termination finish Capacitance Tolerance

Add appropriate failure rate

MIL-PRF-55681/Chips

Military Part Number Identification CDR33/34/35

- Add appropriate termination finish

Capacitance Tolerance

1/ The complete part number will include additional symbols to indicate capacitance tolerance, termination and failure rate level.

Add appropriate termination finish

ANAK

MQ Series – Medical Grade MLCC

General Specifications

GENERAL DESCRIPTION

AVX offers a wide variety of medically qualified passive components. Medical devices require the utmost reliability with respect to the components incorporated into the designs. Advanced design qualification requirements, in-process controls and requirements and lot acceptance testing are implemented to ensure these components will meet the superior reliability levels of a life supporting application. AVX medical MLCC reliability documents provide an advanced level of designing, manufacturing, testing and qualification that places AVX as the top supplier and industry leader of medically qualified MLCCs.

AVX MQ series of medically qualified ceramic capacitors are available in EIA case sizes ranging from 0402 to 2225, at typical voltage ratings between 4 – 200 Vdc with various termination options including Sn, SnPb solder, and Au.

APPLICATIONS

- Implantable cardioverter-defibrillator (ICD)
- Pacemakers
- Neuromodulation

FEATURES

- 0402 to 2225 case sizes
- Voltage range from 4v to 100v
- Capacitance up to 100μF
- Class I & II dielectric materials
- Tight tolerances on Class I dielectric materials
- Various terminations
- Customer specific requirements, screening, & testing

HOW TO ORDER

8.2pF = 8R2

MQ Series – Medical Grade MLCC NP0 (C0G) – Capacitance & Voltage Range

PREFERRED SIZES ARE SHADED

116

MQ Series – Medical Grade MLCC

NP0 (C0G) – General Specifications

TYPICAL ELECTRICAL CHARACTERISTICS

Variation of Impedance with Ceramic Formulation Impedance vs. Frequency 1000 pF - C0G (NP0) vs. X7R

Insulation Resistance vs Temperature Insulation Resistance vs. Temperature

 \blacksquare ⁰⁵⁰⁵¹⁶ 117

MQ Series – Medical Grade MLCC

NP0 (C0G) – Specifications & Test Methods

PREFERRED SIZES ARE SHADED

MQ Series – Medical Grade MLCC

X7R/X7S – General Specifications

TYPICAL ELECTRICAL CHARACTERISTICS

Insulation Resistance vs. Temperature I. Insulation Resistance (Ohm-Farads) 10,000 1,000 100 $0₀$ 20 40 60 80 100 120 Temperature C

AVAK

MQ Series – Medical Grade MLCC

X7R/X7S – Specifications & Test Methods

MQ Series – Medical Grade MLCC X5R – Capacitance & Voltage Range

PREFERRED SIZES ARE SHADED

TYPICAL ELECTRICAL CHARACTERISTICS

Insulation Resistance vs. Temperature

MQ Series – Medical Grade MLCC

X5R – Specifications & Test Methods

General Specifications

The AVX MM series is a multi-layer ceramic capacitor designed for use in medical applications other than implantable/life support. These components have the design & change control expected for medical devices and also offer enhanced LAT including reliability testing and 100% inspection.

T

(X7R only)

APPLICATIONS

Implantable, Non-Life Supporting Medical Devices

• e.g. implanted temporary cardiac monitor, insulin pumps

- **External, Life Supporting Medical Devices**
- e.g. heart pump external controller

External Devices

• e.g. patient monitoring, diagnostic equipment

MAD HOW TO ORDER

100

J

C

2

Special Code A = Standard

A

*Contact AVX for others

COMMERCIAL VS MM SERIES PROCESS COMPARISON

NP0 (C0G) – Specifications & Test Methods

NP0/C0G Capacitance Range

PREFERRED SIZES ARE SHADED

X7R Specifications and Test Methods

X7R Capacitance Range

PREFERRED SIZES ARE SHADED

Packaging of Chip Components

Automatic Insertion Packaging

TAPE & REEL QUANTITIES

All tape and reel specifications are in compliance with RS481.

REEL DIMENSIONS

Metric dimensions will govern.

English measurements rounded and for reference only.

(1) For tape sizes 16mm and 24mm (used with chip size 3640) consult EIA RS-481 latest revision.

Embossed Carrier Configuration

4, 8 & 12mm Tape Only

4, 8 & 12mm Embossed Tape Metric Dimensions Will Govern

CONSTANT DIMENSIONS

VARIABLE DIMENSIONS

NOTES:

1. The cavity defined by A_0 , B_0 , and K_0 shall be configured to provide the following:

Surround the component with sufficient clearance such that:

a) the component does not protrude beyond the sealing plane of the cover tape. b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the cover tape has been removed.

c) rotation of the component is limited to 20º maximum (see Sketches D & E).

d) lateral movement of the component is restricted to 0.5mm maximum (see Sketch F).

2. Tape with or without components shall pass around radius "R" without damage.

3. Bar code labeling (if required) shall be on the side of the reel opposite the round sprocket holes. Refer to EIA-556.

4. B₁ dimension is a reference dimension for tape feeder clearance only.

5. If $P_1 = 2.0$ mm, the tape may not properly index in all tape feeders.

Maximum Component Rotation

Paper Carrier Configuration

8 & 12mm Tape Only

8 & 12mm Paper Tape Metric Dimensions Will Govern

CONSTANT DIMENSIONS

VARIABLE DIMENSIONS

NOTES:

- 1. The cavity defined by A_0 , B_0 , and T shall be configured to provide sufficient clearance surrounding the component so that:
	- a) the component does not protrude beyond either surface of the carrier tape; b) the component can be removed from the cavity in a vertical direction without
	- mechanical restriction after the top cover tape has been removed; c) rotation of the component is limited to 20º maximum (see Sketches A & B);
	- d) lateral movement of the component is restricted to 0.5mm maximum (see Sketch C).

Bar Code Labeling Standard

AVX bar code labeling is available and follows latest version of EIA-556

2. Tape with or without components shall pass around radius "R" without damage.

3. Bar code labeling (if required) shall be on the side of the reel opposite the sprocket holes. Refer to EIA-556.

4. If $P_1 = 2.0$ mm, the tape may not properly index in all tape feeders.

Top View
Sketch "B"

Basic Capacitor Formulas

I. Capacitance (farads)

English: $C = \frac{.224 \text{ K A}}{}$ T_{D} Metric: $C = 0.0884$ K A T_{\odot}

- **II. Energy stored in capacitors (Joules, watt sec)** $E = \frac{1}{2}CV^2$
- **III. Linear charge of a capacitor (Amperes)**

$$
I = C \frac{dV}{dt}
$$

- **IV. Total Impedance of a capacitor (ohms)** $Z = \sqrt{R_S^2 + (X_C - X_L)^2}$
- **V. Capacitive Reactance (ohms)**

$$
x_C = \frac{1}{2 \pi fC}
$$

VI. Inductive Reactance (ohms) $x_L = 2 \pi fL$

VII. Phase Angles:

Ideal Capacitors: Current leads voltage 90° Ideal Inductors: Current lags voltage 90° Ideal Resistors: Current in phase with voltage

VIII. Dissipation Factor (%)

D.F.= tan δ (loss angle) = $\frac{E.S.R.}{E.S.R.}$ = (2 πfC) (E.S.R.) $X^{\vphantom{\dagger}}_{\rm C}$

IX. Power Factor (%) P.F. = Sine δ (loss angle) = Cos ϕ (phase angle) $P.F. =$ (when less than $10\%) = DF$

X. Quality Factor (dimensionless)

 $Q =$ Cotan δ (loss angle) = $\frac{1}{\sqrt{1-\frac{1}{\epsilon^2}}}$ D.F.

METRIC PREFIXES SYMBOLS

- **XI. Equivalent Series Resistance (ohms)** E.S.R. = (D.F.) (Xc) = (D.F.) / (2 π fC)
- **XII. Power Loss (watts)** Power Loss = $(2 \pi fCV^2)$ (D.F.)
- **XIII. KVA (Kilowatts)** KVA = 2π fCV² x 10⁻³

XIV. Temperature Characteristic (ppm/°C)

$$
T.C. = \frac{Ct - C_{25}}{C_{25} (T_t - 25)} \times 10^6
$$

XV. Cap Drift (%)
C.D. =
$$
\frac{C_1 - C_2}{C_1}
$$
 x 100

XVI. Reliability of Ceramic Capacitors

$$
\begin{array}{cc} L_{0} = \left(\frac{V_{t}}{V_{o}}\right)^{\times} & \left(\frac{T_{t}}{T_{o}}\right)^{\vee} \end{array}
$$

XVII. Capacitors in Series (current the same)

Any Number:
$$
\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} - \frac{1}{C_N}
$$

Two: $C_T = \frac{C_1 C_2}{C_1 + C_2}$

XVIII. Capacitors in Parallel (voltage the same) $C_T = C_1 + C_2 - \cdots + C_N$

XIX. Aging Rate

A.R. = $\% \Delta$ C/decade of time

XX. Decibels

$$
db = 20 \log \frac{V_1}{V_2}
$$

Basic Construction – A multilayer ceramic (MLC) capacitor is a monolithic block of ceramic containing two sets of offset, interleaved planar electrodes that extend to two opposite surfaces of the ceramic dielectric. This simple

structure requires a considerable amount of sophistication, both in material and manufacture, to produce it in the quality and quantities needed in today's electronic equipment.

Formulations – Multilayer ceramic capacitors are available in both Class 1 and Class 2 formulations. Temperature compensating formulation are Class 1 and temperature stable and general application formulations are classified as Class 2.

Class 1 – Class 1 capacitors or temperature compensating capacitors are usually made from mixtures of titanates where barium titanate is normally not a major part of the mix. They have predictable temperature coefficients and in general, do not have an aging characteristic. Thus they are the most stable capacitor available. The most popular Class 1 multilayer ceramic capacitors are C0G (NP0) temperature compensating capacitors (negative-positive 0 ppm/°C).

Class 2 – EIA Class 2 capacitors typically are based on the chemistry of barium titanate and provide a wide range of capacitance values and temperature stability. The most commonly used Class 2 dielectrics are X7R and Y5V. The X7R provides intermediate capacitance values which vary only ±15% over the temperature range of -55°C to 125°C. It finds applications where stability over a wide temperature range is required.

The Y5V provides the highest capacitance values and is used in applications where limited temperature changes are expected. The capacitance value for Y5V can vary from 22% to -82% over the -30°C to 85°C temperature range.

All Class 2 capacitors vary in capacitance value under the influence of temperature, operating voltage (both AC and DC), and frequency. For additional information on performance changes with operating conditions, consult AVX's software, SpiCap.

Table 1: EIA and MIL Temperature Stable and General Application Codes

increase no more than 7.5% or decrease no more than 7.5% from -30°C to +85°C. EIA Code will be Y5F. -30°C to +85°C. EIA Code will be Y5F.

In specifying capacitance change with temperature for Class 2 materials, EIA expresses the capacitance change over an operating temperature range by a 3 symbol code. The first symbol represents the cold temperature end of the temperature range, the second represents the upper limit of the operating temperature range and the third symbol represents the capacitance change allowed over the operating temperature range. Table 1 provides a detailed explanation of the EIA system.

Effects of Voltage – Variations in voltage have little effect on Class 1 dielectric but does affect the capacitance and dissipation factor of Class 2 dielectrics. The application of DC voltage reduces both the capacitance and dissipation factor while the application of an AC voltage within a reasonable range tends to increase both capacitance and dissipation |factor readings. If a high enough AC voltage is applied, eventually it will reduce capacitance just as a DC voltage will. Figure 2 shows the effects of AC voltage.

Figure 2

Capacitor specifications specify the AC voltage at which to measure (normally 0.5 or 1 VAC) and application of the wrong voltage can cause spurious readings. Figure 3 gives the voltage coefficient of dissipation factor for various AC voltages at 1 kilohertz. Applications of different frequencies will affect the percentage changes versus voltages.

D.F. vs. A.C. Measurement Volts

Typical effect of the application of DC voltage is shown in Figure 4. The voltage coefficient is more pronounced for higher K dielectrics. These figures are shown for room temperature conditions. The combination characteristic known as voltage temperature limits which shows the effects of rated voltage over the operating temperature range is shown in Figure 5 for the military BX characteristic.

Effects of Time – Class 2 ceramic capacitors change capacitance and dissipation factor with time as well as temperature, voltage and frequency. This change with time is known as aging. Aging is caused by a gradual re-alignment of the crystalline structure of the ceramic and produces an exponential loss in capacitance and decrease in dissipation factor versus time. A typical curve of aging rate for semistable ceramics is shown in Figure 6.

If a Class 2 ceramic capacitor that has been sitting on the shelf for a period of time, is heated above its curie point, (125°C for 4 hours or 150°C for ½ hour will suffice) the part will de-age and return to its initial capacitance and dissi-pation factor readings. Because the capacitance changes rapidly, immediately after de-aging, the basic capacitance measurements are normally referred to a time period sometime after the de-aging process. Various manufacturers use different time bases but the most popular one is one day or twenty-four hours after "last heat." Change in the aging curve can be caused by the application of voltage and other stresses. The possible changes in capacitance due to de-aging by heating the unit explain why capacitance changes are allowed after test, such as temperature cycling, moisture resistance, etc., in MIL specs. The application of high voltages such as dielectric withstanding voltages also tends to de-age

capacitors and is why re-reading of capacitance after 12 or 24 hours is allowed in military specifications after dielectric strength tests have been performed.

Effects of Frequency – Frequency affects capacitance and impedance characteristics of capacitors. This effect is much more pronounced in high dielectric constant ceramic formulation than in low K formulations. AVX's SpiCap software generates impedance, ESR, series inductance, series resonant frequency and capacitance all as functions of frequency, temperature and DC bias for standard chip sizes and styles. It is available free from AVX and can be downloaded for free from AVX website: www.avx.com.

Effects of Mechanical Stress – High "K" dielectric ceramic capacitors exhibit some low level piezoelectric reactions under mechanical stress. As a general statement, the piezoelectric output is higher, the higher the dielectric constant of the ceramic. It is desirable to investigate this effect before using high "K" dielectrics as coupling capacitors in extremely low level applications.

Reliability – Historically ceramic capacitors have been one of the most reliable types of capacitors in use today. The approximate formula for the reliability of a ceramic capacitor is:

$$
\frac{L_o}{L_t} = \left(\frac{V_t}{V_o}\right)^X \left(\frac{T_t}{T_o}\right)^Y
$$

where

 L_0 = operating life **T**_t = test temperature and L_t = test life **T**_o = operating temperature T_o = operating temperature in ${}^{\circ}C$ V_t = test voltage in °C
 V_o = operating voltage X, Y = see text **V_o** = operating voltage

Historically for ceramic capacitors exponent X has been considered as 3. The exponent Y for temperature effects typically tends to run about 8.

A capacitor is a component which is capable of storing electrical energy. It consists of two conductive plates (electrodes) separated by insulating material which is called the dielectric. A typical formula for determining capacitance is:

$$
C = \frac{.224 \text{ KA}}{t}
$$

- **C** = capacitance (picofarads)
- $K =$ dielectric constant (Vacuum = 1)
- $A =$ area in square inches
- **t** = separation between the plates in inches (thickness of dielectric)
- **.224** = conversion constant

(.0884 for metric system in cm)

Capacitance – The standard unit of capacitance is the farad. A capacitor has a capacitance of 1 farad when 1 coulomb charges it to 1 volt. One farad is a very large unit and most capacitors have values in the micro (10^{-6}) , nano (10^{-9}) or pico (10^{-12}) farad level.

Dielectric Constant – In the formula for capacitance given above the dielectric constant of a vacuum is arbitrarily chosen as the number 1. Dielectric constants of other materials are then compared to the dielectric constant of a vacuum.

Dielectric Thickness – Capacitance is indirectly proportional to the separation between electrodes. Lower voltage requirements mean thinner dielectrics and greater capacitance per volume.

Area – Capacitance is directly proportional to the area of the electrodes. Since the other variables in the equation are usually set by the performance desired, area is the easiest parameter to modify to obtain a specific capacitance within a material group.

Energy Stored – The energy which can be stored in a capacitor is given by the formula:

 $E = \frac{1}{2}CV^2$

 $E =$ energy in joules (watts-sec) **= applied voltage C** = capacitance in farads

Potential Change – A capacitor is a reactive component which reacts against a change in potential across it. This is shown by the equation for the linear charge of a capacitor:

$$
I_{\text{ideal}} = c \frac{dV}{dt}
$$

where

- $I =$ Current **C** = Capacitance
- **dV/dt** = Slope of voltage transition across capacitor

Thus an infinite current would be required to instantly change the potential across a capacitor. The amount of current a capacitor can "sink" is determined by the above equation.

Equivalent Circuit – A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic for the equivalent circuit is:

Reactance – Since the insulation resistance $(R₀)$ is normally very high, the total impedance of a capacitor is:

$$
Z = \sqrt{R_S^2 + (X_C - X_L)^2}
$$
 where

$$
Z = \text{Total Impedance}
$$
\n
$$
R_s = \text{Series Resistance}
$$
\n
$$
X_c = \text{Capacitive Reactance} = \frac{1}{2\pi}
$$

 $=$ $\frac{2 \pi}{6}$
= 2π fl X_i = Inductive Reactance

The variation of a capacitor's impedance with frequency determines its effectiveness in many applications.

Phase Angle – Power Factor and Dissipation Factor are often confused since they are both measures of the loss in a capacitor under AC application and are often almost identical in value. In a "perfect" capacitor the current in the capacitor will lead the voltage by 90°.

In practice the current leads the voltage by some other phase angle due to the series resistance R_s . The complement of this angle is called the loss angle and:

> Power Factor (P.F.) = Cos ϕ or Sine δ Dissipation Factor (D.F.) = tan δ

for small values of δ the tan and sine are essentially equal which has led to the common interchangeability of the two terms in the industry.

Equivalent Series Resistance – The term E.S.R. or Equivalent Series Resistance combines all losses both series and parallel in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection.

Dissipation Factor – The DF/PF of a capacitor tells what percent of the apparent power input will turn to heat in the capacitor.

$$
\text{Dissipation Factor} = \frac{\text{E.S.R.}}{X_{\text{C}}} = (2 \pi \text{ fC}) \text{ (E.S.R.)}
$$

The watts loss are:

Watts loss = $(2 \pi fCV^2)$ (D.F.)

Very low values of dissipation factor are expressed as their reciprocal for convenience. These are called the "Q" or Quality factor of capacitors.

Parasitic Inductance – The parasitic inductance of capacitors is becoming more and more important in the decoupling of today's high speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line can be seen from the simple inductance equation:

$$
V = L \frac{di}{dt}
$$

The $\frac{di}{dt}$ seen in current microprocessors can be as high as 0.3 A/ns, and up to 10A/ns. At 0.3 A/ns, 100pH of parasitic inductance can cause a voltage spike of 30mV. While this does not sound very drastic, with the Vcc for microprocessors decreasing at the current rate, this can be a fairly large percentage.

Another important, often overlooked, reason for knowing the parasitic inductance is the calculation of the resonant frequency. This can be important for high frequency, bypass capacitors, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation:

$$
f_{res} = \frac{1}{2\pi\sqrt{LC}}
$$

Insulation Resistance – Insulation Resistance is the resistance measured across the terminals of a capacitor and consists principally of the parallel resistance RP shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the I.R. decreases and hence the product (C x IR or RC) is often specified in ohm farads or more commonly megohm-microfarads. Leakage current is determined by dividing the rated voltage by IR (Ohm's Law).

Dielectric Strength – Dielectric Strength is an expression of the ability of a material to withstand an electrical stress. Although dielectric strength is ordinarily expressed in volts, it is actually dependent on the thickness of the dielectric and thus is also more generically a function of volts/mil.

Dielectric Absorption - A capacitor does not discharge instantaneously upon application of a short circuit, but drains gradually after the capacitance proper has been discharged. It is common practice to measure the dielectric absorption by determining the "reappearing voltage" which appears across a capacitor at some point in time after it has been fully discharged under short circuit conditions.

Corona – Corona is the ionization of air or other vapors which causes them to conduct current. It is especially prevalent in high voltage units but can occur with low voltages as well where high voltage gradients occur. The energy discharged degrades the performance of the capacitor and can in time cause catastrophic failures.

MLC Chip Capacitors

REFLOW SOLDERING

Component Pad Design

Component pads should be designed to achieve good solder filets and minimize component movement during reflow soldering. Pad designs are given below for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering. The basis of these designs is:

- Pad width equal to component width. It is permissible to decrease this to as low as 85% of component width but it is not advisable to go below this.
- Pad overlap 0.5mm beneath component.
- Pad extension 0.5mm beyond components for reflow and 1.0mm for wave soldering.

WAVE SOLDERING

Component Spacing

For wave soldering components, must be spaced sufficiently far apart to avoid bridging or shadowing (inability of solder to penetrate properly into small spaces). This is less important for reflow soldering but sufficient space must be allowed to enable rework should it be required.

Preheat & Soldering

The rate of preheat should not exceed 4°C/second to prevent thermal shock. A better maximum figure is about 2°C/second.

For capacitors size 1206 and below, with a maximum thickness of 1.25mm, it is generally permissible to allow a temperature differential from preheat to soldering of 150°C. In all other cases this differential should not exceed 100°C.

For further specific application or process advice, please consult AVX.

Cleaning

Care should be taken to ensure that the capacitors are thoroughly cleaned of flux residues especially the space beneath the capacitor. Such residues may otherwise become conductive and effectively offer a low resistance bypass to the capacitor.

Ultrasonic cleaning is permissible, the recommended conditions being 8 Watts/litre at 20-45 kHz, with a process cycle of 2 minutes vapor rinse, 2 minutes immersion in the ultrasonic solvent bath and finally 2 minutes vapor rinse.

Recommended Soldering Profiles

REFLOW SOLDER PROFILES

AVX RoHS compliant products utilize termination finishes (e.g.Sn or SnAg) that are compatible with all Pb-Free soldering systems and are fully reverse compatible with SnPb soldering systems. A recommended SnPb profile is shown for comparison; for Pb-Free soldering, IPC/JEDECJ-STD-020C may be referenced. The upper line in the chart shows the maximum envelope to which products are qualified (typically 3x reflow cycles at 260ºC max). The center line gives the recommended profile for optimum wettability and soldering in Pb-Free Systems.

Preheat:

The pre-heat stabilizes the part and reduces the temperature differential prior to reflow. The initial ramp to 125ºC may be rapid, but from that point (2-3)ºC/sec is recommended to allow ceramic parts to heat uniformly and plastic encapsulated parts to stabilize through the glass transition temperature of the body $($ \sim 180 $^{\circ}$ C $)$.

Reflow:

In the reflow phase, the maximum recommended time > 230ºC is 40secs. Time at peak reflow is 10secs max.; optimum reflow is achieved at 250ºC, (see wetting balance chart opposite) but products are qualified to 260ºC max. Please reference individual product datasheets for maximum limits

Cool Down:

Cool down should not be forced and 6ºC/sec is recommended. A slow cool down will result in a finer grain structure of the reflow solder in the solder fillet.

WAVE SOLDER PROFILES

For wave solder, there is no change in the recommended wave profile; all standard Pb-Free (SnCu/SnCuAg) systems operate at the same 260ºC max recommended for SnPb systems.

Preheat:

This is more important for wave solder; a higher temperature preheat will reduce the thermal shock to SMD parts that are immersed (please consult individual product data sheets for SMD parts that are suited to wave solder). SMD parts should ideally be heated from the bottom-Side prior to wave. PTH (Pin through hole) parts on the topside should not be separately heated.

Wave:

250ºC – 260ºC recommended for optimum solderability.

Cool Down:

As with reflow solder, cool down should not be forced and 6ºC/sec is recommended. Any air knives at the end of the 2nd wave should be heated.

IMPORTANT NOTE: Typical Pb-Free reflow solders have a more dull and grainy appearance compared to traditional SnPb. Elevating the reflow temperature will not change this, but extending the cool down can help improve the visual appearance of the joint.

MLC Chip Capacitors

APPLICATION NOTES

Storage

The components should be stored in their "as received packaging" where possible. If the components are removed from their original packaging then they should be stored in an airtight container (e.g. a heat sealed plastic bag) with desiccant (e.g. silica gel). Storage area temperature should be kept between +5 degrees C and +30 degrees C with humidity < 70% RH. Storage atmosphere must be free of gas containing sulfur and chlorine. Avoid exposing the product to saline moisture or to temperature changes that might result in the formation of condensation. To assure good solderability performance we recommend that the product be used within 6 months from our shipping date, but can be used for up to 12 months. Chip capacitors may crack if exposed to hydrogen (H2) gas while sealed or if coated with silicon, which generates hydrogen gas.

Solderability

Terminations to be well soldered after immersion in a 60/40 tin/lead solder bath at $235 \pm 5^{\circ}$ C for 2 ± 1 seconds.

Leaching

Terminations will resist leaching for at least the immersion times and conditions shown below.

Lead-Free Wave Soldering

The recommended peak temperature for lead-free wave soldering is 250°C-260°C for 3-5 seconds. The other parameters of the profile remains the same as above.

The following should be noted by customers changing from lead based systems to the new lead free pastes.

- a) The visual standards used for evaluation of solder joints will need to be modified as lead free joints are not as bright as with tin-lead pastes and the fillet may not be as large.
- b) Lead-free solder pastes do not allow the same self alignment as lead containing systems. Standard mounting pads are acceptable, but machine set up may need to be modified.

General

Surface mounting chip multilayer ceramic capacitors are designed for soldering to printed circuit boards or other substrates. The construction of the components is such that they will withstand the time/temperature profiles used in both wave and reflow soldering methods.

Handling

Chip multilayer ceramic capacitors should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of tweezers or vacuum pick ups is strongly recommended for individual components. Bulk handling should ensure that abrasion and mechanical shock are minimized. Taped and reeled components provides the ideal medium for direct presentation to the placement machine. Any mechanical shock should be minimized during handling chip multilayer ceramic capacitors.

Preheat

It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4°C/second and a target figure 2°C/second is recommended. Although an 80°C to 120°C temperature differential is preferred, recent developments allow a temperature differential between the component surface and the soldering temperature of 150°C (Maximum) for capacitors of 1210 size and below with a maximum thickness of 1.25mm. The user is cautioned that the risk of thermal shock increases as chip size or temperature differential increases.

Soldering

Mildly activated rosin fluxes are preferred. The minimum amount of solder to give a good joint should be used. Excessive solder can lead to damage from the stresses caused by the difference in coefficients of expansion between solder, chip and substrate. AVX terminations are suitable for all wave and reflow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.

Cooling

Natural cooling in air is preferred, as this minimizes stresses within the soldered joint. When forced air cooling is used, cooling rate should not exceed 4°C/second. Quenching is not recommended but if used, maximum temperature differentials should be observed according to the preheat conditions above.

Cleaning

Flux residues may be hygroscopic or acidic and must be removed. AVX MLC capacitors are acceptable for use with all of the solvents described in the specifications MIL-STD-202 and EIA-RS-198. Alcohol based solvents are acceptable and properly controlled water cleaning systems are also acceptable. Many other solvents have been proven successful, and most solvents that are acceptable to other components on circuit assemblies are equally acceptable for use with ceramic capacitors.

Prevention of Metallic Migration

Note that when components with Sn plating on the end terminations are to be used in applications that are likely to experience conditions of high humidity under bias voltage, we strongly recommend that the circuit boards be conformally coated to protect the Sn from moisture that might lead to migration and eventual current leakage.

When using Capacitor Arrays we recommend that there is no differential in applied voltage between adjacent elements.

MLC Chip Capacitors

POST SOLDER HANDLING

Once SMP components are soldered to the board, any bending or flexure of the PCB applies stresses to the soldered joints of the components. For leaded devices, the stresses are absorbed by the compliancy of the metal leads and generally don't result in problems unless the stress is large enough to fracture the soldered connection.

Ceramic capacitors are more susceptible to such stress because they don't have compliant leads and are brittle in nature. The most frequent failure mode is low DC resistance or short circuit. The second failure mode is significant loss of capacitance due to severing of contact between sets of the internal electrodes.

Cracks caused by mechanical flexure are very easily identified and generally take one of the following two general forms:

Mechanical cracks are often hidden underneath the termination and are difficult to see externally. However, if one end termination falls off during the removal process from PCB, this is one indication that the cause of failure was excessive mechanical stress due to board warping.

Type A:
Angled crack between bottom of device to top of solder joint. Angled crack between bottom of device to top of solder joint.

The Bigger B Fracture from top of device to bottom of device.

MLC Chip Capacitors

COMMON CAUSES OF MECHANICAL CRACKING

The most common source for mechanical stress is board depanelization equipment, such as manual breakapart, vcutters and shear presses. Improperly aligned or dull cutters may cause torqueing of the PCB resulting in flex stresses being transmitted to components near the board edge. Another common source of flexural stress is contact during parametric testing when test points are probed. If the PCB is allowed to flex during the test cycle, nearby ceramic capacitors may be broken.

A third common source is board to board connections at vertical connectors where cables or other PCBs are connected to the PCB. If the board is not supported during the plug/unplug cycle, it may flex and cause damage to nearby components.

Special care should also be taken when handling large (>6" on a side) PCBs since they more easily flex or warp than smaller boards.

REWORKING OF MLCS

Thermal shock is common in MLCs that are manually attached or reworked with a soldering iron. AVX strongly recommends that any reworking of MLCs be done with hot air reflow rather than soldering irons. It is practically impossible to cause any thermal shock in ceramic capacitors when using hot air reflow.

However direct contact by the soldering iron tip often causes thermal cracks that may fail at a later date. If rework by soldering iron is absolutely necessary, it is recommended that the wattage of the iron be less than 30 watts and the tip temperature be <300ºC. Rework should be performed by applying the solder iron tip to the pad and not directly contacting any part of the ceramic capacitor.

PCB BOARD DESIGN

To avoid many of the handling problems, AVX recommends that MLCs be located at least .2" away from nearest edge of board. However when this is not possible, AVX recommends that the panel be routed along the cut line, adjacent to where the MLC is located.

NORTH AMERICA

SOUTH AMERICA Tel: +55 11-46881960 Tel: +81 740-321250

EUROPE Tel: 864-967-2150 Tel: +44 1276-697000 Tel: +65 6286-7555

ASIA

JAPAN

Contact:

http://www.avx.com

