# BT149 series

## Thyristors logic level

Rev. 5 — 1 November 2011 Product data sheet

## 1. Product profile

### 1.1 General description

Passivated, sensitive gate thyristors in a SOT54 plastic package.

### 1.2 Features and benefits

- Designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

### 1.3 Applications

- General purpose switching and phase control.

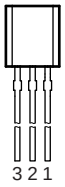
### 1.4 Quick reference data

- $V_{DRM}$, $V_{RRM} \leq 200$ V (BT149B)
- $V_{DRM}$, $V_{RRM} \leq 400$ V (BT149D)
- $V_{DRM}$, $V_{RRM} \leq 600$ V (BT149G)
- $I_{T(RMS)} \leq 0.8$ A
- $I_{T(AV)} \leq 0.5$ A
- $I_{TSM} \leq 8$ A.

## 2. Pinning information

**Table 1. Discrete pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | cathode (K) | | |
| 2 | gate (G) | | |
| 3 | anode (A) | | |




**SOT54 (TO-92)**

## 3. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BT149B | - | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |
| BT149D | | | |
| BT149G | | | |

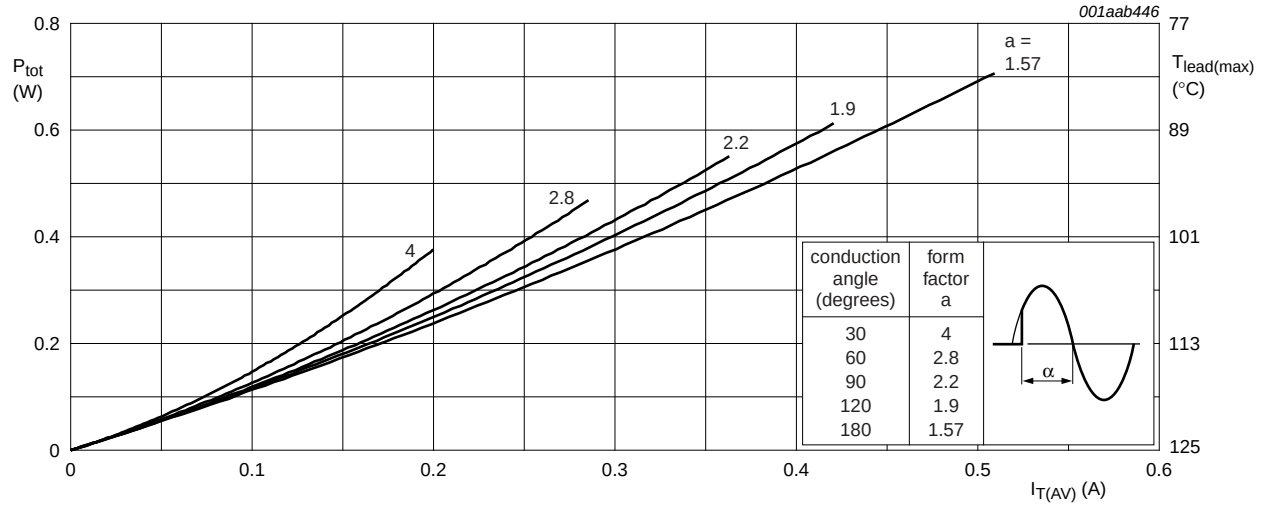
## 4. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

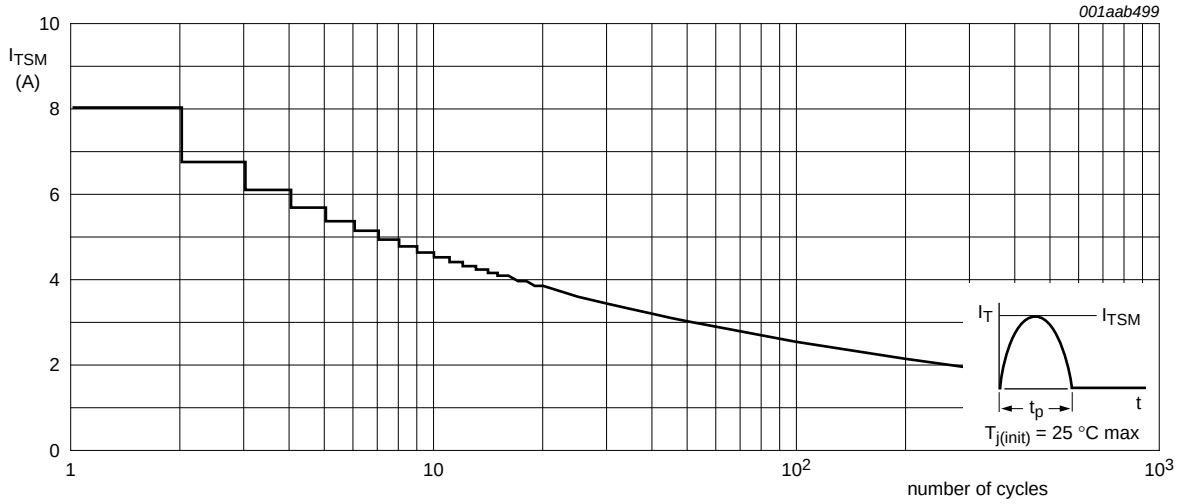
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$, $V_{RRM}$ | repetitive peak off-state voltage | | | | | |
| | BT149B | | [1] | - | 200 | V |
| | BT149D | | [1] | - | 400 | V |
| | BT149G | | [1] | - | 600 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_{lead} \leq 83$ °C; see Figure 1 | | - | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | all conduction angles; see Figure 4 and 5 | | - | 0.8 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | half sine wave; $T_j$ = 25 °C prior to surge; see Figure 2 and 3 | | | | |
| | | t = 10 ms | | - | 8 | A |
| | | t = 8.3 ms | | - | 9 | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | | - | 0.32 | $A^2s$ |
| $dI_T/dt$ | repetitive rate of rise of on-state current after triggering | $I_{TM}$ = 2 A; $I_G$ = 10 mA; $dI_G/dt$ = 100 mA/µs | | - | 50 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 1 | A |
| $V_{GM}$ | peak gate voltage | | | - | 5 | V |
| $V_{RGM}$ | peak reverse gate voltage | | | - | 5 | V |
| $P_{GM}$ | peak gate power | | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.1 | W |
| $T_{stg}$ | storage temperature | | | –40 | +150 | °C |
| $T_j$ | junction temperature | | | - | 125 | °C |

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.



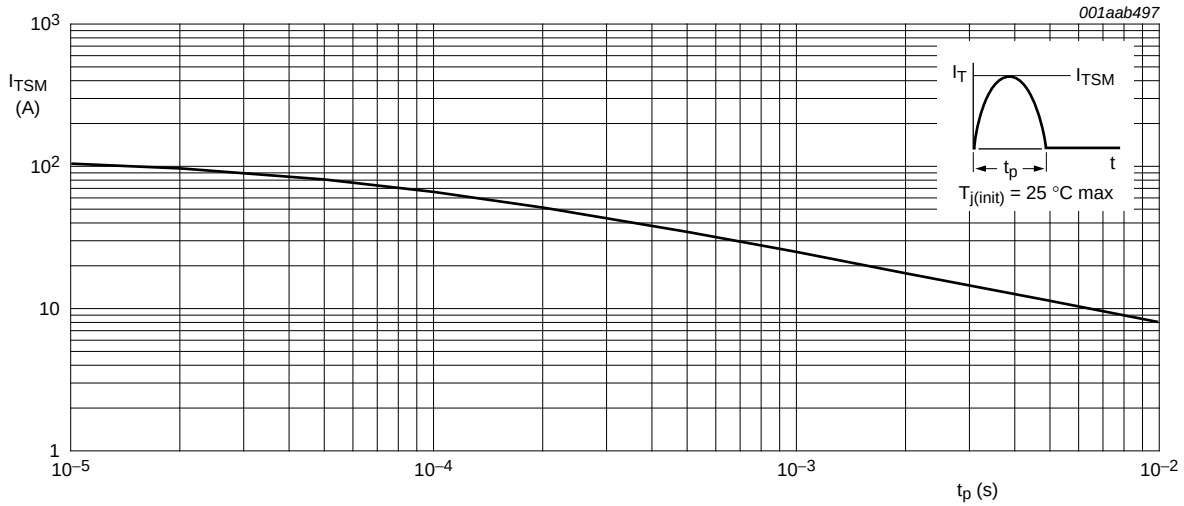

a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

**Fig 1. Total power dissipation as a function of average on-state current; maximum values**



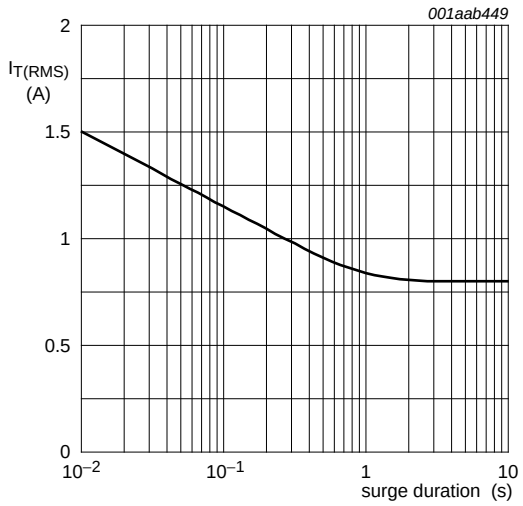

f = 50 Hz.

**Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**



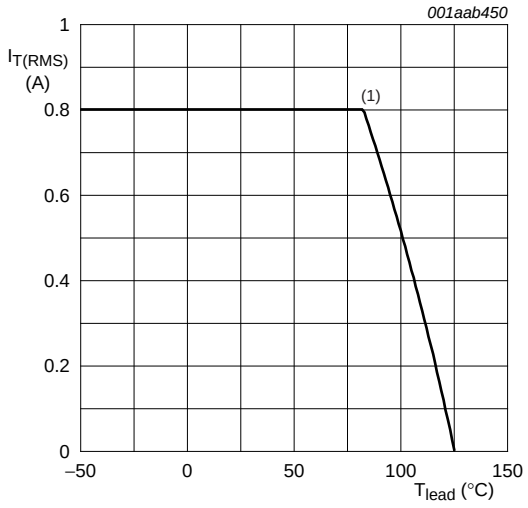

$t_p \leq 10$ ms.

**Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values**




f = 50 Hz; $T_{lead} \leq 83$ °C.

**Fig 4. RMS on-state current as a function of surge duration, for sinusoidal currents; maximum values**




(1) $T_{lead}$ = 83 °C

**Fig 5. RMS on-state current as a function of lead temperature; maximum values**

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}lead)}$ | thermal resistance from junction to lead | | - | - | 60 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | printed-circuit board mounted; lead length = 4 mm | - | 150 | - | K/W |

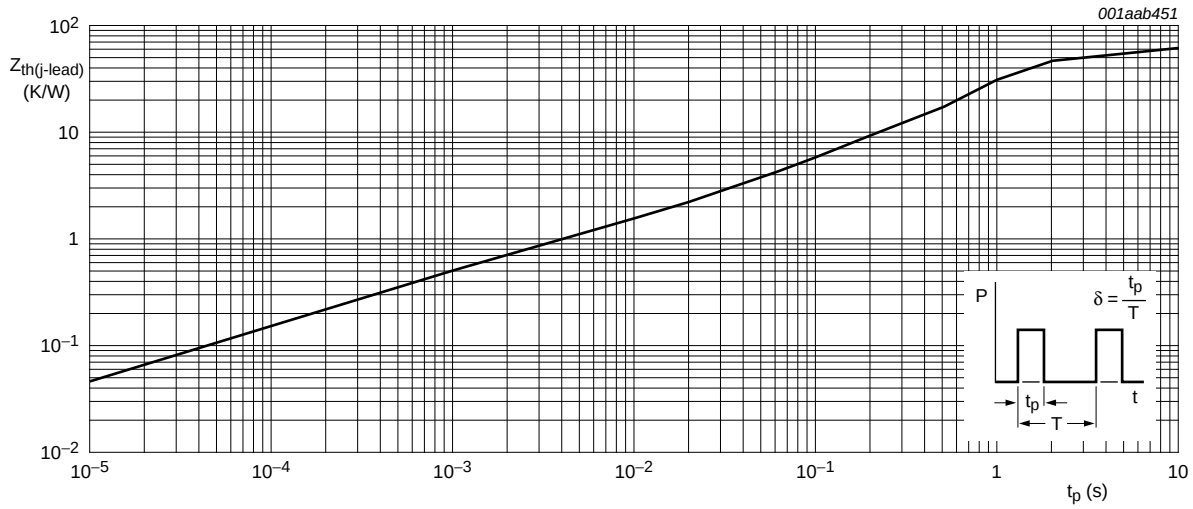



**Fig 6. Transient thermal impedance as a function of pulse width**

## 6. Characteristics

**Table 5. Characteristics**

*$T_j$ = 25 °C unless otherwise stated.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 10 mA; gate open circuit; see Figure 8 | - | 50 | 200 | µA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ; see Figure 10 | - | 2 | 6 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $I_{GT}$ = 0.5 mA; $R_{GK}$ = 1 kΩ; see Figure 11 | - | 2 | 5 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1.2 A | - | 1.25 | 1.7 | V |
| $V_{GT}$ | gate trigger voltage | $I_T$ = 10 mA; gate open circuit; see Figure 7 | | | | |
| | | $V_D$ = 12 V | - | 0.5 | 0.8 | V |
| | | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | 0.2 | 0.3 | - | V |
| $I_D$, $I_R$ | off-state leakage current | $V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j$ = 125 °C; $R_{GK}$ = 1 kΩ | - | 0.05 | 0.1 | mA |
| **Dynamic characteristics** | | | | | | |
| $dV_D/dt$ | critical rate of rise of off-state voltage | $V_{DM}$ = 67 % $V_{DRM(max)}$; $T_j$ = 125 °C; exponential waveform; see Figure 12 | | | | |
| | | gate open circuit | - | 25 | - | V/µs |
| | | $R_{GK}$ = 1 kΩ | 500 | 800 | - | V/µs |
| $t_{gt}$ | gate controlled turn-on time | $I_{TM}$ = 2 A; $V_D = V_{DRM(max)}$; $I_G$ = 10 mA; $dI_G/dt$ = 0.1 A/µs | - | 2 | - | µs |
| $t_q$ | circuit commuted turn-off time | $V_D$ = 67 % $V_{DRM(max)}$; $T_j$ = 125 °C; $I_{TM}$ = 1.6 A; $V_R$ = 35 V; $dI_{TM}/dt$ = 30 A/µs; $dV_D/dt$ = 2 V/µs; $R_{GK}$ = 1 kΩ | - | 100 | - | µs |

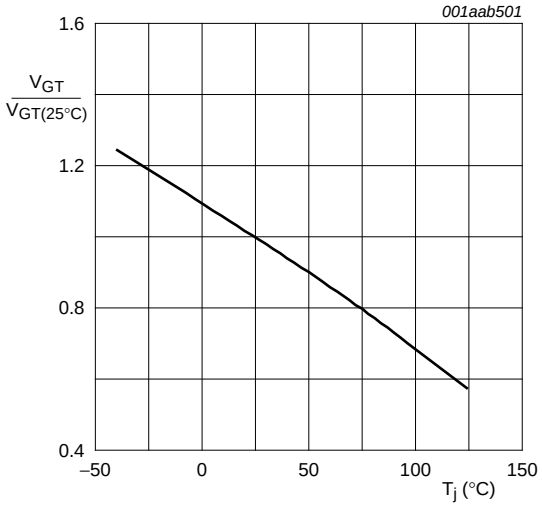



**Fig 7. Normalized gate trigger voltage as a function of junction temperature**

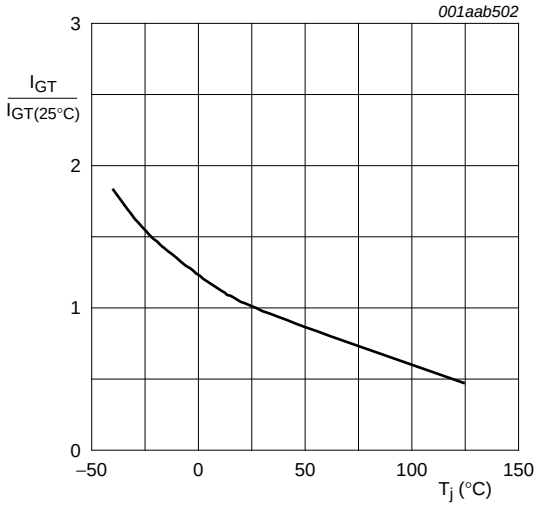
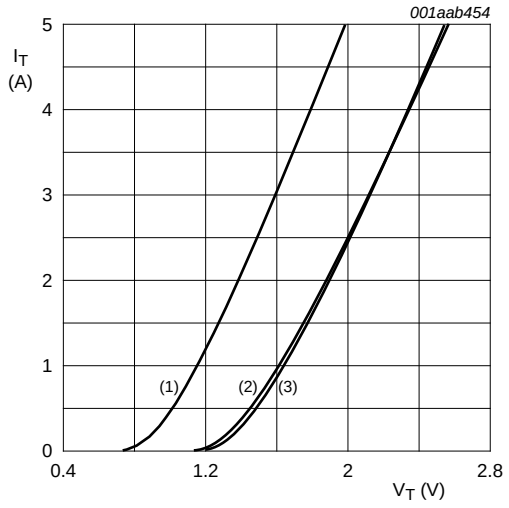



**Fig 8. Normalized gate trigger current as a function of junction temperature**




$V_O$ = 1.067 V.

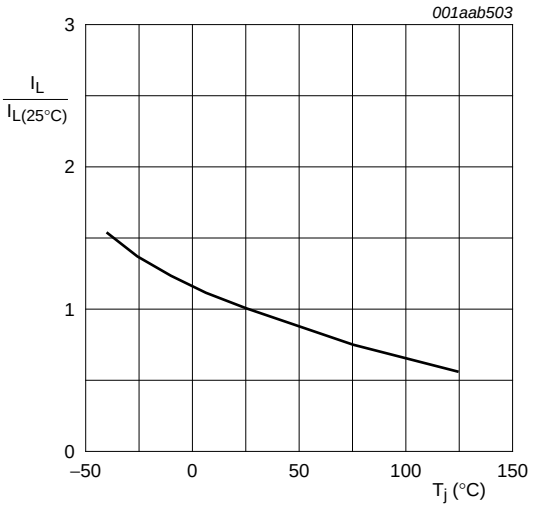
$R_S$ = 0.187 Ω.

(1) $T_j$ = 125 °C; typical values

(2) $T_j$ = 125 °C; maximum values

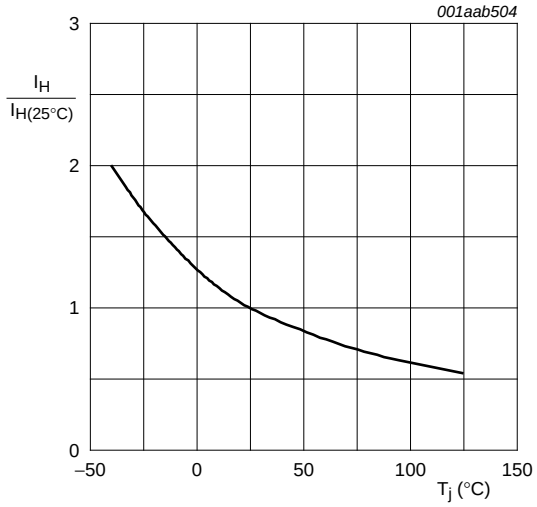
(3) $T_j$ = 25 °C; maximum values

**Fig 9. On-state current characteristics**



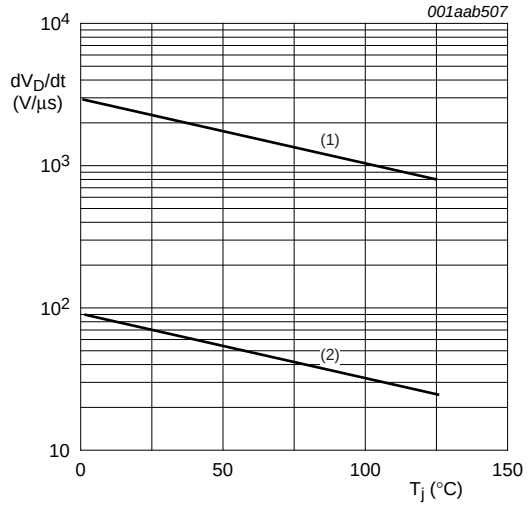

$R_{GK}$ = 1 kΩ.

**Fig 10. Normalized latching current as a function of junction temperature**




$R_{GK}$ = 1 kΩ.

**Fig 11. Normalized holding current as a function of junction temperature**




(1) $R_{GK}$ = 1 kΩ.

(2) Gate open circuit.

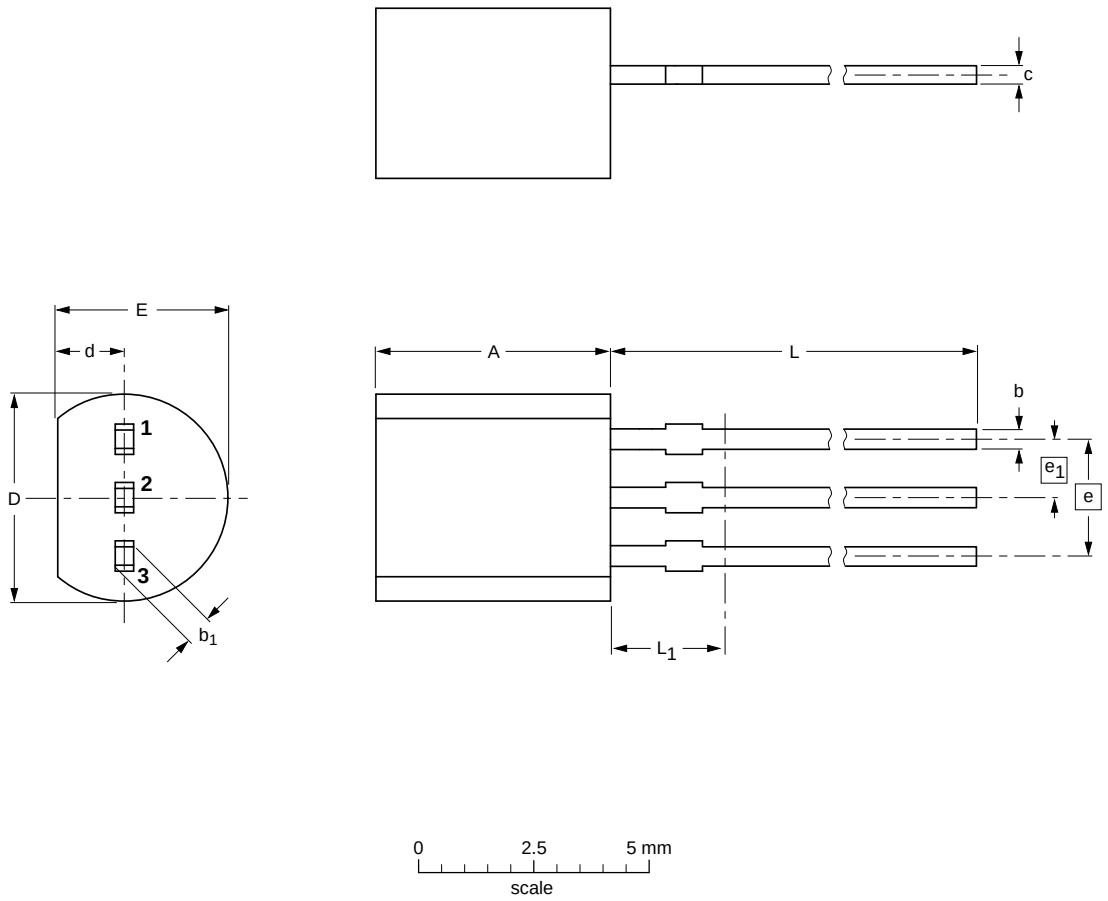
**Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values**

## 7. Package information

Epoxy meets requirements of UL94 V-0 at $^1/_8$ inch.

## 8. Package outline

**Plastic single-ended leaded (through hole) package; 3 leads** **SOT54**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$ (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.55 | 0.45<br>0.38 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27 | 14.5<br>12.7 | 2.5 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT54 | | TO-92 | SC-43A | | | ~~04-06-28~~<br>04-11-16 |

**Fig 13. Package outline SOT54 (TO-92)**

## 9. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BT149_SER v.5 | 20111101 | Product data sheet | | BT149_SERIES v.4 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| BT149_SERIES v.4 | 20040820 | Product data sheet | | BT149_SERIES v.3 |
| BT149_SERIES v.3 | 20010902 | Product specification | | BT149_SERIES v.2 |
| BT149_SERIES v.2 | 20010901 | Product specification | | BT149_SERIES v.1 |
| BT149_SERIES v.1 | 19970901 | Product specification | | - |

# 10. Legal information

## 10.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 12. Contents





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