



500V N-Channel MOSFET

Lead Free Package and Finish

General Features

- Advanced Planar Process
- $R_{DS(ON),typ.}=85\text{ m}\Omega@V_{GS}=10\text{V}$
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

BV_{DSS}	$R_{DS(ON),typ.}$	I_D
500V	85m Ω	46A

Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

Ordering Information

Part Number	Package	Brand
PTW40N50	TO-3P	

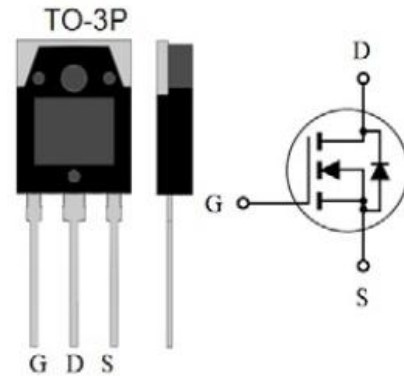
Absolute Maximum Ratings

Symbol	Parameter	PTW40N50	Unit
V_{DSS}	Drain-to-Source Voltage	500	V
V_{GSS}	Gate-to-Source Voltage	± 30	
I_D	Continuous Drain Current	46	A
	Continuous Drain Current @ $T_C=100^\circ\text{C}$	30	
I_{DM}	Pulsed Drain Current at $V_{GS}=10\text{V}^{[2,4]}$	180	
E_{AS}	Single Pulse Avalanche Energy	5000	mJ
dv/dt	Peak Diode Recovery $dv/dt^{[3]}$	5.0	V/ns
P_D	Power Dissipation	540	W
	Derating Factor above 25°C	4.32	W/ $^\circ\text{C}$
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	$^\circ\text{C}$
T_J & T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTW40N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.23	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	



$T_C=25^\circ\text{C}$ unless otherwise specified



Electrical Characteristics

OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	5	μA	$V_{DS}=500V, V_{GS}=0V$
		--	--	500		$V_{DS}=400V, V_{GS}=0V, T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+30V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-30V, V_{DS}=0V$

ON Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	85	100	$m\Omega$	$V_{GS}=10V, I_D=23A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
g_{FS}	Forward Transconductance	--	32	--	S	$V_{DS}=25V, I_D=23A$

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1.0	--	nF	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$
C_{rss}	Reverse Transfer Capacitance	--	0.1	--		
C_{oss}	Output Capacitance	--	0.7	--		
Q_g	Total Gate Charge	--	138	--	nC	$V_{DD}=250V, I_D=23A, V_{GS}=0 \text{ to } 10V$
Q_{gs}	Gate-to-Source Charge	--	38	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	27	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	25	--	nS	$V_{DD}=250V, I_D=23A, V_{GS}=10V, R_G=10\Omega$
t_{rise}	Rise Time	--	39	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	100	--		
t_{fall}	Fall Time	--	36	--		

**Source-Drain Body Diode Characteristics** $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current ^[2]	--	--	46	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current ^[2]	--	--	180		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	$I_S=46\text{A}$, $V_{GS}=0\text{V}$
trr	Reverse recovery time	--	730	--	ns	$V_{GS}=0\text{V}$, $I_F=46\text{A}$, $di_F/dt=100\text{A}/\mu\text{s}$
Qrr	Reverse recovery charge	--	3.0	--	uC	

Note:

- [1] $T_J=+25^{\circ}\text{C}$ to $+150^{\circ}\text{C}$.
[2] Silicon limited current only.
[3] Package limited current.
[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width $\leq 380\mu\text{s}$; duty cycle $\leq 2\%$.



Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

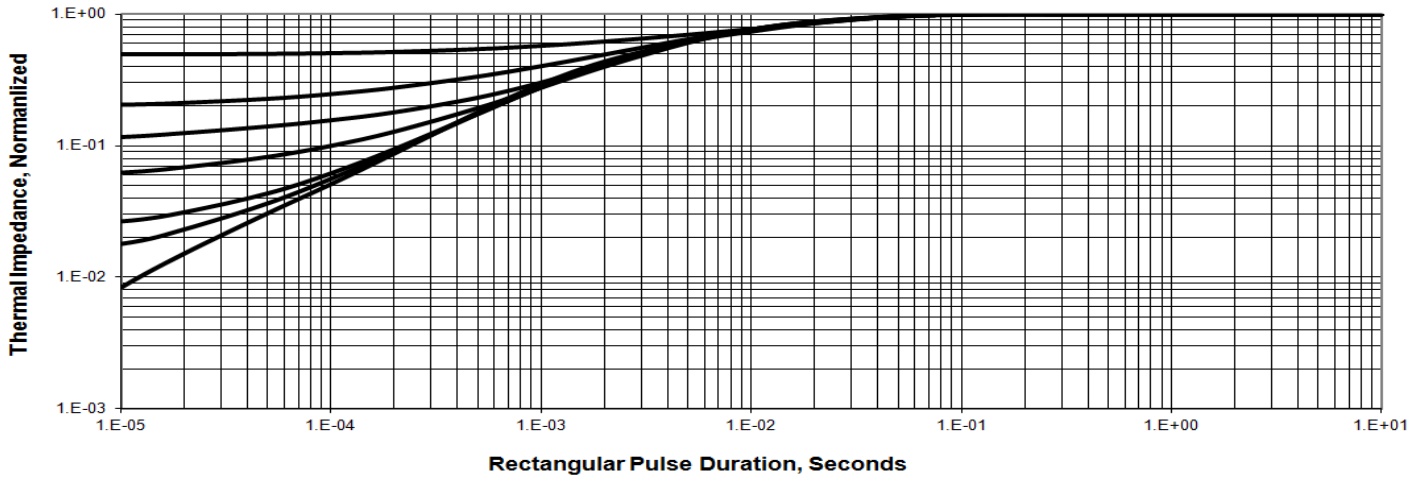


Figure 2 . Max. Power Dissipation vs Case Temperature

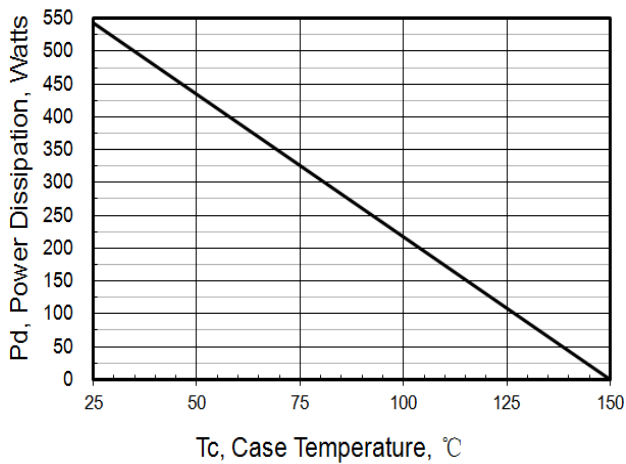


Figure 3 .Maximum Continuous Drain Current vs Tc

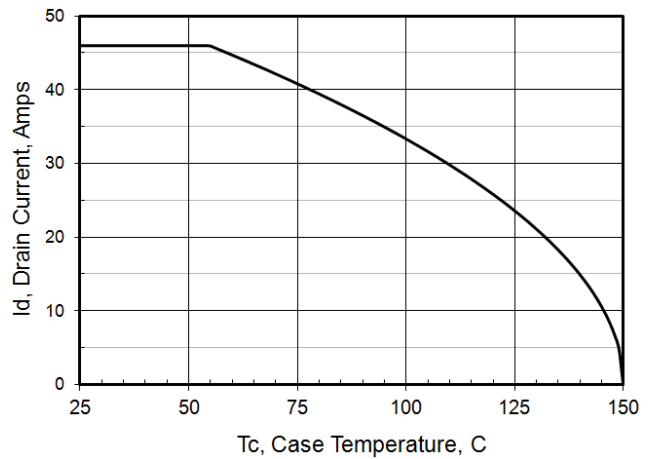


Figure 4. Typical Output Characteristics

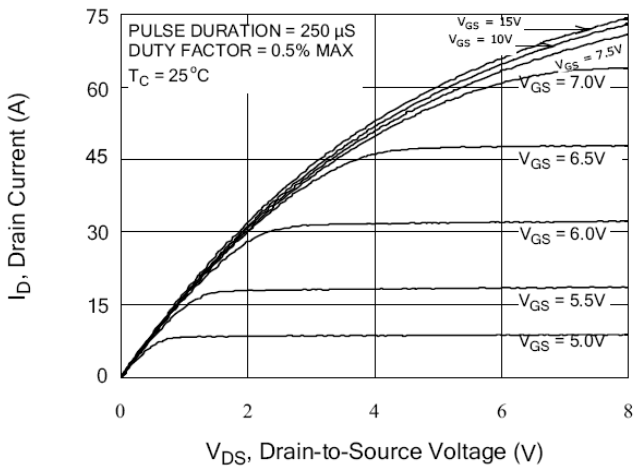
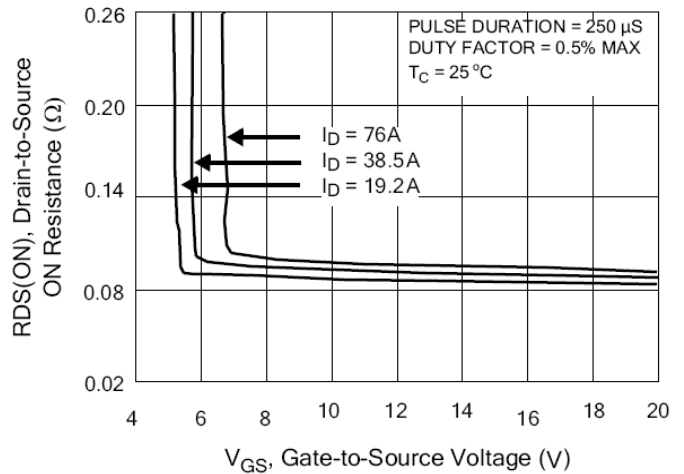


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current





Typical Characteristics(Cont.)

Figure 6. Peak Current Capability

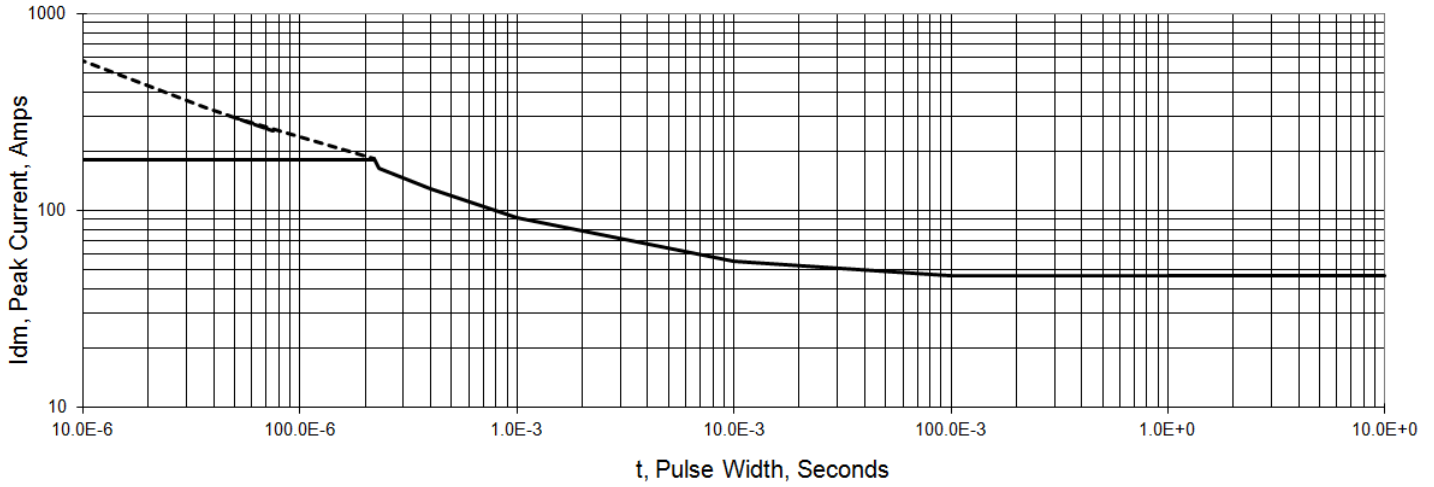


Figure 7. Typical Transfer Characteristics

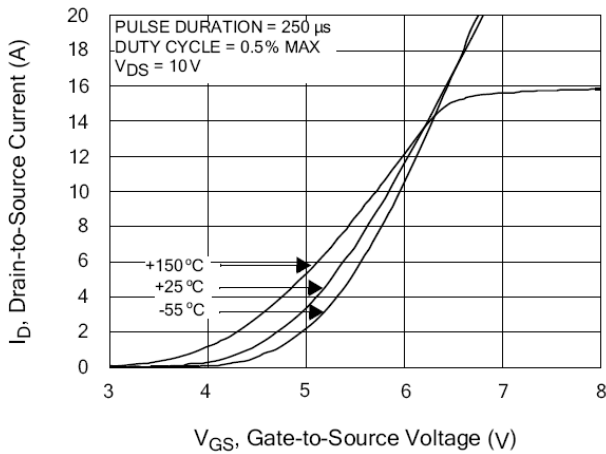


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

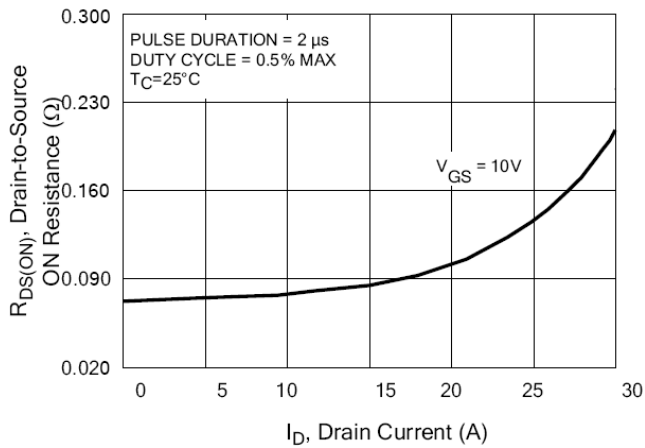


Figure 8. Unclamped Inductive Switching Capability

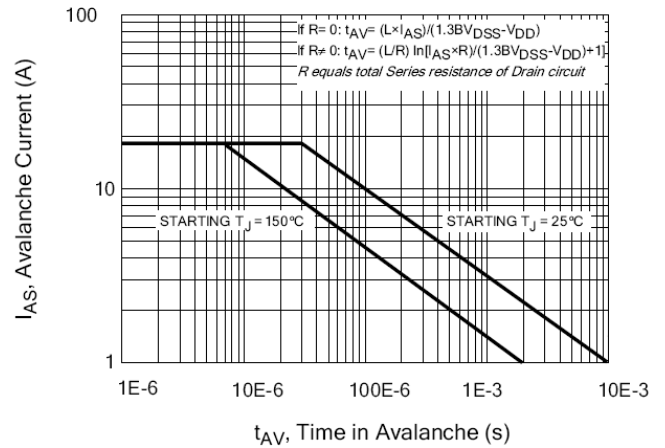
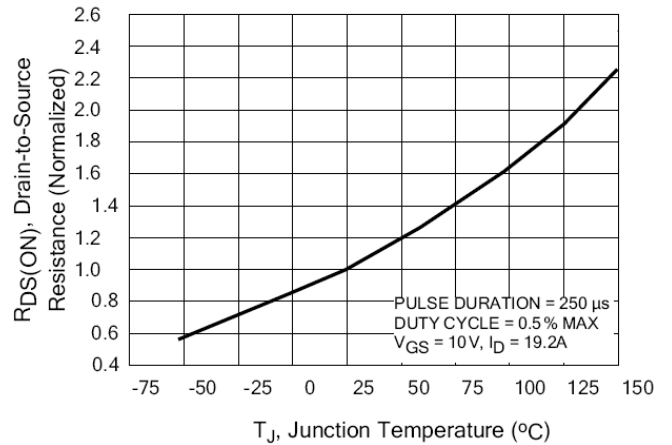


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature





Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

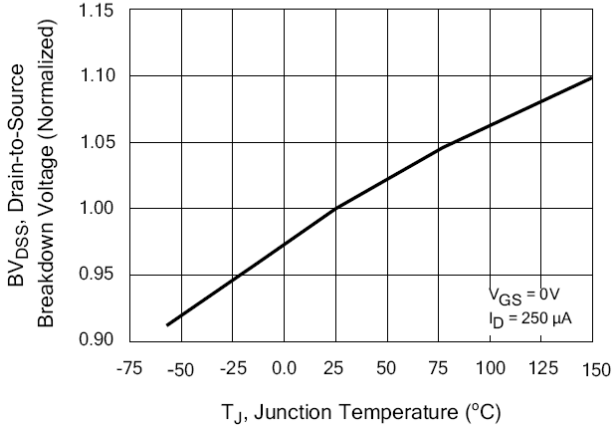


Figure 12. Typical Threshold Voltage vs Junction Temperature

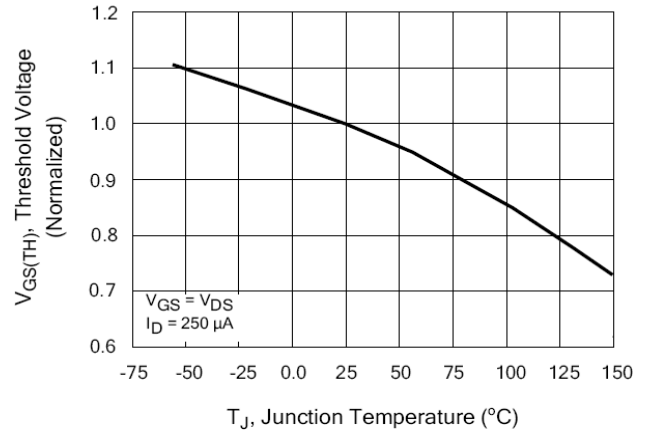


Figure 13. Maximum Forward Bias Safe Operating Area

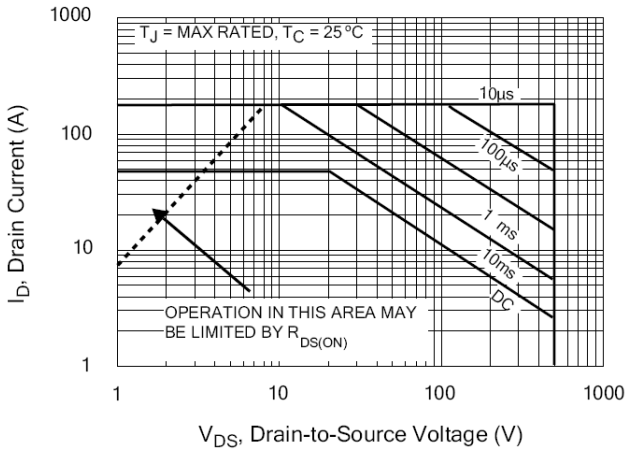


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

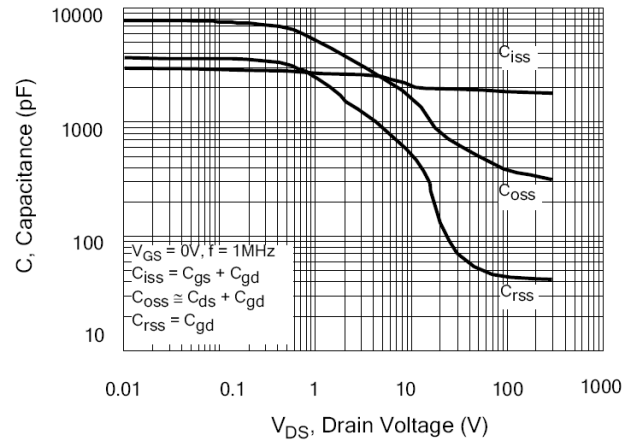


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

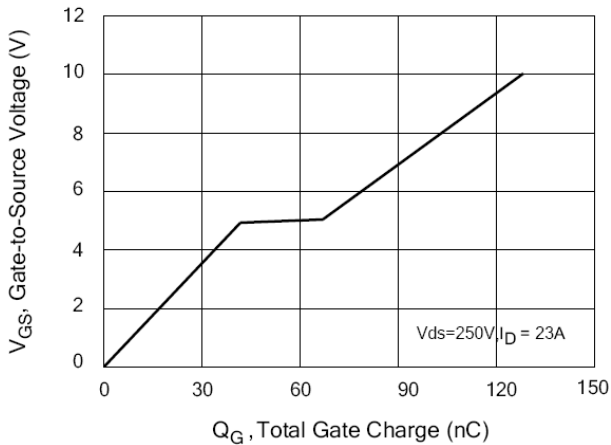
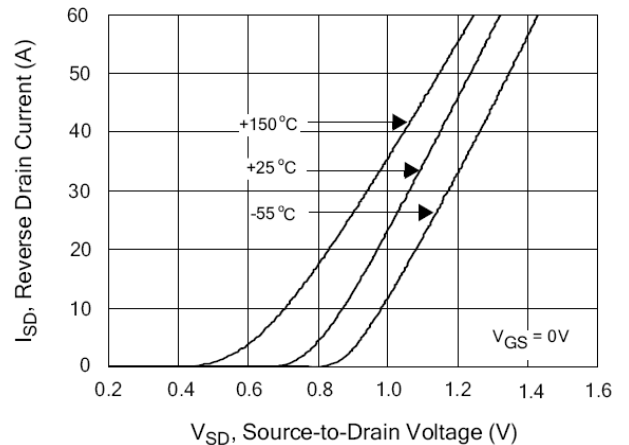


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

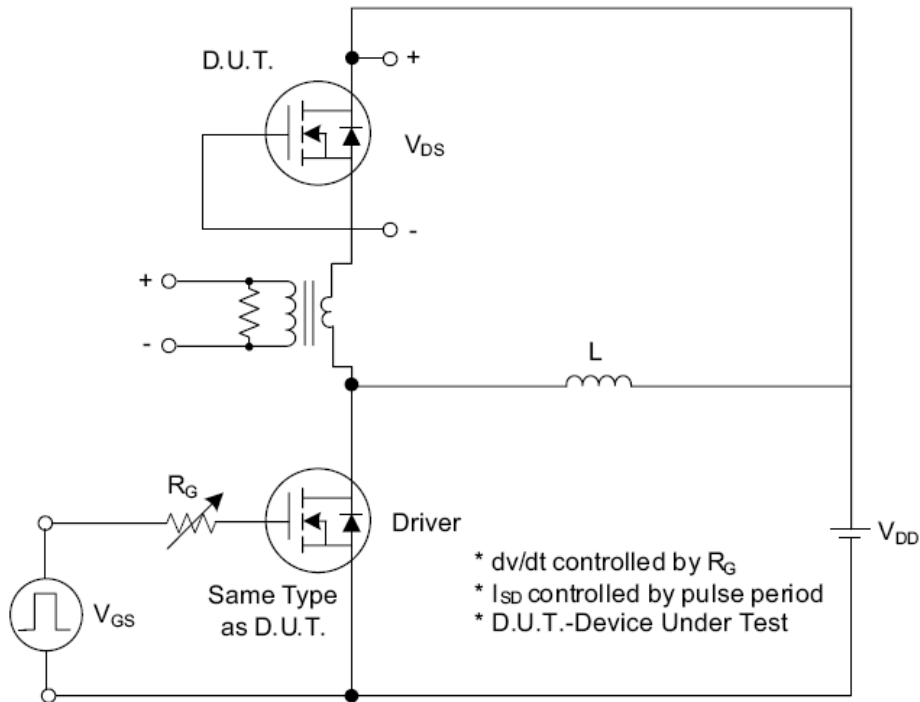


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

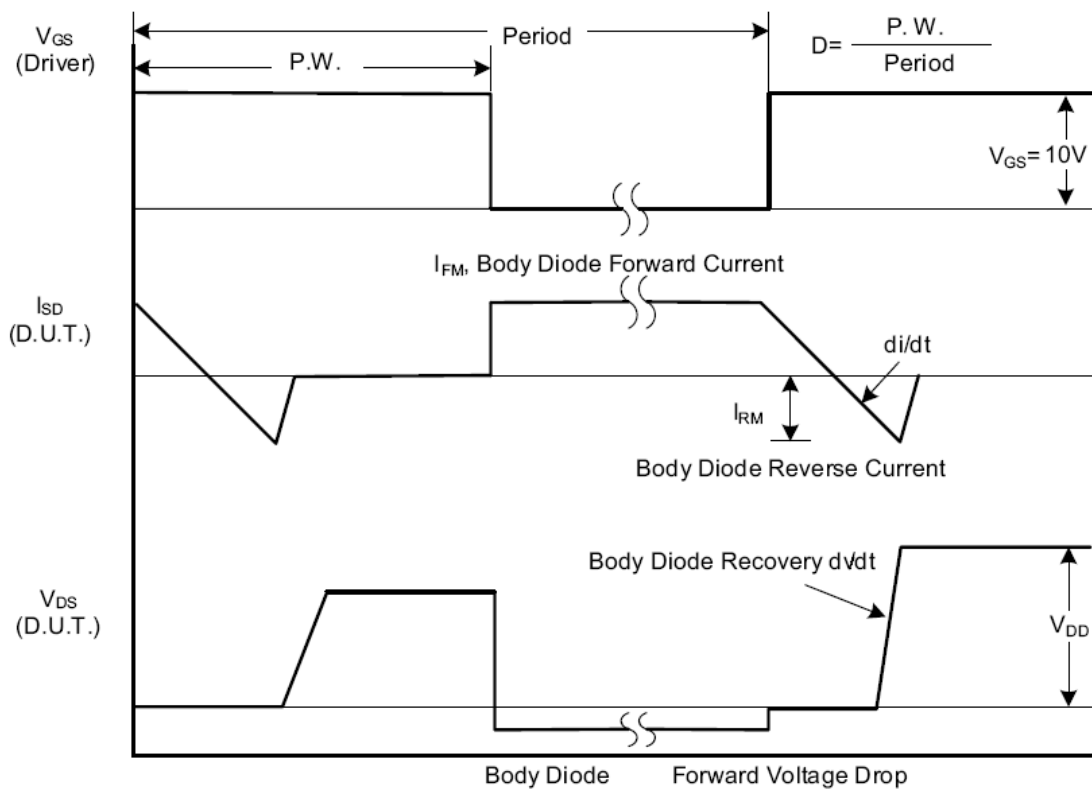


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

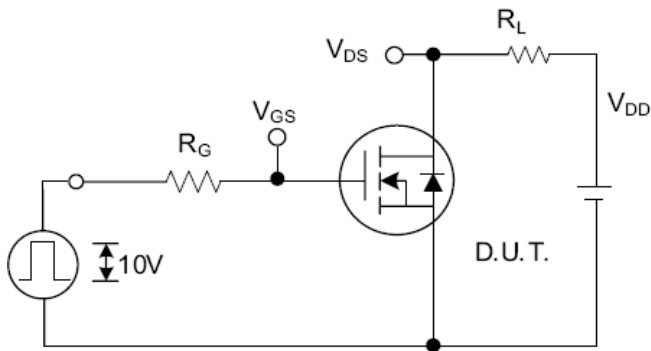
Test Circuits and Waveforms (Cont.)


Fig. 2.1 Switching Test Circuit

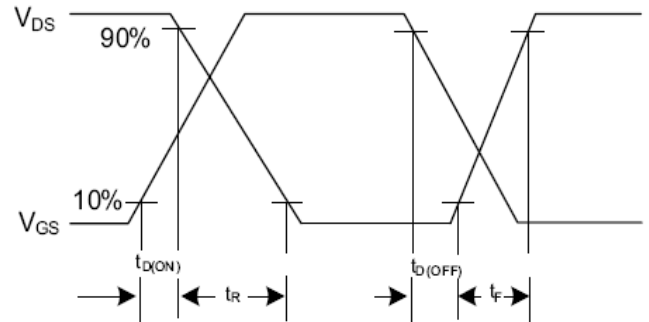


Fig. 2.2 Switching Waveforms

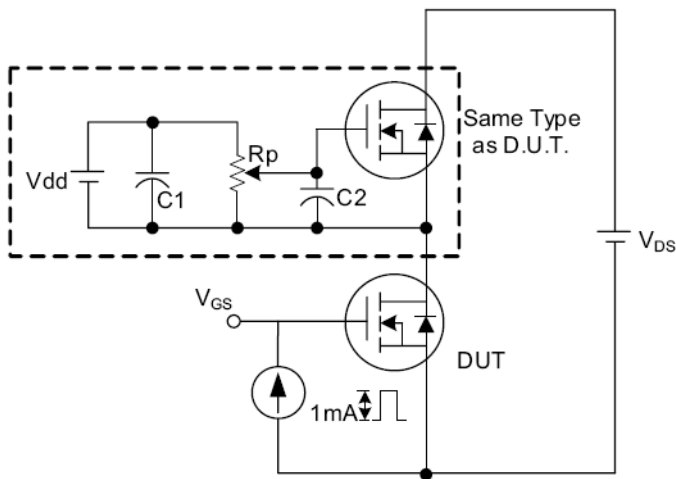


Fig. 3.1 Gate Charge Test Circuit

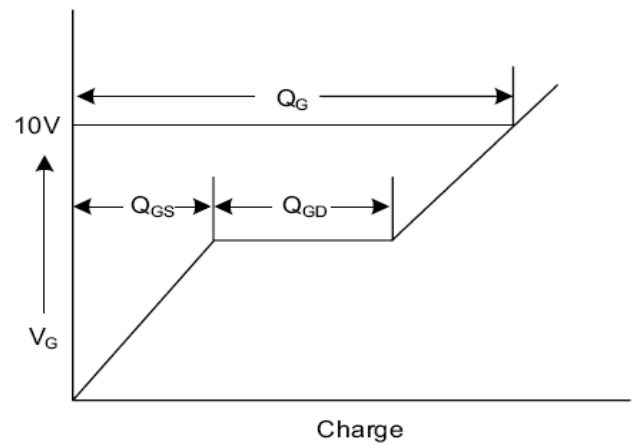


Fig. 3.2 Gate Charge Waveform

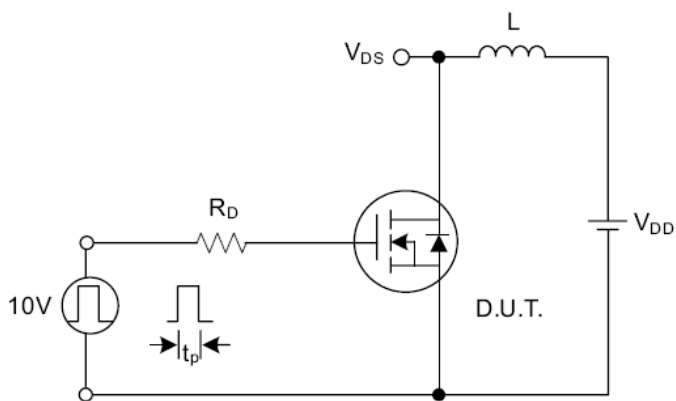


Fig. 4.1 Unclamped Inductive Switching Test Circuit

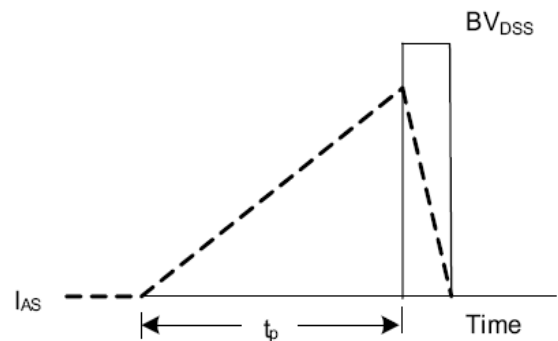


Fig. 4.2 Unclamped Inductive Switching Waveforms



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