Doc version: HME-M7DSE08, Dec, 2018
For more information about M7 Family, please see ***User Guide*** or go to www.hercules-micro.com

Some of the device information comes from CME.

1. Features

32-bit Configurable Application Platform (CAP)

- **High Performance SRAM-based FPGA**
- **High-performance, low-power consumption, 32-bit RISC processor (ARM® Cortex™-M3)**
- **Multi-voltage, multi-standard, multi-banks I/O**
- **2 High-performance dedicated AHB Master/Slave BUS**
- **128 KB Instruction Code SRAM**
- **64 KB Data SRAM**
- **8 KB Instruction Code cache**
- **High-performance dedicated DDRI/II/III controller supporting DDRI/II/III SDRAM**
- **Eight independent high-performance DMA channels**
- **Dual 12 bit 1MSPS ADC and other standard Peripherals**
- **Advanced real-time, in-system debugging capabilities**
- **High security to protect FPGA and M3 processor firmware**
- **In System Management**
  - ISC (In System Configuration)
  - Multi-configuration image support

FPGA

- **SRAM-based FPGA Fabric**
  - up to 11520 4-input Look-up Tables, 7680 DFF-based registers
- **Performance up to 200MHz**
- **Embedded RAM Block Memory**
  - 144 4.5Kbit programmable dual-port memory EMB5K blocks
- **Embedded DSPs block**
  - 16 de-skew global clocks
  - 4 PLLs support frequency multiplication, frequency division, phase-shifting, de-skew
- **8 external input clocks, 1 external crystal clock input**
- **Multi-voltage, multi-standard, multi-banks I/O**
  - 3.3V to 1.5V single-ended and differential I/O standards and protocols
  - Low-cost HSTL and SSTL memory interfaces
  - Dedicated Serdes Circuit for LVDS, DDR II/III standard
  - Up to 800 Mbps data transfer rate per differential I/O
  - Programmable driving strength
  - Programmable slew rate
  - programmable input and output delay
  - Calibrated series and parallel

termination resistor

ARM® Cortex™-M3 processor

- 300 MHz maximum frequency, 375 DMIPS/1.25 DMIPS/MHz performance at 0 wait state memory access
- Single-cycle multiplication and hardware division
- JTAG interfaces
- Cortex-M3 Embedded Trace Macrocell™
- Sleep, Deepsleep low power mode

Memories

- 128 KB Instruction Code SRAM
- 64 KB Data SRAM
- 8KB Instruction Code cache

Peripheral

- High-performance hard DDRI/II/III controller support 16bit DDRII/III memory up to 333MHz
- USB High Speed OTG 2.0 & PHY
- ETH 10/100/1000M controller
- 8 channels DMA
- 2 I2C
- 2 SPI
- 3 UART
- 4 32 bit Timer
- 1x32 GPIO
- 2 CAN 2.0A/B
- low-power RTC
- Dual 12 bit 1MSPS ADC

Configuration

- JTAG Mode
- AS Mode
- PS Mode
- Dynamic/Multi-configuration Image Support

Security

- Encrypted bitstream with 256-bit AES
- Based Efuse and SPI Flash security settings
- Protection against copying, overbuilding, cloning and tampering with both of the FPGA and M3 processor firmware

Feature Summary

Part Number*(1)		M7A12N0(2)	M7A12N5	M7M12N5
Programmable Logic Block (PLB)* (3)	LUT	11520	11520	11520
	Register	7680	7680	7680
Embedded Memory Block (EMB)	4.5Kb	144	144	144
	Max	648Kb	648Kb	648Kb
SRAM* (4)	Code RAM	128KB	128KB	128KB
	Max	128KB	128KB	128KB
	Data RAM	64KB	64KB	64KB
	Max	64KB	64KB	64KB
SDRAM		-	-	64Mb
DSP (5)		48	48	48
PLL		4	4	4
DLL		4	4	4
Crystal (6)		1	1	1
Cortex-M3		1	1	1
DDRII/III Controller		1	1	1
USB High Speed OTG 2.0 & PHY (7)		1	1	1
ETH 10/100/1000M controller		1	1	1
CAN 2.0A/B		2	2	2
12 bit 1MSPS ADC		2	2	2
UART		3	3	3
I2C		2	2	2
SPI		2	2	2
SPI Flash		0	16Mb	16Mb
Max User I/O		310	310	310

Package Information

IPs	Packages				
	LQFP144	FBGA256	VFBGA324	FBGA484	QFN88
RTC (8)	--	1	1	1	-
ADC	8 ch	2 ch	14 ch	14 ch	6ch
DDR data width (9)	--	16 bit	16 bit	16 bit	-
User I/Os (LVDS pairs)	97(27)	156(31)	204(47)	310(75)	59（11）
Part numbers					
M7A12N0	--	Yes	Yes	Yes	Yes
M7A12N5	Yes	Yes	Yes	Yes	Yes
M7M12N5	-	-	-	-	Yes

Notes:

(1) M: FPGA + MCU + SDRAM/PSRAM A: FPGA+ Analog + MCU

(2) 'N0': indicates device contains no Flash, 'N5 'indicates that device contains 16Mb Flash.

(3) Each HME-M7 PLB contains four LPs (Logic parcel). Each LP contains three LUTs and two registers.

(4) M7 series devices: SRAM could only be used by MCU/ FPGA or MCU and FPGA share half SRAM.

(5) Each DSP Block contains an 18 x 18 multiplier with 48 bits accumulator and adder. Each DSP Block can also support two independent 12 x 9 multipliers with 25 bits accumulator.

(6) Crystal need 2 dedicated pins.

(7) USB need 11 dedicated pins.

(8) RTC need 4 dedicated pins.

(9) The M7 must connect 16bit DDR memory.

(10) M6 does not have Cortex-M3, DDRII/III Controller, USB High Speed OTG 2.0 & PHY, ETH 10/100/1000M controller, CAN 2.0A/B, 12 bit 1MSPS ADC, UART, I2C, SPI.

This part gives a brief overview of the M7 family, including its architecture, port definition, and memory map.

2. Overview

The **HME-M7** family device is an intelligent device integrated the ARM Cortex™-M3 32-bit RISC core, high performance FPGA and plenty of peripherals. This high-performance core works at a 300 MHz frequency, a memory protection unit(MPU), high-speed embedded memories (Code RAM memory up to 128 Kbytes with 8K code cache and data RAM up to 64 Kbytes).The high performance FPGA can fulfill customized system design and IP using the programmable logic resources, embedded RAM blocks and DSPs. All devices offer dual 12-bit 1MSPS ADC, four general-purpose 32-bit timers which can be used as time bases. Moreover, the devices contain standard and advanced communication interfaces: I2Cs and SPIs, USARTs, Ethernet, dual CAN and a USB. They also include a real-time clock. The 16bit DDR2/3 hard controller can meet the large and high-speed data memory with access requirements. The AHB bus is used to connect the FPGA, ARM core and the peripherals. A high-performance internal AHB system bus interconnects the embedded processor, its peripherals, and the FPGA at a maximum speed of 300MHz. The bus simultaneously provides 32 bits of read data, 32 bits of write data, and a 32-bit address. Multiple bus masters arbitrate for bus access. Potential bus masters include the ARM Cortex™-M3 processor, the read and write channels of each DMA channel, the JTAG interface, and the FPGA fabric.

Architecture

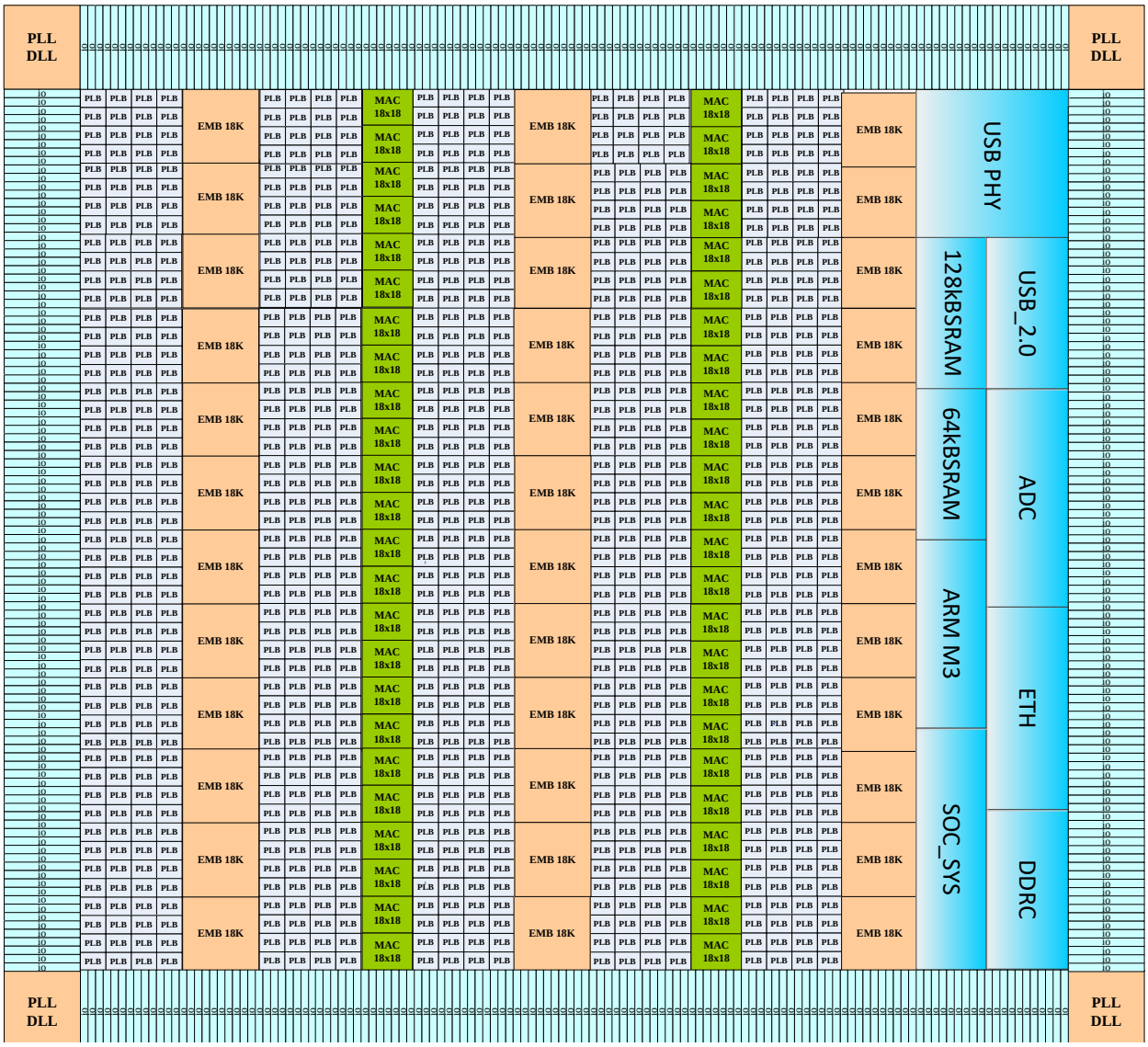


Figure 1 HME-M7 FAMILY FPGA Architecture

Block Diagram

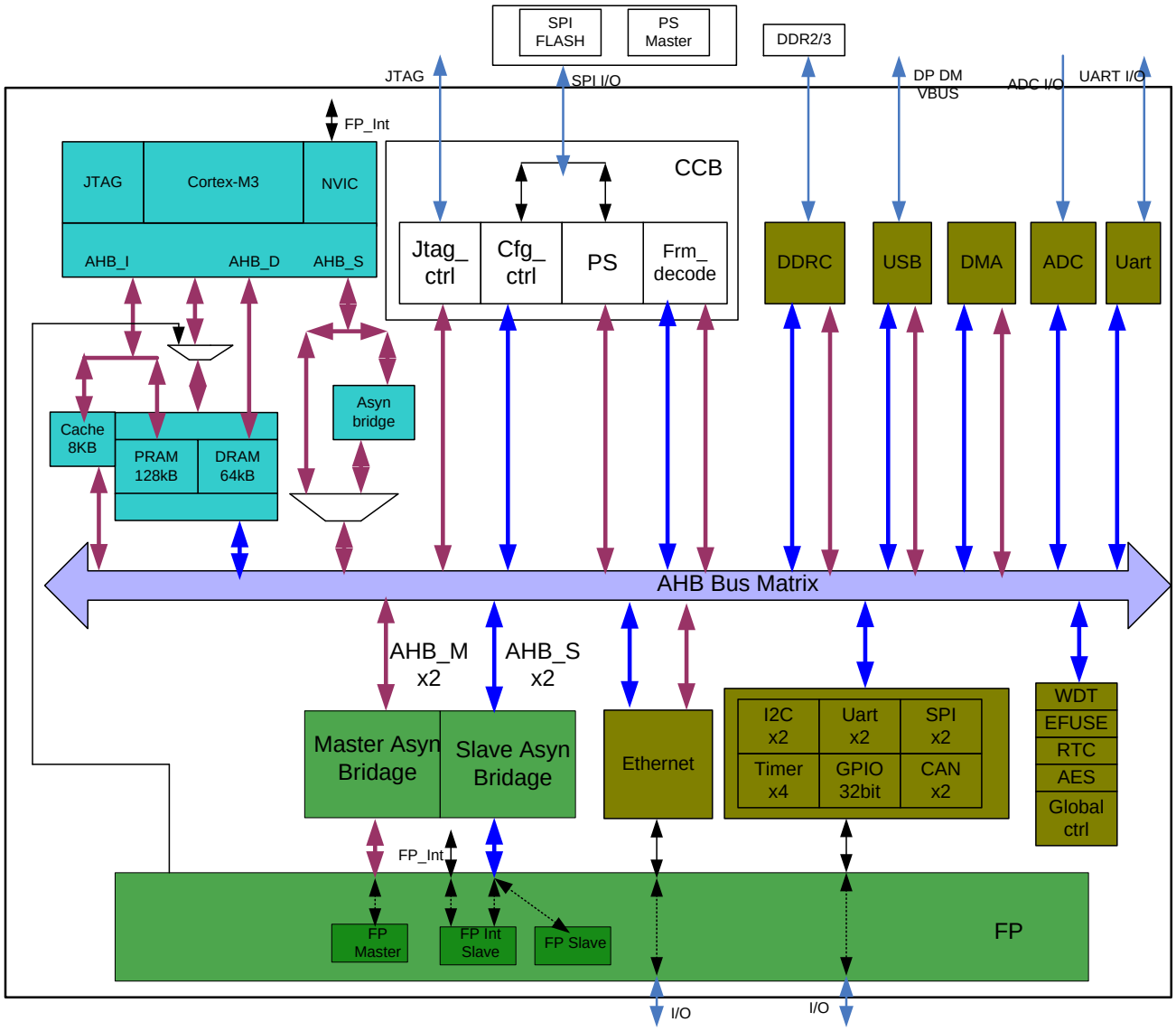


Figure 2 CAP Diagram

The red arrows represent the masters, and the green arrows represent the slaves.

Port Definition

In the view of a FPGA design, the ARM and other modules are considered to be as macro blocks, which will be instantiated in the RTL code of the user design.

The port's direction is from the view of the AHB master the peripherals. All the ports listed below must be routed to fabric or to I/O pins via the fabric, and then the relative IP can be used by FPGA or external devices.

Table 1 CAP Port Definition

Name	Type	Bus Size	Description
Clock			
fp_clk_sys	I	1	System clock from global clock.
fp_clk_adc	I	1	ADC clock from global clock.
fp_clk_usb	I	1	USB clock from global clock.
fp_clk_arm	I	1	ARM core clock from global clock.
fp_clk_ddrc	I	1	DDR controller clock from global clock.
GPIO Interface			
gpio_0_out_o	O	32	GPIO output.
gpio_0_oe_o	O	32	GPIO output enable, high valid.
gpio_0_in_i	I	32	GPIO input.
Interrupt Interface			
fp_interrupt	I	16	Interrupt source from FP to ARM core.
I2C Interface			
i2c0_scl_oe_o	o	1	SCL of I2C 0 output enable; active high.
i2c0_sda_oe_o	o	1	SDA of I2C 0 output, active high.
i2c0_scl_i	i	1	SCL of I2C 0 input.
i2c0_sda_i	o	1	SDA of I2C 0 input.
i2c1_scl_oe_o	o	1	SCL of I2C 1 output enable; active high.
i2c1_sda_oe_o	o	1	SDA of I2C 1 output, active high.
i2c1_scl_i	i	1	SCL of I2C 1 input.
i2c1_sda_i	o	1	SDA of I2C 1 input.
UART Interface			
uart0_rts_o	O	1	Request to send, active high. The UART is ready to receive serial data when this signal is set high.
uart0_txd_o	O	1	Serial data output.
uart0_cts_i	I	1	Clear to send, active high. This is an enable signal for the UART to send serial data.
uart0_rxd_i	I	1	Serial data input.
Uart1_rts_o	O	1	Request to send, active high. The UART is ready to receive serial data when this signal is set high.
Uart1_txd_o	O	1	Serial data output.
Uart1_cts_i	I	1	Clear to send, active high. This is an enable signal for the UART to send serial data.
Uart1_rxd_i	I	1	Serial data input.
SPI Interface			
spi0_mosi	O	1	Data output of SPI 0.

Name	Type	Bus Size	Description
spi0_sck	O	1	Clock of SPI 0.
spi0_ssn	O	1	Chip select of SPI 0.
spi0_miso	I	1	Data input of SPI 0.
spi1_mosi	O	1	Data output of SPI 1.
Spi1_sck	O	1	Clock of SPI 1.
Spi1_ssn	O	1	Chip select of SPI 1.
Spi1_miso	I	1	Clock of SPI 1.
CAN Interface			
pad_can0_o_clk	O	1	Clock output that derived from CAN system clock
pad_can0_o_tx0	O	1	TX0 is the transmit data bus to the transceiver
pad_can0_o_tx1	O	1	tx1 usually ~tx0 but can be setup by OCR register as the tx_clock which is the bit time clock, Baud rate, fires each bit_time period.
pad_can0_oen_tx0	O	1	Tx0 enable, high active.
pad_can0_oen_tx1	O	1	Tx1 enable, high active.
pad_can0_i_rx0	I	1	Receive data, sampled at the negedge pad_can0_o_clk
pad_can1_o_clk	O	1	Clock output that derived from CAN system clock
pad_can1_o_tx0	O	1	TX0 is the transmit data bus to the transceiver
pad_can1_o_tx1	O	1	tx1 usually ~tx0 but can be setup by OCR register as the tx_clock which is the bit time clock, Baud rate, fires each bit_time period.
pad_can1_oen_tx0	O	1	Tx0 enable, high active.
pad_can1_oen_tx1	O	1	Tx1 enable, high active.
pad_can1_i_rx0	I	1	Receive data, sampled at the negedge pad_can1_o_clk
FP0 AHB Master Interface			**FP AHB master 0**
clk_ahb_fp0	I	1	This clock times all bus transfers. All signal timings are related to the rising edge of the clock.
rst_ahb_fp0_n	I	1	The bus reset signal is active LOW and is used to reset the system and the bus.
fp0_m_ahb_mastlock	I	1	Indicates that the current master is performing a locked sequence of transfers. This signal has the same timing as the HMASTER signal.
fp0_m_ahb_prot	I	4	The signals indicate if the transfer is an opcode fetch or data access, as well as if the transfer is a privileged mode access or user mode access. For bus masters with a memory management unit these signals also

Name	Type	Bus Size	Description
			indicate whether the current access is cacheable or bufferable.
fp0_m_ahb_size	I	3	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit), or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
fp0_m_ahb_addr	I	32	The 32-bit system address bus
fp0_m_ahb_write	I	1	When HIGH this signal indicates a write transfer and when LOW a read transfer.
fp0_m_ahb_burst	I	3	Indicates if the transfer forms part of a burst. Four, eight, and sixteen beat bursts are supported and the burst may be either incrementing or wrapping.
fp0_m_ahb_trans	I	2	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
fp0_m_ahb_wdata	I	32	The write data bus is used to transfer data from the master to the bus slaves during write operations.
fp0_m_ahb_ready	O	1	When HIGH the HREADYsignal indicates a transfer has finished on the bus. This signal may be driven LOW to extend a transfer.
fp0_m_ahb_resp	O	1	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.
fp0_m_ahb_rdata	O	32	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
FP0 AHB Slave Interface			**FP AHB slave 0**
fp0_s_ahb_mastlock	O	1	Indicates that the current master is performing a locked sequence of transfers. This signal has the same timing as the HMASTER signal.
fp0_s_ahb_prot	O	4	The signals indicate if the transfer is an opcode fetch or data access, as well as if the transfer is a privileged mode access or user mode access. For bus masters with a memory management unit these signals also indicate whether the current access is cacheable or bufferable.
fp0_s_ahb_size	O	3	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit), or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
fp0_s_ahb_sel	O	1	Each AHB slave has its own slave select signal and this

Name	Type	Bus Size	Description
			signal indicates that the current transfer is intended for the selected slave.
fp0_s_ahb_addr	O	32	The 32-bit system address bus.
fp0_s_ahb_write	O	1	When HIGH this signal indicates a write transfer and when LOW a read transfer.
fp0_s_ahb_burst	O	3	Indicates if the transfer forms part of a burst. Four, eight and sixteen beat bursts are supported and the burst may be either incrementing or wrapping.
fp0_s_ahb_trans	O	2	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE, or BUSY.
fp0_s_ahb_wdata	O	32	The write data bus is used to transfer data from the master to the bus slaves during write operations.
fp0_s_ahb_readyout	I	1	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer.
fp0_s_ahb_resp	I	1	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.
fp0_s_ahb_rdata	I	32	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
FP1 AHB Master Interface			**FP AHB master 1**
clk_ahb_fp1	I	1	This clock times all bus transfers. All signal timings are related to the rising edge of the clock.
rst_ahb_fp1_n	I	1	The bus reset signal is active LOW and is used to reset the system and the bus.
fp1_m_ahb_mastlock	I	1	Indicates that the current master is performing a locked sequence of transfers. This signal has the same timing as the HMASTER signal.
fp1_m_ahb_prot	I	4	The signals indicate if the transfer is an opcode fetch or data access, as well as if the transfer is a privileged mode access or user mode access. For bus masters with a memory management unit these signals also indicate whether the current access is cacheable or bufferable.
fp1_m_ahb_size	I	3	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit), or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
fp1_m_ahb_addr	I	32	The 32-bit system address bus
fp1_m_ahb_write	I	1	When HIGH this signal indicates a write transfer and

Name	Type	Bus Size	Description
			when LOW a read transfer.
fp1_m_ahb_burst	I	3	Indicates if the transfer forms part of a burst. Four, eight and sixteen beat bursts are supported and the burst may be either incrementing or wrapping.
fp1_m_ahb_trans	I	2	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
fp1_m_ahb_wdata	I	32	The write data bus is used to transfer data from the master to the bus slaves during write operations.
fp1_m_ahb_ready	O	1	When HIGH the HREADYsignal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer.
fp1_m_ahb_resp	O	1	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.
fp1_m_ahb_rdata	O	32	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
FP1 AHB Slave Interface			**FP AHB slave 1**
fp1_s_ahb_mastlock	O	1	Indicates that the current master is performing a locked sequence of transfers. This signal has the same timing as the HMASTER signal.
fp1_s_ahb_prot	O	4	The signals indicate if the transfer is an opcode fetch or data access, as well as if the transfer is a privileged mode access or user mode access. For bus masters with a memory management unit these signals also indicate whether the current access is cacheable or bufferable.
fp1_s_ahb_size	O	3	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit), or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
fp1_s_ahb_sel	O	1	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave.
fp1_s_ahb_addr	O	32	The 32-bit system address bus.
fp1_s_ahb_write	O	1	When HIGH this signal indicates a write transfer and when LOW a read transfer.
fp1_s_ahb_burst	O	3	Indicates if the transfer forms part of a burst. Four, eight and sixteen beat bursts are supported and the burst may be either incrementing or wrapping.

Name	Type	Bus Size	Description
fp1_s_ahb_trans	O	2	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE, or BUSY.
fp1_s_ahb_wdata	O	32	The write data bus is used to transfer data from the master to the bus slaves during write operations.
fp1_s_ahb_readyout	I	1	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer.
fp1_s_ahb_resp	I	1	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.
fp1_s_ahb_rdata	I	32	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
SDRAM interface			
A[0:10]	O	11	Multiplexed pins for row and column address. Row address: A0-A10. Column address: A0-A7. A10 is sampled during a precharge command to determine if all banks are to be precharged or bank selected by BS0, BS1.
BS[0:1]	O	2	Select bank to activate during row address latch time, or bank to read/write during address latch time.
DQ[0:31]	I/O	32	Multiplexed pins for data output and input.
$\overline{CS}$	O	1	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
$\overline{RAS}$	O	1	Command input. When sampled at the rising edge of the clock $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed.
$\overline{CAS}$	O	1	Referred to $\overline{RAS}$
$\overline{WE}$	O	1	Referred to $\overline{RAS}$
DQM[0:3]	I/O	4	The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
CLK	O	1	System clock used to sample inputs on the rising edge of clock.
CKE	O	1	CKE controls the clock activation and deactivation. When CKE is low, Power Down

Name	Type	Bus Size	Description
			mode, Suspend mode, or Self Refresh mode is entered.

Memory Map

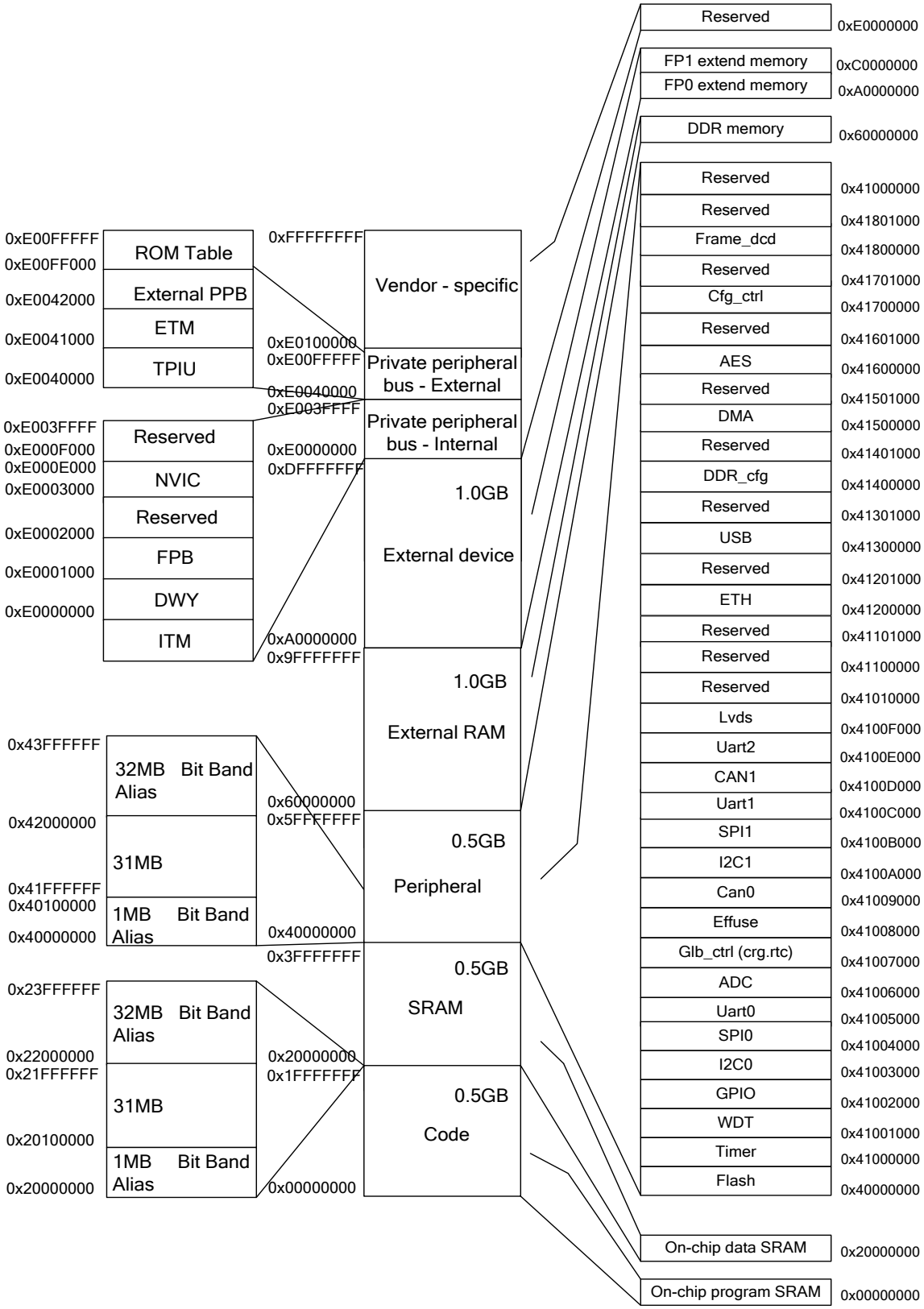


Figure 3 System Memory Map

Table 2 M7 Boundary Addresses

ADDR	Size	Port No.	Description
32'h0000_0000 ---32'h1fff_ffff	0.5G	B	S_memory program region (only m3_sys/jtag/dmac can access this region)
32'h2000_0000 ---32'h3fff_ffff	0.5G	D	S_memory data region
32'h4000_0000 ---32'h40ff_ffff	16M	0	Flash
32'h4100_0000 ---32'h4100_0fff	4k	1	Timer
32'h4100_1000 ---32'h4100_1fff	4k	1	WDT
32'h4100_2000 ---32'h4100_2fff	4k	1	GPIO
32'h4100_3000 ---32'h4100_3fff	4k	1	I2C0
32'h4100_4000 ---32'h4100_4fff	4k	1	SPI0
32'h4100_5000 ---32'h4100_5fff	4k	1	Uart0
32'h4100_6000 ---32'h4100_6fff	4k	1	ADC
32'h4100_7000 ---32'h4100_7fff	4k	1	Glb_ctrl
32'h4100_8000 ---32'h4100_8fff	4k	1	Effuse
32'h4100_9000 ---32'h4100_9fff	4k	1	Can0
32'h4100_a000 ---32'h4100_afff	4k	1	I2C1
32'h4100_b000 ---32'h4100_bfff	4k	1	SPI1
32'h4100_c000 ---32'h4100_cfff	4k	1	Uart1
32'h4100_d000 ---32'h4100_dfff	4k	1	Can1
32'h4100_e000 ---32'h4100_efff	4k	1	Uart2
32'h4100_f000 ---32'h4100_ffff	4k	1	Lvds
32'h4101_0000 ---32'h410f_ffff	---	1	Reserved
32'h4110_0000 ---32'h4110_0fff	4k	2	Reserved
32'h4110_1000 ---32'h411f_ffff	---	2	Reserved
32'h4120_0000 ---32'h4120_0fff	4k	3	ETH
32'h4120_1000 ---32'h412f_ffff	---	3	Reserved
32'h4130_0000 ---32'h4130_0fff	4k	4	USB
32'h4130_1000 ---32'h413f_ffff	---	4	Reserved
32'h4140_0000 ---32'h4140_0fff	4k	5	DDR register
32'h4140_1000 ---32'h414f_ffff	---	5	Reserved
32'h4150_0000 ---32'h4150_0fff	4k	6	DMA
32'h4150_1000 ---32'h415f_ffff	---	6	Reserved
32'h4160_0000 ---32'h4160_0fff	4k	7	AES
32'h4160_1000 ---32'h416f_ffff	---	7	Reserved
32'h4170_0000 ---32'h4170_0fff	4k	8	Configuration register
32'h4170_1000 ---32'h417f_ffff	---	8	Reserved

ADDR	Size	Port No.	Description
32'h4180_0000 ---32'h4180_0fff	4k	9	Frame_dcd
32'h4180_1000 ---32'h418f_ffff	---	9	Reserved
32'h4190_0000 ---32'h5fff_ffff	---	A	Reserved
32'h6000_0000 ---32'h9fff_ffff	1G	F	DDR memory
32'ha000_0000 ---32'hbfff_ffff	0.5G	C	Expand memory space for user logic in FP0
32'hc000_0000 ---32'hdfff_ffff	0.5G	E	Expand memory space for user logic in FP1
32'he000_0000 ---32'hffff_ffff	0.5G	A	Reserved

Note: *The operation to the reserved region is forbidden, otherwise, unexpected exception will happen.*

This part lists the DC and Switching characteristics for users to quickly search.

3. DC & Switching Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

DC Electrical Characteristics

Absolute Maximum Ratings

Stresses beyond those listed in table below: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods adversely affects device reliability.

Table 3 Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Max	Units
VDD_CORE	Internal supply voltage		-0.5	1.25	V
VDDIO	I/O driver supply voltage		-0.5	3.75	V
VIN	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	GND-0.2		V
	Voltage applied to all Dedicated pins		GND-0.2		V
VESD	Electrostatic Discharge Voltage	Human body model	0	±2000	V
		Charged device model	-	±500	V
		Machine model	-	±200	V
TJ	Junction temperature		-40	125	°C
TSTG	Storage temperature		–65	150	°C

Power Supply Specifications

Table 4 Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Typ	Units
VDD_CORET	Threshold for the VCCINT supply		0.7	V

Symbol	Description	Min	Typ	Units
VDD33T	Threshold for the VDDIO supply		1.863	V

Table 5 Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
VDD_CORET	Ramp rate from GND to valid VCCINT supply level	10		us
VDD33R	Ramp rate from GND to valid VDDIO supply level	10		us

Notes: *The VDD_CORE must be powered to the threshold before the VDDIO.*

General Recommended Operating Conditions

Table 6 Recommended Basic Operating Conditions

Symbol	Parameter	Min	Typ	Max
TJ	Junction temperature	-40°C	25°C	125°C
VDD_CORE	Core power	1.0V	1.1V	1. 2V
VDD33	JTAG/FLASH power	3.135V	3.3V	3.465V
VCC33A_PLL	USB PHY PLL power	3.135V	3.3V	3.465V
VCC33A_HSRT	JTAG/FLASH power	3.135V	3.3V	3.465V
RTC_VDDBAT	RTC Power	2.2V		3.3V
VDDADC	ADC Power @ 3.3V	3.135V	3.3V	3.465V
	@2.5V	2.375V	2.5V	2.625V
VDDIO	I/O supply voltage @ 3.3V	2.97V	3.3V	3.63V
	@2.5V	2.375V	2.5V	2.625V
	@1.8V	1.71V	1.8V	1.89V
	@1.5V	1.425V	1.5V	1.575V
V_I	Input Voltage	-0.5	-	VDDIO +0.3
V_O	Output Voltage	-0.3	-	VDDIO
I_L	Input Leakage Current	±1μA		

General Core Leakage Current

Table 7 General Leakage Current

Symbol	Parameter	Min	Typ	Max
I_{slc}	Static leakage core supply current		100mA	

General DC Characteristics for I/O Pins

Table 8 I/O Pin Leakage Current

Symbol	Parameter	Min	Typ	Max
I_{ozl}	Tristated I/O pin leakage Current	-10uA	-	10uA
I_{IL}	Input Leakage Current	-10uA	-	10uA

Symbol	Parameter	Min	Typ	Max
I_{IOL}	VCC I/O leakage current(@3.3V)		10uA	

Table 9 Single-ended I/O Pin Driving Strength

Supported Voltage and Current Capabilities	Attributes	Value
Drive strength	I/O supply voltage @ 3.3V	4mA
		8mA
		12mA
		16mA
	I/O supply voltage @ 2.5V	4mA
		8mA
		12mA
		16mA
	I/O supply voltage @ 1.8V	2mA
		4mA
		8mA
		12mA
	I/O supply voltage @ 1.5V	2mA
		4mA
		8mA

Table 10 Single-ended I/O Pull-Up and Pull-Down Resistor

Symbol	Parameter	Min	Typ	Max	Units
R_{PU}	Value of the I/O pin pull-up resistor		70		kΩ

Table 11 DDR I/O pull up/pull down termination resister select

Symbol	Attributes	Min	Typ	Max	Units
$R_{tpdt/pu}$	DDR I/O pull up/pull down termination resister value on temperature =25°C condition		0		Ω
			25		Ω
			33		Ω
			45		Ω
			50		Ω
			75		Ω
			100		Ω
			150		Ω

I/O Standard Specifications

Table 12 Single-ended I/O Standard Input DC Specifications

I/O Standard	VDDIO (V)			Vref (V)			Vil (V)	Vih (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
3.3V LVTTL and LVCMOS	3.135	3.3	3.465	-	-	-	0.8	1.7
2.5V LVTTL and LVCMOS	2.375	2.5	2.625	-	-	-	0.7	1.7
1.8V LVTTL and LVCMOS	1.710	1.8	1.890	-	-	-	0.35 x VDDIO	0.65 x VDDIO
1.5V LVCMOS	1.425	1.5	1.575	-	-	-	0.35 x VDDIO	0.65 x VDDIO
SSTL2 Class I	2.375	2.5	2.625	1.19	1.25	2.31	Vref-0.18 (DC) Vref-0.35 (AC)	Vref+0.18 (DC) Vref+0.35 (AC)
SSTL2 Class II	2.375	2.5	2.625	1.19	1.25	2.31	Vref-0.18 (DC) Vref-0.35 (AC)	Vref+0.18 (DC) Vref+0.35 (AC)
SSTL18 Class I	1.7	1.8	1.9	0.833	0.9	0.969	Vref-0.125 (DC) Vref-0.250 (AC)	Vref+0.125 (DC) Vref+0.250 (AC)
SSTL18 Class II	1.7	1.8	1.9	0.833	0.9	0.969	Vref-0.125 (DC) Vref-0.250 (AC)	Vref+0.125 (DC) Vref+0.250 (AC)
1.8V HSTL Class I	1.71	1.8	1.89	0.85	0.9	0.95	Vref-0.1 (DC) Vref-0.2 (AC)	Vref+0.1 (DC) Vref+0.2 (AC)
1.8V HSTL Class II	1.71	1.8	1.89	0.85	0.9	0.95	Vref-0.1 (DC) Vref-0.2 (AC)	Vref+0.1 (DC) Vref+0.2 (AC)
1.5V HSTL Class I	1.425	1.5	1.575	0.71	0.75	0.79	Vref-0.1 (DC) Vref-0.2 (AC)	Vref+0.1 (DC) Vref+0.2 (AC)
1.5V HSTL Class II	1.425	1.5	1.575	0.71	0.75	0.79	Vref-0.1 (DC) Vref-0.2 (AC)	Vref+0.1 (DC) Vref+0.2 (AC)

Table 13 Single-ended I/O Standard Output DC Specifications

I/O Standard	Test Conditions		Voltage Threshold	
	Iol (mA)	Ioh (mA)	Maximum Vol (V)	Minimum Voh (V)
3.3V LVTTL	4	-4	0.4	2.4
3.3V LVCMOS	0.1	-0.1	0.4	VDDIO – 0.4
2.5V LVTTL and LVCMOS	1	-1	0.4	2.1
1.8V LVTTL and LVCMOS	2	-2	0.45	VDDIO – 0.45
1.5V LVTTL and LVCMOS	2	-2	0.375	VDDIO – 0.375
SSTL2 Class I	8.1	-8.1	Vtt-0.57	Vtt+0.57
SSTL2 Class II	16.4	-16.4	Vtt-0.76	Vtt+0.76
SSTL18 Class I	6.7	-6.7	Vtt-0.475	Vtt+0.475

I/O Standard	Test Conditions		Voltage Threshold	
	Iol (mA)	Ioh (mA)	Maximum Vol (V)	Minimum Voh (V)
SSTL18 Class II	13.4	-13.4	0.28	VDDIO – 0.28
1.8V HSTL Class I	8	-8	0.4	VDDIO – 0.4
1.8V HSTL Class II	16	-16	0.4	VDDIO – 0.4
1.5V HSTL Class I	8	-8	0.4	VDDIO – 0.4
1.5V HSTL Class II	16	-16	0.4	VDDIO – 0.4

Table 14 Differential I/O Standard Output DC Specifications

I/O Standard	VDDIO (V)			Vid (V)			Vicm (V)			Vil (V)		Vih (V)	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	2.375	2.5	2.625	0.1		0.65	0.1		2.0	-	-	-	-
MiniLVDS	2.375	2.5	2.625	-	-	-	-	-	-	-	-	-	-
RSDS	2.375	2.5	2.625	-	-	-	-	-	-	-	-	-	-
Differential 1.5V HSTL Class I and Class II	1.425	1.5	1.575	0.2	-	VDDIO + 0.6	0.68	0.75	0.90	-	Vref – 0.2	Vref + 0.2	-
Differential 1.8V HSTL Class I and Class II	1.71	1.8	1.89	0.2	-	VDDIO + 0.6	0.68	-	0.90	-	Vref – 0.2	Vref + 0.2	-
Differential SSTL2 Class I and Class II	2.375	2.5	2.625	0.36	-	VDDIO + 0.6	0.5 x VDDIO - 0.2	0.5 x VDDIO	0.5 x VDDIO + 0.2	-	Vref – 0.35	Vref + 0.35	-
Differential SSTL18 Class I and Class II	1.7	1.8	1.9	0.25	-	VDDIO + 0.6	0.5 x VDDIO - 0.2	0.5 x VDDIO	0.5 x VDDIO + 0.2	-	Vref – 0.25	Vref + 0.25	-

RTC Specifications

Table 15 RTC DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vin	Input Voltage		2.2	3.0	3.3	V
Tst	Star-up time	vddbat =3.0v			5	s
I_{QC}	Battery current	vddbat =2.5v		1		uA

ADC Specifications

Table 16 ADC Specifications

Conditions: VDDADC=2.5V, CEXT=1uF, SYSCLK=32Mhz,25°C, unless other specified

Symbol	Description	Min	Typ	Max
VDDADC	Analog power	2.375V	2.5V	2.625V
		3.135V	3.3V	3.465V
VREFP			1.0V	
VREFN			0	
Input voltage range (Vinp-Vinn)		-1V		1V
ENOB		10.0		
SNDR			62dB	
SFDR	Differential input		-75dB	
DNL			+/-0.7LSB	
INL			+/-1LSB	
Conversion Speed			1MSPS	
Conversion time	Number of clk cycle			32
ADC clock frequency				32MHz
Channel Crosstalk			-60dB	
On-chip supply moinitor error	With calibration			1.0%
On-chip temperature monitor error	With calibration			±4°C
Supply current	Operating Current		2.0mA	

USB Specifications

Table 17 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBUS	VBUS input	All operating modes	4.75	5.0	5.25	V
VCCA	Analog power supply	VCC33A_HSRT and VCC33A_PLL belong to the VCCA group	3.0	3.3	3.6	V
VCC	Digital power supply	VCC10D_U20	0.9	1	1.1	V
Vnoise	Allowable power noise on analog supply	1 Hz ~ 100 kHz	-	-	300	mV
Vnoise	Allowable power noise	1 Hz ~ 100 kHz	-	-	100	mV

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	on digital supply					
IVCC33A_HSRT	Operating current of the VCC33A_HSRT domain in a different mode	In the HS mode (480 Mbps)	-	-	35	mA
		In the FS mode (12 Mbps)	-	-	20	mA
		In the LS mode (1.5 Mbps)	-	-	15	mA
		In the suspend mode (Without connecting the pull-up resistor on DP)	-	-	20	uA
IVCC33A_PLL	Operating current of the VCC33A_HSRT domain in a different mode	In the HS mode (480 Mbps)	-	-	10	mA
		In the FS mode (12 Mbps)	-	-	10	mA
		In the LS mode (1.5 Mbps)	-	-	10	mA
		In the suspend mode (Without connecting the pull-up resistor on DP)	-	-	10	uA
I VCC10D_U20	Operating current of the VCC10D_U20 domain in a different mode	In the HS mode (480 Mbps)	-	-	5	mA
		In the FS mode (12 Mbps)	-	-	3	mA
		In the LS mode (1.5 Mbps)	-	-	3	mA
		In the suspend mode at 25 °C (Without connecting the pull-up resistor on DP)	-	-	200	uA
		In the suspend mode at 125 °C (Without connecting the pull-up resistor on DP)	-	-	2	mA
Tj	Operating junction temperature	-	-40		125	°C
IOZ5.25V	5-V tolerance current	Measured at DP/DM in the suspend mode	-	-	100	uA

Table 18 Static Characteristics of Analog I/O Pins (DP/DM)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
USB 2.0 Transceiver (HS) Input levels (Differential receiver)						
V_{HSDIFF}	High-speed differential input sensitivity	|VI(DP)– VI(DM)| Measured at the connection as an application circuit	300	-	-	mV
V_{HSCM}	High-speed data signaling common mode voltage range	-	-50	-	500	mV
V_{HSSQ}	High-speed squelch	Squelch detected	-	-	100	mV

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	detection threshold	No squelch detected	200	-	-	mV
VHSDSC	High-speed disconnection	Disconnection detected	625	-	-	mV
	detection threshold	Disconnection not detected	-	-	525	mV
Output levels						
VHSOI	High-speed idle level output voltage (Differential)	-	-10	-	10	mV
VHSOL	High-speed low level output voltage (Differential)	-	-10	-	10	mV
VHSOH	High-speed high level output voltage (Differential)	-	360	400	440	mV
VCHIRPJ	Chirp-J output voltage (Differential)	-	700	-	1100	mV
VCHIRPK	Chirp-K output voltage (Differential)	-	-900	-	-500	mV
IDP/DM	Allowable output current of DP/DM	When the termination is 45 0 ±10%	14.55	17.78	21.79	mA
Resistance						
RDRV	Driver output impedance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
ZHSTERM	Differential impedance	-	76.5	90	103.5	Ω
VBUS output threshold levels						
VV 日 USVALID	Valid VBUS level for the operation	-	4.4	-	4.75	V
VAVALID	Valid level of A device	-	0.8	-	2.0	V
VBVALID	Valid level of device	-	0.8	-	4.0	V
VSESSEND	Session end level	-	0.2	-	0.8	V
USB 1.1 transceiver (FS/LS)						
Input levels (Differential receiver)						
VDI	Differential input sensitivity	|V|(DP) - V|(DM)|	0.2	-	-	V
Vcm	Differentia |	-	0.8	-	2.5	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	common mode voltage					
zhsdrv	Driver output resistance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
RPU1	Pull-up resistor during idle	Equivalent resistance used for the internal chip	900	-	1575	Ω
RPU2	Driver output resistance	Equivalent resistance use internal chip	525	-	1515	Ω
RPD	Driver output resistance	Equivalent resistance used for the internal chip	14.25	-	24.8	kΩ
Input levels (Single-ended receiver)						
VSE	Single-ended receiver threshold	-	0.8	-	2.0	V
Output levels						
VOL	Low-level output voltage	-	0	-	0.3	V
VOH	High-level output voltage	-	2.8	-	3.6	V

Table 19 Dynamic Characteristics of Analog I/O Pins (DP/DM)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Driver Characteristics High-speed Mode						
THSRDRATE	High-speed TX data rate		479.76		480.24	Mbps
THSRDRATE	High-speed RX data rate		479.76		480.24	Mbps
tHSR	High-speed differential rise time		500	-	-	ps
tHSF	High-speed differential fall time		500	-	-	ps
Full-speed Mode						
TFSDRATE	Full-speed TX data rate		11.99	-	12.01	Mbps
TFSRDRATE	Full-speed RX data rate		11.99	-	12.03	Mbps

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tFR	Rise time	CL= 50 pF 10% ~ 90% of |VOH–VOL|	4	-	20	ns
tFF	Fall time	CL= 50 pF 90% ~ 10% of |VOH – VOL|	4	-	20	ns
tFRMA	Differential rise time/faltime matching (FR/tFF)	Excluding the first the transition from idle mode	90	-	110	%
VCRS	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Low-speed Mode						
TLSDRATE	Low-speed TX data rate	-	1.50	-	1.50	Mbps
TLSRDRATE	Low-speed RX data rate	-	1.49625	-	1.50375	Mbps
tLR	Rise time	CL= 200 pF ~ 600 pF 10% ~ 90% of |VOH–VOL|	75	-	300	ns
tLF	Fall time	CL= 200 pF ~ 600 pF 10% ~ 90% of |VOH–VOL|	75	-	300	ns
tFRMA	Differential rise time/faltime matching (FR/tFF)	Excluding the first the transition from idle mode	80	-	125	%
VCRS	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3		2.0	V
Driver Timing High-speed Mode						
	Driver waveform requirement	Please refer to the eye pattern of template 1.	Please follow template 1 described in the USB Specification			
Full-speed mode	VI, FSE0, OE to DP, DM Propagation delay	For detailed descriptions of VI, FSE0, and OE, please refer to the USB 1.1 Specification.	-	-	15	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TFDEOP	Source jitter for differential transition to SE0 transition		-2	-	5	ns
TJR1	Receiver jitter	To the next transition	-18.5	-	18.5	ns
TJR2	Receiver jitter	For paired transition	-9	-	9	ns
TFEOPT	Source SE0 interval of EOP		160	-	175	ns
TFEOPR	Receiver SE0 interval of EOP		82	-	-	ns
TFST	Width of SE0 interval during differential transition		-	-	14	ns
Low-speed Mode						
TLDEOP	Source jitter for differential transition to SE0 transition		-40	-	100	ns
TJR1	Receiver jitter	To the next transition	-75	-	75	ns
TJR2	Receiver jitter	For paired transition	-45	-	45	ns
TLEOPT	Source SE0 interval of EOP		1.25	-	1.5	ns
TLEOPR	Receiver SE0 interval of EOP		670	-	-	ns
TLST	Width of SE0 interval during differential transition		-	-	210	ns
Not specified: Low-speed delay time is dominated by the slow tLR and tLR .						
Receiver Timing **High-speed mode (Template 4, USB specification rev. 2.0)**						
	Data source jitter and receiver jitter tolerance	Please refer to the eye pattern of template 4.	Please follow template 4 described in the USB Specification.			
Full-speed Mode						
tPLH(rcv) tPHH(rcv)	Receiver propagation delay (DP; DM to RX_DP, RX_DM)	For detailed descriptions of RCV, please refer to the USB 1.1 Specification.	-	-	15	ns
tPLH(single) tPHL(single)	Receiver propagation delay (DP; DM to RX_DP, RX_DM)18	-	-	-	18	ns

Table 20 Reliability Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
HBM	ESD Human Body mode	-	-	-	2.0	KV
MM	ESD Machine Mode	-	-	-	200	V
CDM	ESD Charged Device Mode	-	-	-	500	V
VLatch	Latch-up voltage	VCC33A_HSRT and VCC33A_PLL domain	-	-	5.4	V
VLatch	Latch-up voltage	VCC10D_U20 domain	-	-	1.98	mA
ILatc	Latch-up current	-	-	-	400	mA

Switching Characteristics

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics.

Clock Performance

Table 21 Global Clock Performance

Symbol	Max Frequency	Units
GCLK	400	MHz

JTAG Switching Characteristics

Table 22 JTAG Clock Performance

Symbol	Max Frequency	Units
TCK	50	MHz

PS Switching Characteristics

Table 23 PS Clock Performance

Symbol	Max Frequency	Units
SCLK	50	MHz

PLL Specifications

Table 24 PLL Specifications

Symbol	Description	Min	Typ	Max	Unit
VDDIO	IO power voltage	2.375	2.5	2.625	V
		3.135	3.3	3.465	V
Fin	Input clock freq.	2		500	MHz
Fpfd	PFD input freq.	2		125	MHz
Fout	Output freq.	10		1250	MHz

Symbol	Description	Min	Typ	Max	Unit
Fvco	VCO operation freq.	600		1250	MHz
Tlock	Lock time			100	us
Duty	Output clock duty cycle	45	50	55	%
N	Input divider	1		256	--
M	Loop divider	1		256	--
MP *1	VCO post divider	1		16	--
C0~C3	Output divider	1		256	--
Ntmp	Output clock delay	0		255	--
Terr	Static phase error	-10		10	Degree
Ivddio	active power consumption			10	mA
Trst	Pulse width on reset signal	1			Us
Ipd	Total power-down current			30	uA
Tjit	Jitter performance	90		130	ps

I/O Timing

Table 25 Single-Ended I/O Performance

IO Standard	Primary Usage	Driving Strength	Max Frequency
LVCMOS/LVTTL	1.5v general purpose	4mA	75MHz
		8mA	125MHz
		12mA	150MHz
		16mA	175MHz
	1.8v general purpose	4mA	125MHz
		8mA	175MHz
		12mA	200MHz
		16mA	230MHz
	2.5v general purpose	4mA	175MHz
		8mA	200MHz
		12mA	230MHz
		16mA	230MHz
	3.3v general purpose	4mA	200MHz
		8mA	230MHz
		12mA	230MHz
		16mA	230MHz

Table 26 LVDS I/O Performance

IO Standard	Attribute	Min	Typ	Max
LVDS	Frequency			400MHz

Table 27 SSTL/HSTL I/O Performance

IO Standard	Attribute	Min	Typ	Max
SSTL/HSTL	Frequency			400MHz

Table 28 DDR memory Performance

IO Standard	Attribute	Min	Typ	Max
DDR	Frequency			333MHz

Table 29 I/O adjustable Input/Output Delay @200MHz

Delay setting	Min	Typ	Max	Units
0		0.18		ns
1		0.26		ns
2		0.35		ns
3		0.43		ns
4		0.5		ns
5		0.60		ns
6		0.68		ns
7		0.76		ns
8		0.83		ns
9		0.9		ns
10		0.95		ns
11		0.99		ns
12		1.08		ns
13		1.15		ns
14		1.17		ns
15		1.3		ns

LP Timing

Table 30 LP Timing

Symbol	Description	Min	Max	Units
tco	When reading from the Flip-Flop, the time from the active transition at the CLK input to data appearing at the QS (QX) output	446	497	ps
tsu	Time from the setup of data at the LUT input to the active transition at the CLK input of the Reg	7	989	ps
th	Time from the active transition at the CLK input to the point where data is last held at the input	-878	177	ps
tp	The time it takes for data to travel from	68	1062	ps

Symbol	Description	Min	Max	Units
	the LP's Flip-Flop input to the output			

PLB Performance

Table 31 PLB Performance

Symbol	Description	Min	Max	Units
ADD16	16 bit adder performance @ recommended operating condition.	400		MHz
ADD32	32 bit adder performance @ recommended operating condition.	360		MHz
ADD64	64 bit adder performance @ recommended operating condition.	215		MHz
CNT8	8 bit counter performance @ recommended operating condition.	400		MHz
CNT16	16 bit counter performance @recommended operating condition.	400		MHz
CNT32	32 bit counter performance @ recommended operating condition.	400		MHz

EMB Performance

Table 32 EMB Performance

Symbol	Description	Min	Max	Units
EMB5K	Using register path.	260		MHz
	Not using the register path.	200		MHz
EMB18K	Using register path.	260		MHz
	Not using the register path.	200		MHz

DSP Performance

Table 33 DSP Performance

Symbol	Description	Min	Max	Units
DSP 12x9-bit multiplier	DSP using register path.	260		MHz
	DSP not using the register path.	200		MHz
DSP 18x18-bit multiplier	DSP using register path.	260		MHz
	DSP not using the register path.	200		MHz

ARM Cortex-M3 Performance

Table 34 ARM Cortex-M3 Performance

Symbol	Description	Min	Max	Units
ARM Cortex-M3	ARM Cortex-M3 core		300	MHz

AHB Bus Performance

Table 35 AHB Bus Performance

Symbol	Description	Min	Max	Units
AHB Bus	AHB Bus		300	MHz

This part lists the pin definitions and rules as well as available package information. For the detailed pin list please see the Pin List doc.

4. Pins and Package

Pins Definitions and Rules

Table 36 Pins Definitions and Rules

Pin Name	Direction	Description
User I/O Pins		
IOXX_# IO_XXY_#	inout	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.
Multi-Function Pins		
IOXXX/ZZZ_# IO_XXY/ZZZ_#		Multi-function pins are labeled IOXXX/YYY_# and IO_XXY/ZZZ_#, where YYY represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Multi-Function Pins: SPI serial configuration Pins		
FLS_SCLK	Input/ output	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into device. In active serial configuration mode, SCLK is a clock output from device. The pin can be used as regular user I/Os after configuration.
FLS_SI	output	Dedicated configuration data output pin in AS mode. No configuration function in PS mode. The pin can be used as regular user I/Os after configuration in AS mode
FLS_SO	Input/ output	Serial data input from external master in PS mode or from spi flash in AS mode. The pin can be used as regular user I/Os after configuration.
FLS_CSN	output or input	Chip select output to enable a SPI Flash in AS mode or input as a HME-M7 device select. This output is used during AS mode. The pin can be used as regular user I/Os after configuration in AS mode. it is used as chip selection control (input) during PS.The pin can

Pin Name	Direction	Description
		be used as regular user I/Os after configuration in PS mode.
FLS_WP	Input/ output	Write Protect Output (Data Input Output 2)
FLS_HOLD	Input/ output	Hold Output (Data Input Output 3)
Multi-Function Pins: Configuraiton		
CONF_DONE	output	This is a dedicated configuration status pin, the pin will output high during configuration. The pin can be used as regular user I/Os after configuration.
CFG_MODE	input	0: Active Serial mode, 1 Passive Serial mode. The pin can be used as regular user I/Os after configuration.
nCONFIG	input	Chip global reset input. Active low.
Dedicated Pins: JTAG		
TCK	input	TCK Input Boundary-Scan Clock.
TDI	input	TDI Input Boundary-Scan Data Input.
TDO	output	TDO Output Boundary-Scan Data Output.
TMS	input	TMS Input Boundary-Scan Mode Select.
Multi-Function Pins: Clock Pins		
CLK[X], CLK[X]	input	These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
Dedicated Pins: Crystal Pins		
XIN	input	External crystal input. If not used it is better to connect to GND.
XOUT	output	Output to crystal. Not used can be floating.
Dedicated Pins: RTC Pins		
RTC_XIN	input	External crystal input for RTC 32K clock. If not used it is better to connect to GND.
RTC_XOUT	output	32K clock output to crystal. If not used can be floating.
RTC_VDDBAT	N/A	RTC power. 2.0-3.3V.
RTC_GNDBA	N/A	RTC ground.
Dedicated Pins: ARM Pins		
NMI	input	ARM dedicated NMI input.
Dedicated Pins: Ethernet Pins		
ETH_PHY_TXER_O	output	PHY Transmit Error
ETH_PHY_TXD_O[7:0]	output	Data transmitted to the PHY
ETH_PHY_RXD_I[7:0]	input	Data received from the PHY.

Pin Name	Direction	Description
ETH_PHY_CRS_I	input	PHY CRS This signal, valid only in the GMII/MII mode, is asserted by the PHY when either the transmit or receive medium is not idle. The PHY de-asserts this signal when both transmit and receive medium are idle. This signal is not synchronous to any clock
ETH_PHY_INTF_SEL_I[2]	input	PHY Interface Select, connect to GND if Ethernet is enabled.
ETH_PHY_RXER_I	input	PHY Receive Error
ETH_PHY_TXEN_O	output	PHY Transmit Data Enable
ETH_GMII_MDO_IO	inout	MDIO is the management data.
ETH_CLK_RX_I	input	Receive Clock
ETH_PHY_RXDV_I	input	PHY Receive Data Valid.
ETH_GMII_MDC_O	output	MDC is the management data clock reference for the serial management interface.
ETH_CLK_TX_I	input	Transmit Clock
ETH_PHY_COL_I	input	GMII and MII Collision
Dedicated Pins: DDR Pins		
DQ[15:0]	inout	Data input/output
DM[1:0]	output	Input data mask
DQS0/1, DQS0/1N	inout	Data strobe
VREF0, VREF1	N/A	Reference voltage
CKE	output	Clock enable
BA[2:0]	output	Bank address inputs
A[14:0]	output	Address inputs
CLK, CLKN	output	DDR Clock
RASN	output	Command inputs
CASN	output	Command inputs
WEN	output	Command inputs
RESETN	output	DDR Reset. low active
ODT	output	On-die termination
CSN	output	Chip select, low active
Dedicated Pins: USB Pins		
XSCI	input	USB PHY crystal input
XSCO	output	USB PHY crystal input
DM	inout	USB negative data pin
DP	inout	USB positive data pin
RREF	N/A	External 1% bias resistor. Requires a 12K resistor to ground.
ID	input	Analog input.

Pin Name	Direction	Description
		0: When the ID pin is grounded 1: When the ID pin is floating or with a 100-kΩ pull-down resistor
VBUS	N/A	USB power supply, 5V.
VCC33A_HSRT	N/A	Analog power for USB PHY, 3.3V.
VCC33A_PLL	N/A	Analog power for USB PHY PLL, 3.3V.
GND33A_HSRT	N/A	Analog GND for USB PHY.
GND33A_PLL	N/A	Analog GND for USB PLL.
Dedicated Pins: ADC Pins		
ADCI0-11P, ADCI0-11N	input	ADC input pin, can be used as general IO if not used
ADC_VIPP, ADC_VIPN	input	Dedicated ADC input
ADC_VINP, ADC_VINN	input	Dedicated ADC input
ADC_VREFP, ADC_VREFN	input	Dedicated ADC reference. When the external 1v accurate reference voltage source(+/-0.25%) is tied to the pin of VREFP , the ADC can be worked at the best performance. When VREFP is floating, On-chip Bandgap Reference(1.00V+/-3%) is activated. VREFP and VREFN must be treated as analog signal. To properly operate, CEXT(1uF~10uF) external capacitor is needed to be placed between this PIN and VREFN pin.
VDD_ADC	N/A	ADC power supply, 3.3V.
Dedicated Pins: Power		
VDD33	N/A	Digital power for Configuration which also supply all the PLLs power, 3.3V.
VDDIO_X	N/A	Digital power for IO,1.5/1.8/2.5/3.3V.
VDD_CORE	N/A	Digital power for core, 1.1V.
GND	N/A	Digital ground.

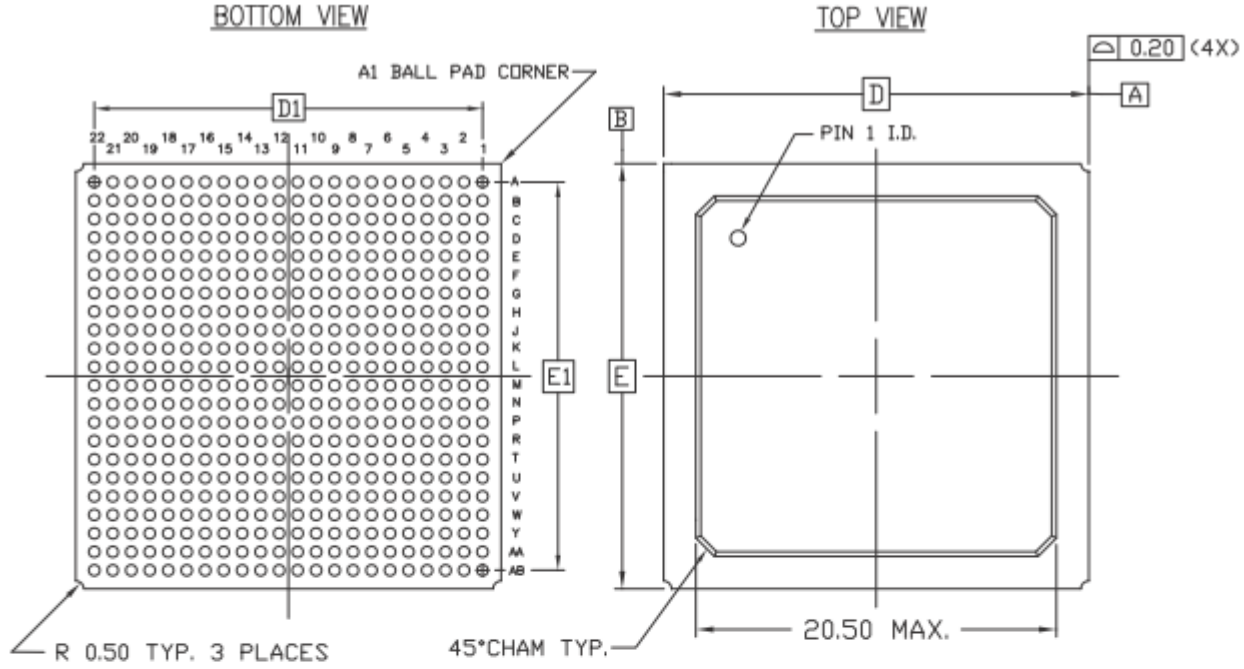
***Note**:*

(1) VDD33 is the power for JTAG/SPI Flash that must be 3.3V.

(2) There is a power sequence requirement: The VDD_CORE must be power on before the VDD33.

Package Information

FBGA484 Fineline BGA Package Specifications

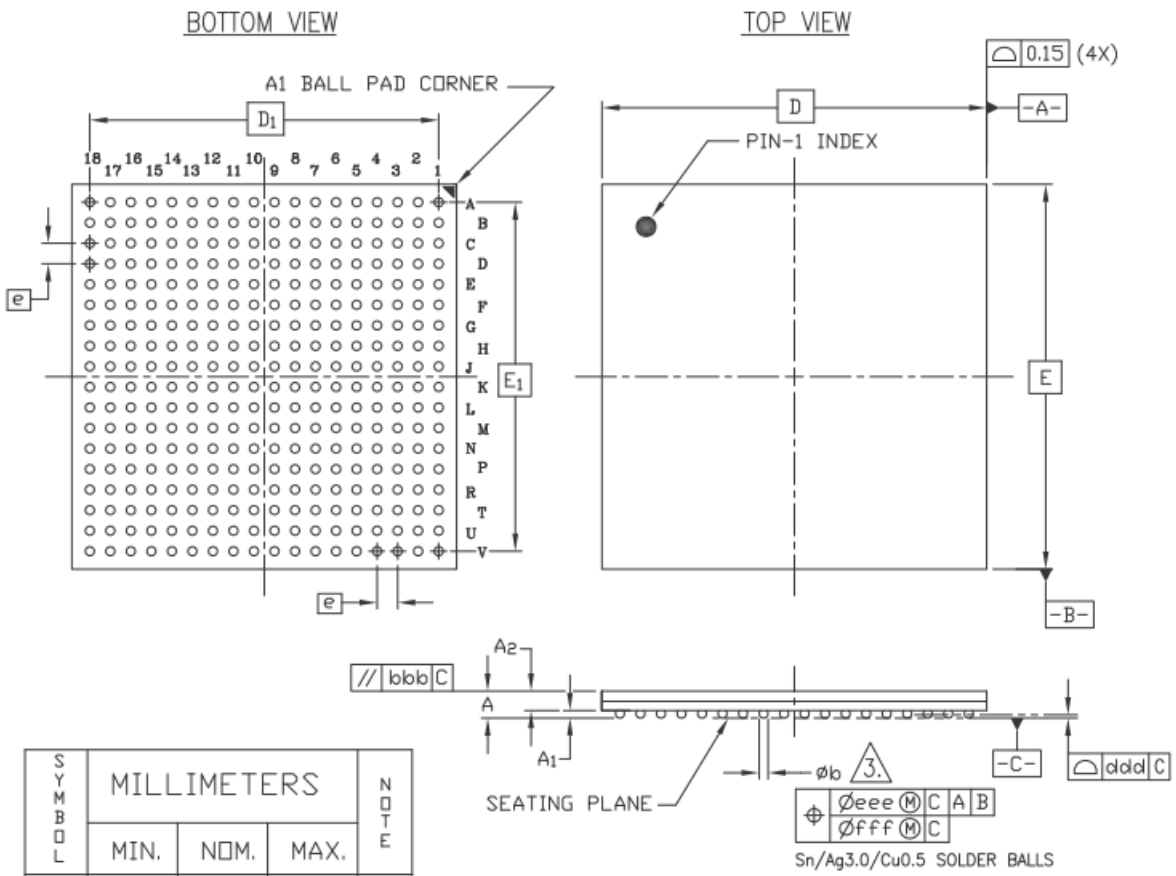


SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	2.20	2.60	
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAJ–1.

VBGA324 stands for 0.8mm pitch VFBGA

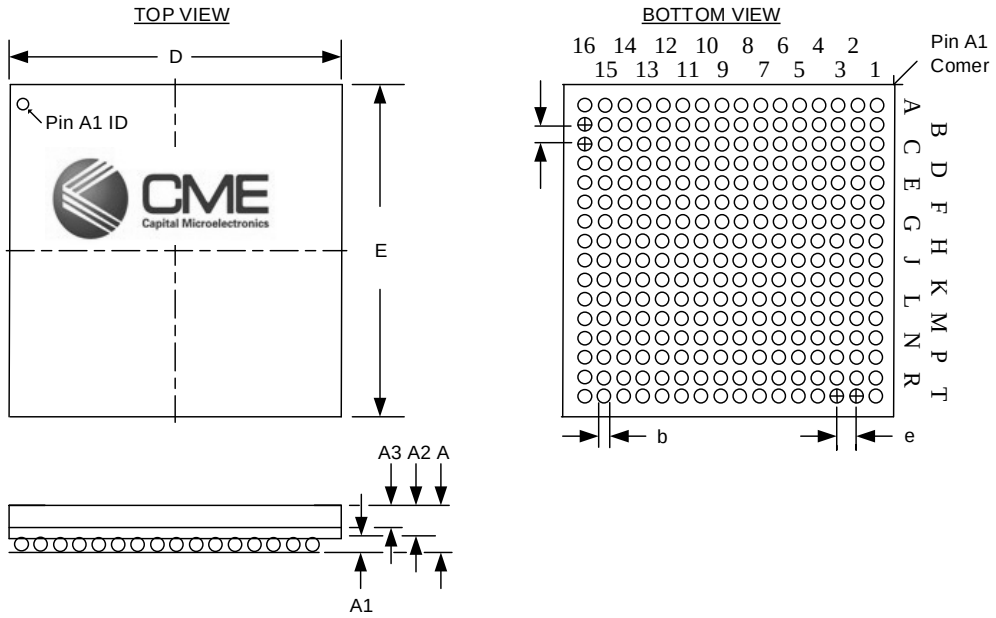


SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.00		1.50	
A_1	0.25	0.30	0.40	
A_2	0.75	0.90	1.10	
D/E	15.00 BSC			
D_1/E_1	13.60 BSC			
e	0.80 BSC			
øb	0.40	0.45	0.50	3
bbb			0.20	
ddd			0.20	
eee			0.15	
fff			0.08	
M	18			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE
5. CONFORMS TO JEDEC MO–275–KKAB–1

FBGA256 Fineline BGA Package Specifications

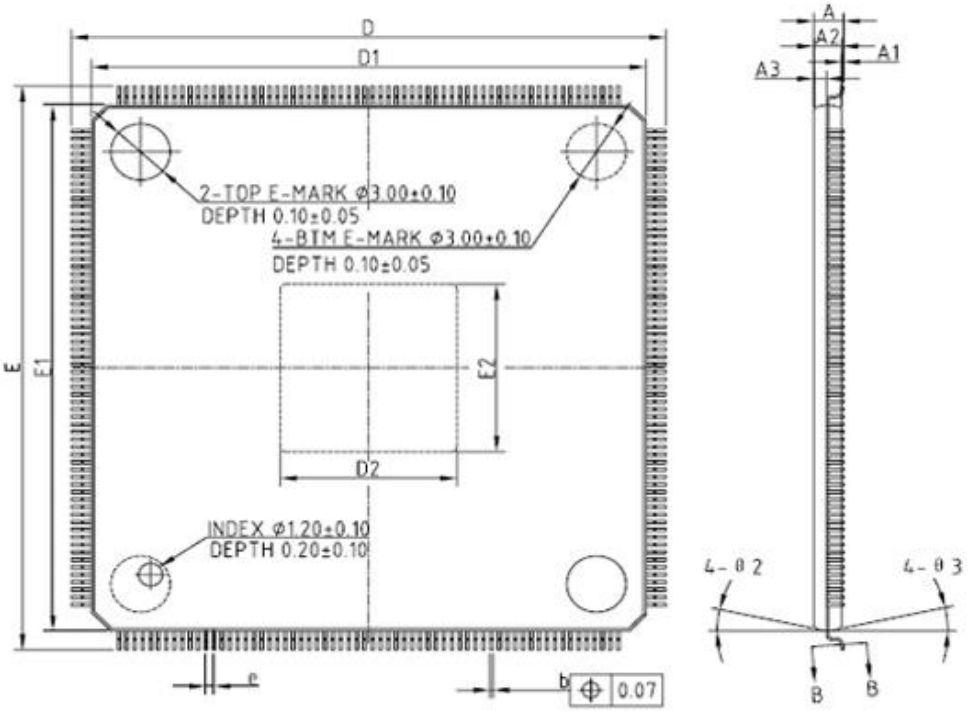


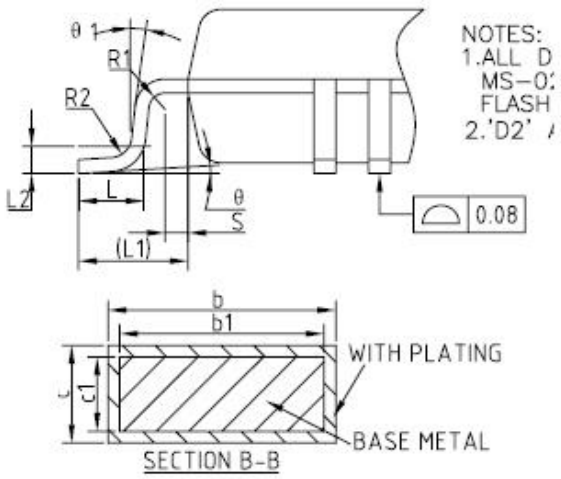
Package Information	
Description	**Specification**
Ordering Code Reference	F
Package Acronym	FBGA
Substrate Meterial	BT
Solder ball composition	Regular: 63Sn: 37Pb (Typ.) Pb-free: Sn: 3Ag: 0.5Cu (Typ.)
JEDEC Outline Reference	MO-192 Variation: DAF-1
Lead Coplanarity	0.008 inch (0.2 mm)
Weight	0.93 g (Typ.)
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Dimension Table			
Symbol	**Millimeters**		
	Min.	Nom.	Max.
A	1.35	1.45	1.55
A1	0.30	0.40	0.50
A2	0.85	1.05	1.25
A3	0.65	0.70	0.75
D		17.00 BSC	
E		17.00 BSC	
b	0.40	0.50	0.60
e		1.00 BSC	

Controlling dimension is in millimeters.
Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

LQFP256 Low profile Quad Flat Package Specifications





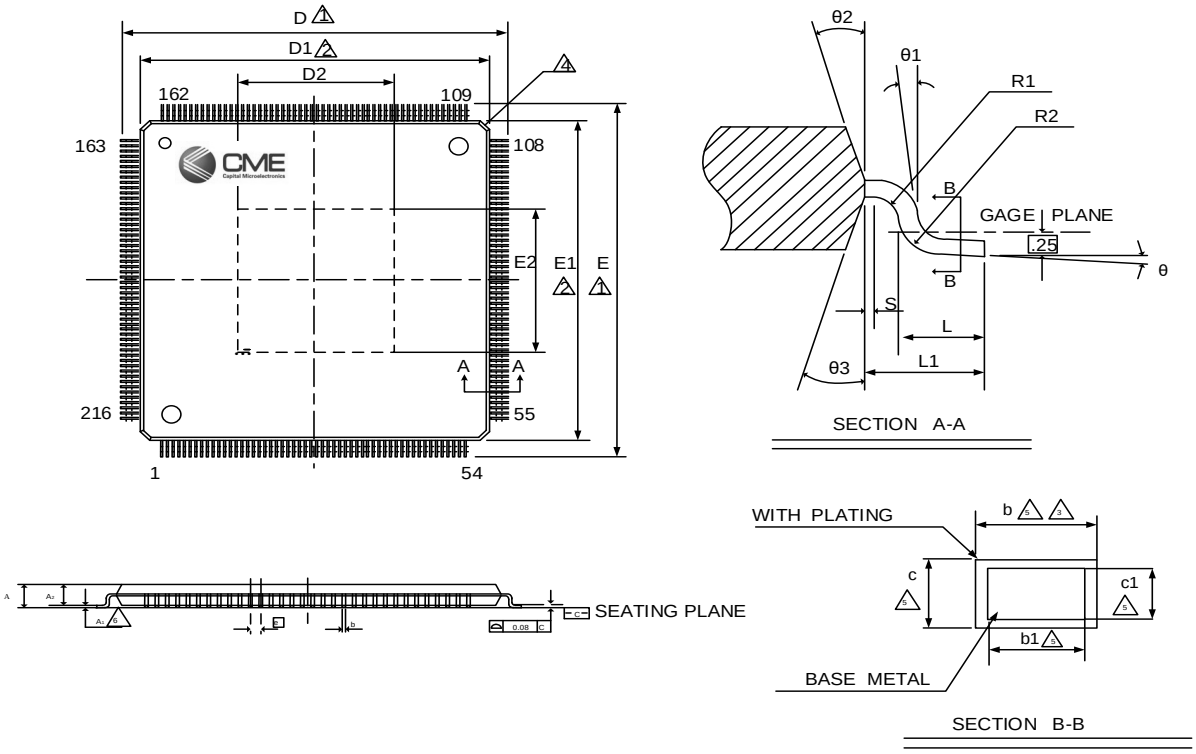
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	–	0.23
b1	0.13	0.16	0.19
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	29.80	30.00	30.20
D1	27.90	28.00	28.10
D2		8.92REF	
E	29.80	30.00	30.20
E1	27.90	28.00	28.10
E2		8.92REF	
e	0.30	0.40	0.50
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BJC-HD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. "D2" AND "E2" ARE VARIABLES DEPENDING ON DIE PAD SIZES.

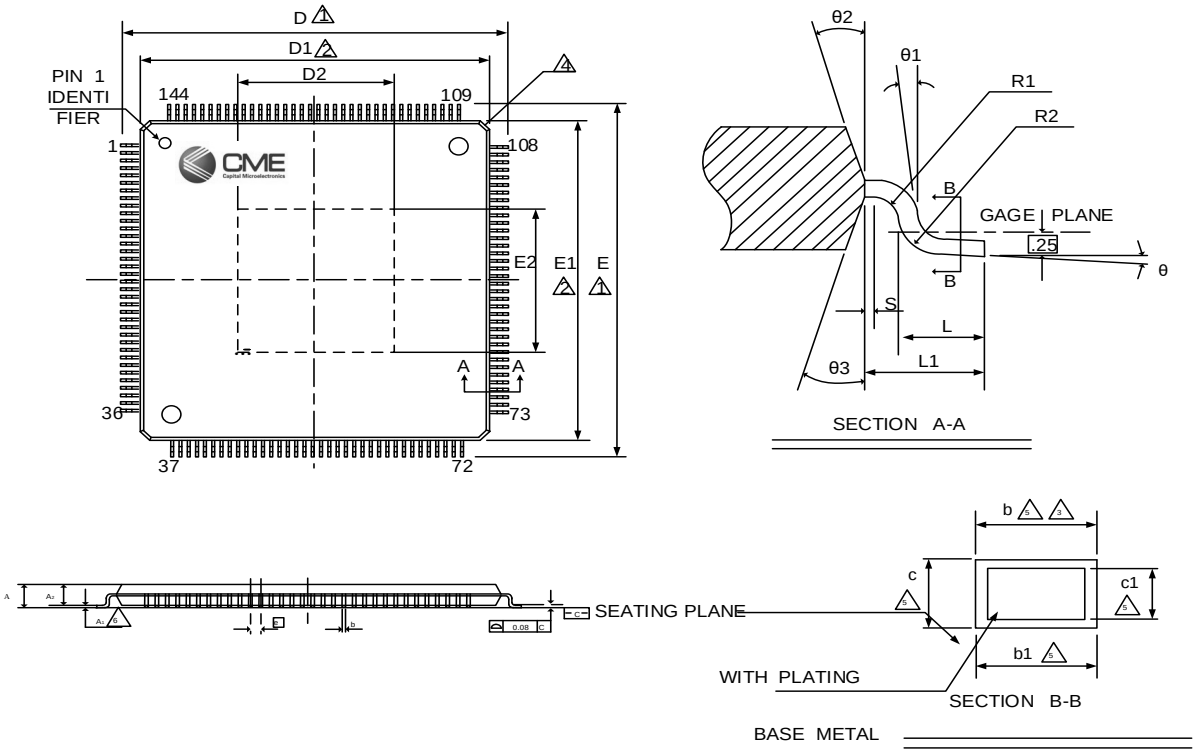
LQFP216 Low profile Quad Flat Package Specifications



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	0.14	0.20
c1	0.09	0.12	0.16
D	25.85	26.00	26.15
D1	23.90	24.00	24.10
E	25.85	26.00	26.15
E1	23.90	24.00	24.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	—	—
R2	0.08	—	—
S	0.20	—	—
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°

1. TO BE DETERMINED AT SEATING PLANE -C-
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION
   INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS
   OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD
   BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING
   PLANE
7. CONTROLLING DIMENSION : MILLIMETER.

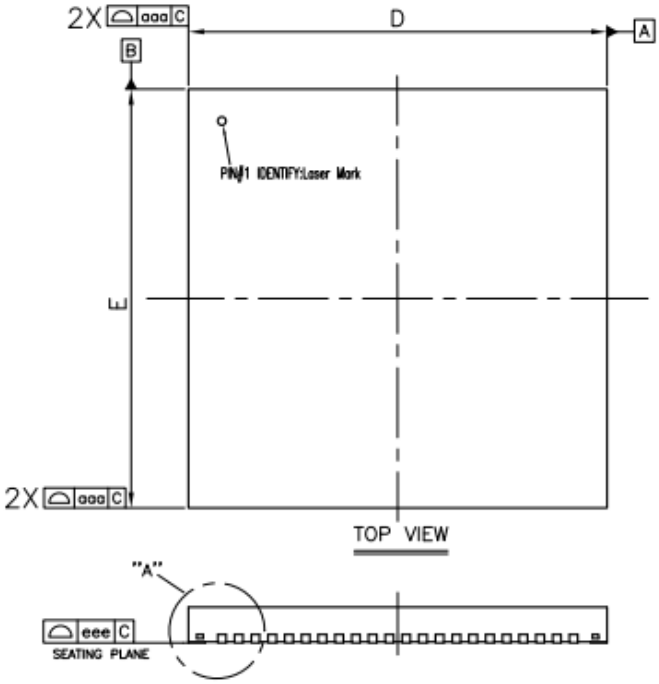
LQFP144 Low profile Quad Flat Package Specifications

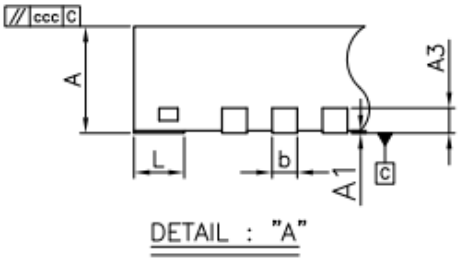


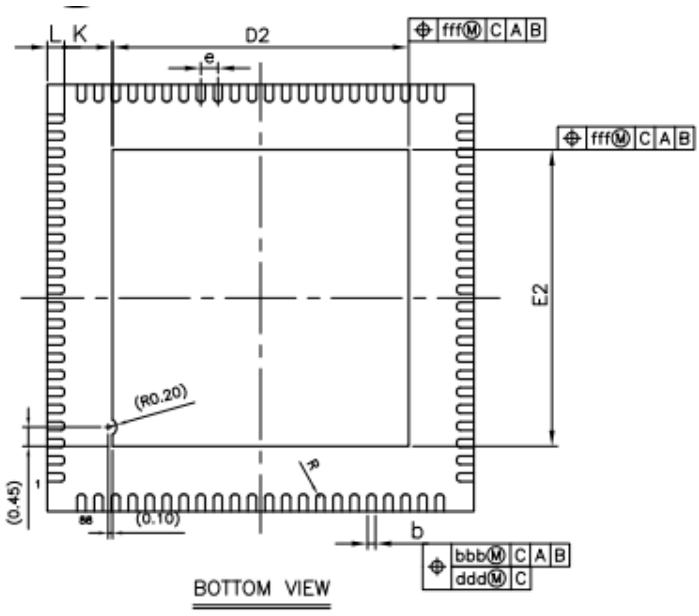
Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	—
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.20 REF		
c	0.12	—	0.20
c1	0.13 REF		
D	21.85	22.00	22.15
D1	19.90	20.00	20.10
E	21.85	22.00	22.15
E1	19.90	20.00	20.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R	0.15 REF		
R1	0.15 REF		
S	0.19 REF		
θ	0°	3.5°	7°
θ1	7° REF		
θ2	12° REF		
θ3	12° REF		

1. TO BE DETERMINED AT SEATING PLANE -C-
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION
   INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS
   OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD
   BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING
   PLANE
7. CONTROLLING DIMENSION : MILLIMETER.
   TO THE LOWEST POINT OF THE PACKAGE BODY.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BFB

QFN88 Quad Flat No-leads Package Specifications







Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D2	6.85	6.95	7.05	0.270	0.274	0.278
E2	6.85	6.95	7.05	0.270	0.274	0.278
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

This appendix lists the heart revisions of this doc for your reference.

Ordering Information

All part numbers have the following conventions:

Table 37 Part number conventions

Vendor	Product Family	LUT Density	Device Type	Flash	Package Type	Temperature	Speed Grade
HME-	M7	A	12	N5	F484	C	7

Product Series

- ❒ **M7 Hua/BAO SHAN family**

Device Type

- ❒ **A Analog + FPGA + MCU + SRAM**
- ❒ **P Pure FPGA**

LUT Density

- ❒ **12 12K LUTs**
- ❒ **09 9K LUTs**
- ❒ **07 7K LUTs**

Configuration NVM (SPI-flash) Option

- ❒ **N0 Without internal SPI-flash**
- ❒ **N5 With 16Mb internal SPI-flash**

Package Type: <type><#>

- ❒ **T Thin Quad Flat Pack (TQFP)**
- ❒ **L Low profile quad flat package (LQFP)**
- ❒ **Q Quad Flat No-leads package (QFN)**
- ❒ **V VFineline BGA**
- ❒ **F Fineline BGA**
- ❒ **# Pin number (208 for 208pin, 100 for 100pin…)**

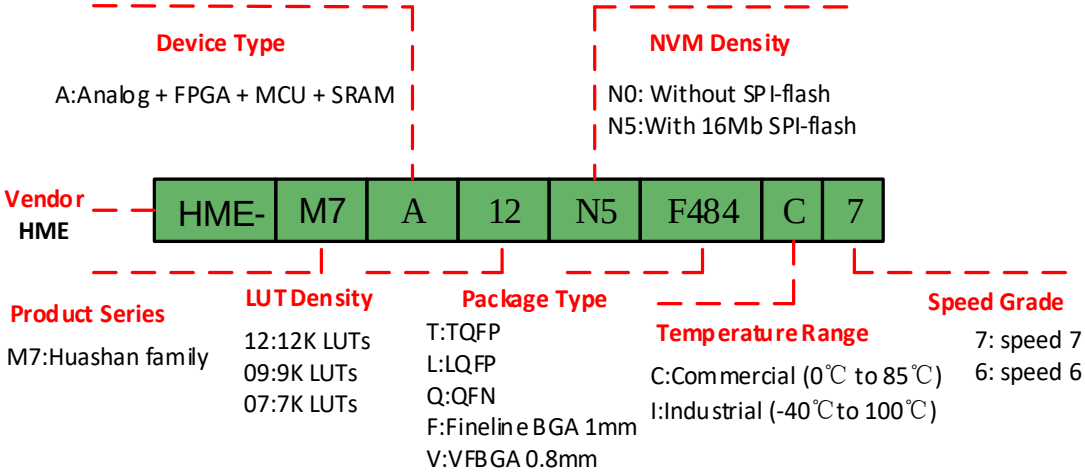
Temperature Range

- ❒ **C Commercial (0℃ to 85℃)**
- ❒ **I Industrial (-40℃ to 100℃)**

Speed Grade

- ❒ **# Speed (7 for speed 7, 6 for speed 6, …)**

Example: **HME-M7C12N5F484C7**



This appendix lists the heart revisions of this doc for your reference.

Revision History

The table below shows the revision history for this document.

Release Date	Doc Version	Revision
June, 2014	CME-M7DSE01	Initial release.
July, 2014	CME-M7DSE02	■ Update VDD CORE parameters, see Table 6 Recommended Basic Operating Conditions ■ Add sections of JTAG Switching Characteristics and PS Switching Characteristics ■ Update ETH_PHY_INTF_SEL_I and VDD_CORE parameters, see Table 36 Pins Definitions and Rules ■ Update Figure 2 CAP Diagram
October, 2014	CME-M7DSE03	■ ADD I/O delay table ■ ADD power sequence requirement ■ Update LQFP144 /216 package ■ Change the part number HME-M7CxxN4 to HME-M7CxxN5 ■ Delete LQFP216 DDR support ■ Update configuration scheme
March, 2015	CME-M7DSE04	■ Update configuration pins description
March, 2016	CME-M7DSE05	■ Update Feature Summary to add M6 information ■ Update Package Information to add M6 information ■ Update Ordering Information to add M6 information
July,2018	HME-M7DSE06	■ Update ESD value
Oct.2018	HME-M7DSE07	■ Add QFN88 package information
Dec.2018	HME-M7DSE08	■ Update Feature Summary,Package Information